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Ltr	REVISIONS	DATE	INITIALS
A	As Issued	6-13-79	

Model No.	Stock No. SEE TABLE ON PAGE 6
Title 40K ROM	
Description DETAILED DESCRIPTION	Date 6-13-79
Author Bond Ying	Sheet No. 1 of 5
	Drawing No. 4-1LB7-9001-1

I GENERAL DESCRIPTION

The CMOS 40K ROM circuit consists of 40960-bit Read Only Memory, with associated addressing control, and timing logic. (Figure I).

The 16-bit addresses come in serially on a bidirectional line ISA. 12-bit addresses are used to access one of 4096 10-bit words of the memory. 4-bit addresses are used to select one of 16 ROM chips.

The 10-bit word (I_0, I_1, --- I_9) of the output of the ROM are serially shifted out through ISA line during SYNC signal is active.

The CMOS 40K ROM circuit has power sleep mode which will be used to save power during idling conditions.

There are three pads on this CMOS 40KROM circuit. One pad is used to disable the chip. Two pads are used to select the chip by hard wire connections to V_{CC} or GND. These three pads are TEST,13,14.

II DETAILED DESCRIPTION

Refer Fig. 1 and Fig.2. Five signals are used by CMOS 40K ROM circuit for communication to central processing unit (CPU).

2.1 ISA - This is a bit serial bidirectinal line. During bit time 14 (T14) through bit time 29 (T29), the 16 addresses are input serially (LSB or A_0 first) on the ISA line from CPU to 40K ROM circuitry.

The first 12-bit addresses are used to access the ROM word. The last 4-bit addresses combined with Pad 13 and Pad 14 are decoded for chip select. For example, if Pad 13 and Pad 14 connect to V_{CC}, address A13 and A14 should be at V_{CC} level in order to select this chip.

2.1 CONT'D

The 10-bit ROM word is first latched in the Instruction Register. During SYNC signal active, the 10-bit ROM work is shifted out serially through ISA line.

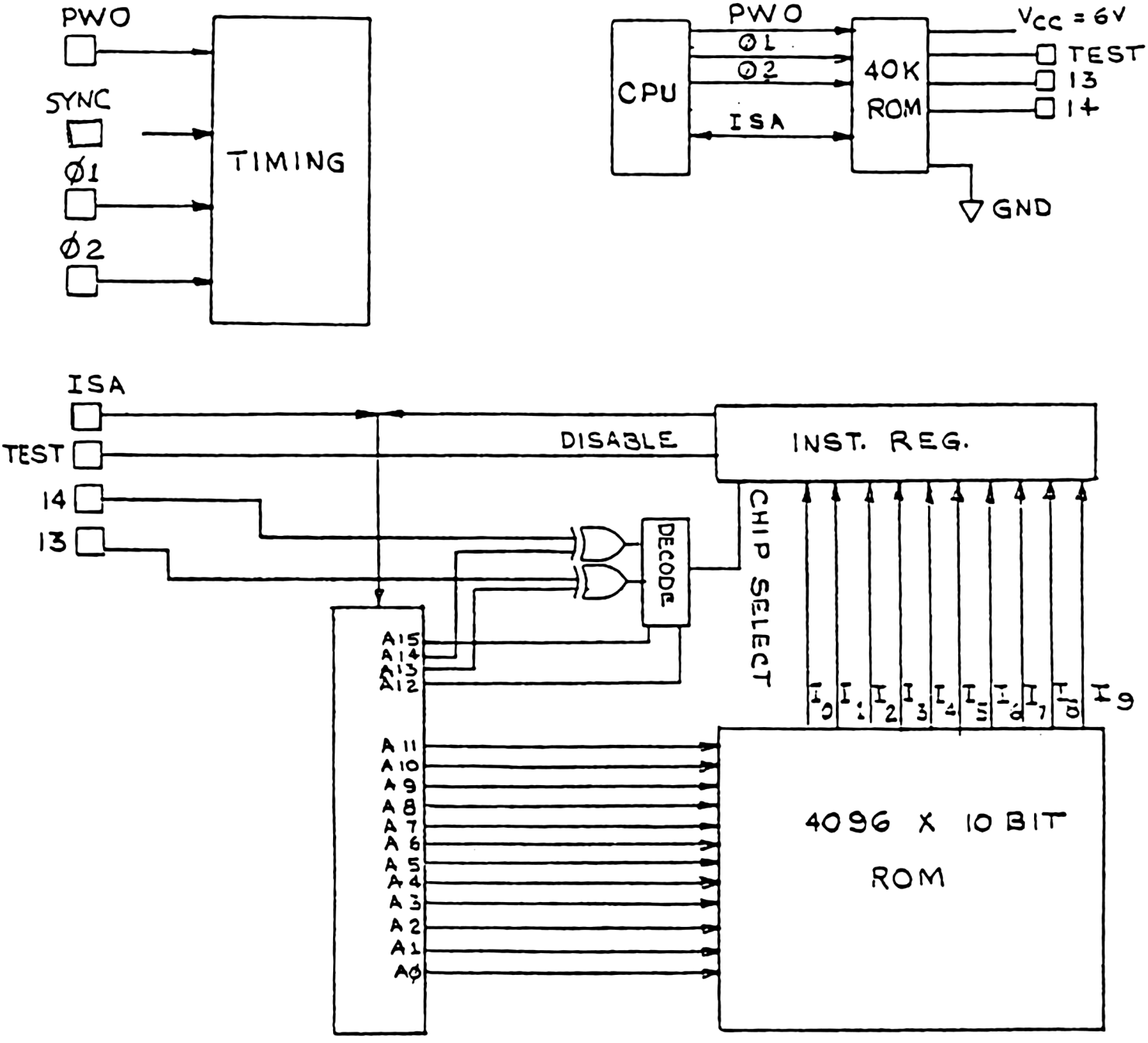
2.2 PWO - This signal is used to synchronize the timing of the 40K ROM chip and also to control the chip in active mode or sleep mode. During PWO signal is high, the ROM chip is active. If the PWO signal goes to low, the ROM chip is in sleep mode which means no clock running through the chip circuitry, any mode in this chip will stay in high or low level.

2.3 SYNC-This signal is used to synchronize the timing of the chip. The rom still get its synchronization with the system even if the sync line is grounded. The rom can be synronized by the PWO line.

2.4 $\emptyset_1$, $\emptyset_2$ - These two clock lines come from CPU. They are active two pulses before PWO signal goes high and stays active during PWO high and maintain another two pulses after PWO goes low.

2.5 TEST - This pad normally pulls up to high. If this pad is forced to grund, it will disable the chip.

2.6 13, 14 - These two pads can be programmed to high or low or hard wired to high or low.



BLOCK DIAGRAM

FIGURE I

				MODEL	SIZE NO SEE PAGE 6
				DETAILED DESCRIPTION - CMOS 40K ROM	
				BY Bond Ying	DATE 6-13-79
LT	P.C. NO	APPROVED	DATE	APPD	SHEET NO 4 OF 6

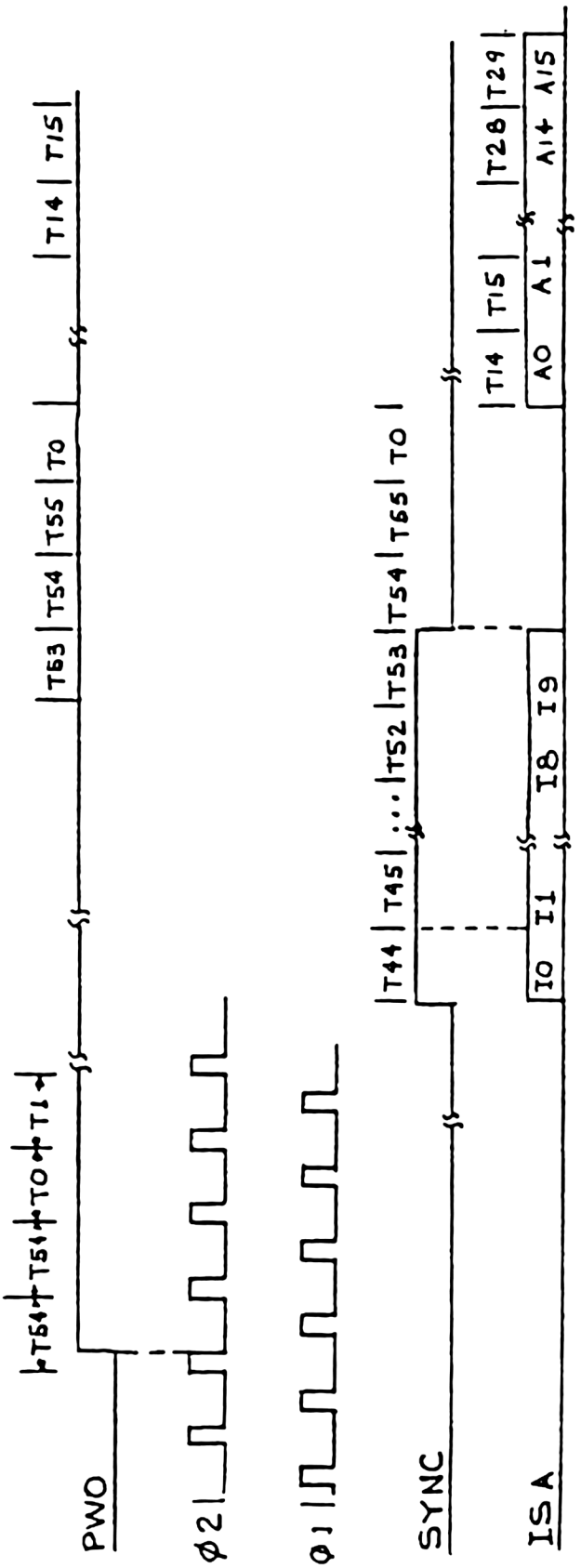


FIGURE II TIMING

MODEL		STK NO	SEE PAGE 6
DETAILED DESCRIPTION - CMOS 40K ROM			
BY Bond Yiee		DATE	6-13-79
APPD		SHEET NO	5 OF 6

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TABLE

1LB7-0001
1LB7-0002
1LB7-0003
1LB7-0004
1LB7-4005
1LB7-4017
1LB7-4018
1LB7-4019
1LB7-4020
1LB7-4021
1LB7-4022
1LB7-4023

LTR	P C NO	APPROVED	DATE

REVISIONS

MODEL	STK NO See Above
40 K Rom/ Detailed Description	
BY Bond Ying	DATE 6-13-79
APPD	SHEET NO. 6 OF 6
SUPERSEDES	DWG NO A-1LB7-9001-1

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Ltr	REVISIONS	DATE	INITIALS
A	As Issued	4-27-78	RQ / [illegible]

Model No.	Stock No. 1826-0566	
Title IC-LINEAR BIPOLAR CIRCUIT		
Description DETAILED DESCRIPTION		Date 2-27-78
By John Wong		Sheet No. 1 of 4

I GENERAL DESCRIPTION

1.1 The Bipolar circuit is an extremely low current, low power device which performs all analog functions. It contains three temperature compensated voltage reference outputs for driving LCD's; a low level detect circuit; and a high efficient voltage converter circuit to give a constant 6V output with a wide range of battery input voltages. Along with the converter circuit, there is a control input to turn the entire chip on or off, and an output to indicate that the supply voltage is adequate for proper operation. This chip also goes into a standby mode when the control input is turned off, and it shuts off a majority of the circuits to obtain a very low standby current.
Figure 1 shows a simplified block diagram of the circuit. Along with the IC, several external components are required to perform the functions: RSET sets up a majority of the bias currents in the chip; LEXT is an external inductor for the Power Supply; COSC is the timing element for the internal oscillator; DEXT is the pass diode for the Power Supply; and CFILTER is the filter capacitor for the Power Supply.

II SIGNALS AND OPERATIONS

2.1 GND - System ground, OV. The Bipolar Chip has two ground inputs, analog and digital ground. It is necessary to connect them externally.

2.2 VBAT - Battery voltage input to power this chip and the source of power for the Power Supply. It's range is between 3.5V to 6V.

2.3 VCI - VCI is a control pin which enables or disables the chip. With VCI at OV, all the circuits in the chip are disabled.

2.3 Cont'd.

The only current consumed by the chip is the leakage current of less than 5 ua. V_{CC} becomes a voltage one diode drop below V_{BAT}, supply small leakage current to the CMOS chips. When VCI is brought to a high level, sourcing at least lua to the base of a transistor, all circuits on the chip turns on.

2.4 VCO - After VCI goes high enabling the chip, a certain amount of time is required for the oscillator and the power supply to charge up the V_{CC} output to 6V. When it passes the threshold of the voltage regulator (between 6.0 to 6.5V) a negative pulse is generated on VCO to indicate that V_{CC} is up to an operating level. After that time, the conditions of VCO are ignored until another VCI cycle.

2.5 V_{CC} - V_{CC} is the main supply for the CMOS circuits in the system. During normal operation, V_{CC} runs between 6.0 to 6.5V from Power Supply of this chip. with a VBAT input of 3.5V to 6.0V. In the sleep mode, (off with kept alive to memories) V_{CC} becomes VBAT voltage minus one diode drop. The range of current drain from V_{CC} is between 0 to 20 ma. This chip is designed to consume a very minimum current drain when ICC is 0.

2.6 OSC - OSC is an input for an external capacitor to control the oscillator frequency. The oscillator is used in the Power Supply circuit to drive the inductor. The oscillator is free running, the output is gated with the output of the voltage regulator circuit.

2.7 EXT IND - A pin to connect an inductor and a diode for the power supply.

2.8 RSET - RSET is a current adjust input to control a majority of BIAS currents in the chip. It can be set to allow minimum of quiescient current for the required ICC output. It is possible to increase the current through RSET to increase ICC current beyond the 20ma as specified.

2.9 LLD - LLD is a low level detection of the battery voltage. As VBAT drops below 3.7 to 3.9V, the LLD output goes active low signaling a low battery condition to the system. There is a built-in hysteresis on LLD to prevent oscillations.

2.10 L3V, L2V, L1V - These are three LCD drive voltages required for the liquid crystal display. The nominal voltage for L3V is 3.3V at 25°C and its output has a negative temperature coefficient of - 20 mv/°C in the range of 0° to 45°C. The L2V and L1V are scaled down 2/3 and 1/3 from the L3V output voltage. These outputs will source or sink currents.