C I R C U I T D E S C R I P T I O N S S E R I E S 4 0

1.	1LF5-0002 1LF5-0301	HP-41 CPU DESCRIPTION. HP-11C, 12C CPU DESCRIPTION.	42pp.
2.	1LA4-4001	HP-41 DISPLAY DRIVER DESCRIPTION	23pp.
3.	1LA7-9002-1	HP-41 RAM IC DESCRIPTION	6pp.
4.	1LB6-4001	PIL IC DESCRIPTION	9pp.
5.	1LB5-4001	PIL IC ELECTRICAL SPECIFICATION	14pp.

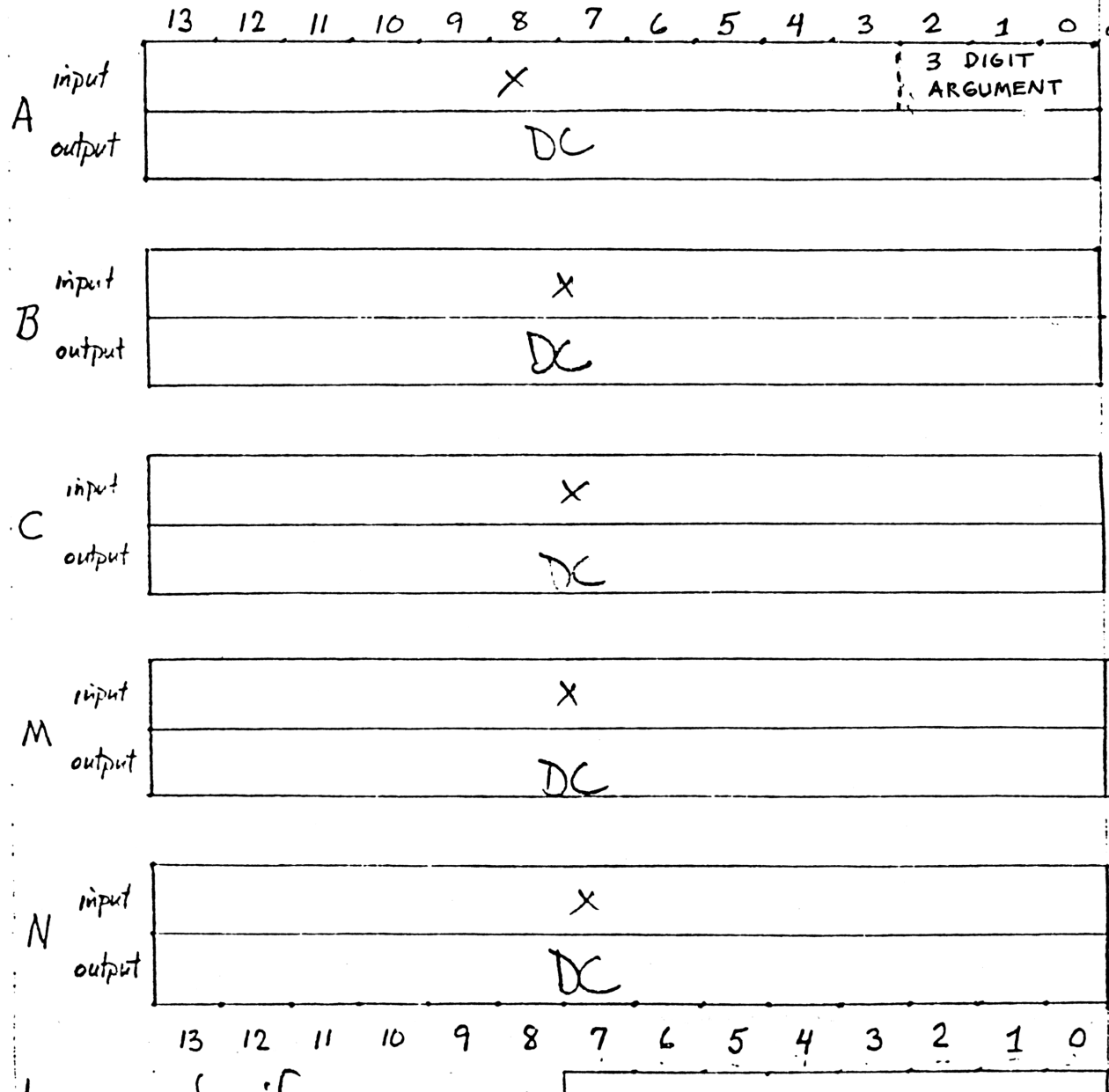
RJN

C I R C U I T D E S C R I P T I O N S S E R I E S 4 0

1.	1LF6-4001	TIME MODULE (+CX) IC DESCRIPTION.	30pp.
2.	1LF6-4001	TIME MODULE IC ELECTRICAL SPECIFICATION.	7PP.
3.	1LB4-4001	PERIPHERAL (82143) IC DESCRIPTION.	7pp.
4.	1LB4-4001	PERIPHERAL (82143) IC ELECTRICAL SPECIFICATION.	8pp.

microcode ERS register usage definition

XROM fcns 5/23/78



operand, if any, in reg 9 right justified w/ leading zeroes

	PTR SELECTED	PTR VALUE		ALU MODE	CHIP SELECTED	STATUS SET
input	P	scr	scr	hex	0	0
output (if returning to NFRPU)	DC	DC	DC	DC	⊘	DC

☐ P or active pointer

Q

no peripheral enabled is sufficient

NFRPU on the subroutine stack should return to appropriate NFTC

DC ≡ don't care
SCR ≡ scratch
X ≡ unused

form date 1/18/78

HEWLETT-PACKARD CO. HP 41 CPU

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As Issued	7/14/81	TR

Model No. | Stock No.

Title C.P.U.

Description DETAILED DESCRIPTION | Date 7/14/81

By: TOM REVERE | Sheet No. 1 of 42

Supersedes | Drawing No. A-1LF5-9002-1

9320-3248 (6/73)

HEWLETT-PACKARD CO.

PART NUMBER

1LF5-0301

1LF5-0002

LTR	PC NO	APPROVED	DATE
	REVISIONS		

MODEL	STK NO
DETAILED DESCRIPTION CPU	
BY TOM REVERE	DATE 7/14/81
APPD	SHEET NO 2 OF 42
SUPERSEDES	DWG NO A-1LF5-9002-1

I. GENERAL DESCRIPTION

The 1LE3 CPU is designed for 41C and 11C, 12C calculator. At wafer and package level, their part numbers are designated as follows:

	11C 12C	41C
WAFER	1LF5-01	1LF5-02
PACKAGE	1LF5-0301	1LF5-0002

The difference between the two parts are programmed at metal mask (mask 7, CMOSV). The rest of masks are common to both. Electrically, the differences are in the two circuits:

1) VCI, VCO CIRCUIT

In 41C mode, the VCI and VCO pins are provided to interface with a power supply. When the CPU wishes to wake up, it will pull the VCI line high. It will then wait until VCO is pulled low by the power supply circuitry indicating that VCC has reached the desired level. In 11C and 12C mode, this function is bypassed, however, VCI will still be active.

2) POWER ON CIRCUIT

In 41C mode, a resistor voltage divider is connected across th PWO line so that a lower PWO voltage is provided to the power on circuit. When the battery voltage becomes low, and with the presence of the PHASE 1 CLOCK, the low PWO voltage will cause a hardware shutdown at VCC=4.0 volts.

In 11C and 12C mode, this function is bypassed by disconnecting the voltage divider. The low voltage shutdown hardware circuitry resides in the display chip.

The operating range of the two chips are also different and are summarized as follows:

	VOLTAGE RANGE	CLOCK FREQUENCY RANGE
41C	6.0 to 7.0	340 to 380 KHz
11C 12C	3.0 to 5.0	200 to 230 KHz

Other than the differences described above, both chips are functional identical.

The CPU is a highly intelligent, bit serial, low power, psuedo non-volatile CMOS processor.

All instructions and address communicate via a bit serial, bidirectional ISA line. The ISA is divided into 56 bit words each having 16 bits of address and 10 bits of instruction. This allows a maximum of 64K addressable ROM locations. The address is transmitted from bit time T14 to bit time T29 with the LSB ant T14. Instructions are transmitted at bit time T44 to bit time T53 with LSB at T44. Data may be transferred (to data storage chips, peripheral equipment, display drivers, etc.) via the bidirectional DATA line. Data, in the form of digits, is transferred in bit serial form with 14 digits transferred per word time.

For timing diagram refer to the electrical specifications.

The CPU also controls keyboard scanning, flags in/out and clock generation.

II. INSTRUCTIONS

2.1 The instruction set is divided into 4 categories based on bit patterns of the first two bits of the instruction.

TYPE 0 INSTRUCTIONS

There are 16 groups of instructions in this category. Each group has 16 available instructions. In essence, this category provides 256 instructions for such things as pointers, status bits, data storage manipulations and any other non-branch (or jump) non-arithmetic instructions.

TYPE 1 INSTRUCTIONS

These are two word time JUMP instructions that may jump anywhere within 64K of ROM. During the first word bits 0-7 of the address are transfered, the second word transfers bits 8-15. Decisions to JUMP are based on the state of the carry FF.

TYPE 2 INSTRUCTIONS

This is the arithmetic category with 32 possible instructions. All arithmetic operations are performed on the field defined by TIME ENABLE "TE"

TYPE 3 INSTRUCTIONS

This defines a one word branch instruction which may reach to anywhere within $\pm$64 locations relative to the program counter. Decisions to branch are dependent of the state of the carry FF.

TYPE 00 INSTRUCTIONS

19 18	17 16	15 14 13	12	11 10
MODIFIER		GROUP		0 0

	19	18	17	16	15	14	13	12	MASM MNEMONICS
NOP	0	0	0	0	0	0	0	0	
*RESET STATUS BIT "D"	X	X	X	X	0	0	0	1	SD=0 where D is bit
CLEAR STATUS BITS	1	1	1	1	0	0	0	1	CLR ST
*SET STATUS BIT "D"	X	X	X	X	0	0	1	0	SD=1 where D is bit
RESET KBF	1	1	1	1	0	0	1	0	RST KB
*IF STATUS BIT "D"=1	X	X	X	X	0	0	1	1	?SD=1 where D is bit
IF KBF	1	1	1	1	0	0	1	1	CHK KB
LOAD CONSTANT "N"	N	N	N	N	0	1	0	0	LC
*IF POINTER "P" OR "Q" AT "D"	X	X	X	X	0	1	0	1	?PT=
DECREMENT POINTER	1	1	1	1	0	1	0	1	DEC PT
C→G (P, P+1)	0	0	0	1	0	1	1	0	G=C
G→C (P,P+1)	0	0	1	0	0	1	1	0	C=G
C↔G (P, P+1)	0	0	1	1	0	1	1	0	CG EX
C→M (W)	0	1	0	1	0	1	1	0	M=C
M→C (W)	0	1	1	0	0	1	1	0	C=M
C↔M (W)	0	1	1	1	0	1	1	0	CM EX or MC EX
SB→F (W)	1	0	0	1	0	1	1	0	F=SB
F→SB (W)	1	0	1	0	0	1	1	0	SB=F
SB↔F (W)	1	0	1	1	0	1	1	0	FEXSB
C→SB (DIGITS 0,1)	1	1	0	1	0	1	1	0	ST =C
SB→C (DIGITS 0,1)	1	1	1	0	0	1	1	0	C =ST
C↔SB (DIGITS 0,1)	1	1	1	1	0	1	1	0	CST EX
SET POINTER "P" OR "Q" AT "D"	D	D	D	D	0	1	1	1	PT=D
INCREMENT POINTER	1	1	1	1	0	1	1	1	INC PT
POP JSB	0	0	0	0	1	0	0	0	SPOPND
PWO OFF	0	0	0	1	1	0	0	0	POWOFF
SELECT POINTER "P"	0	0	1	0	1	0	0	0	SEL P
SELECT POINTER "Q"	0	0	1	1	1	0	0	0	SEL Q

				MODEL	STK NO SEE TABLE
				DETAILED DESCRIPTION - CPU	
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TYPE 00 INSTRUCTIONS CONT'D

	19	18	17	16	15	14	13	12	MNEMONICS
IF P = Q	0	1	0	0	1	0	0	0	?P=Q
CLEAR ALL REGISTORS (A,B, & C)	0	1	1	0	1	0	0	0	CLRABC
C→ROM	0	1	1	1	1	0	0	0	GOTOC
KEYS→C	1	0	0	0	1	0	0	0	C = KEYS
SET HEX	1	0	0	1	1	0	0	0	SETHEX
SET DEC	1	0	1	0	1	0	0	0	SETDEC
DISPLAY OFF	1	0	1	1	1	0	0	0	DISOFF
DISPLAY TOGGLE	1	1	0	0	1	0	0	0	DISTOG
RETURN ON "CARRY"	1	1	0	1	1	0	0	0	RTN C
RETURN ON "NO CARRY"	1	1	1	0	1	0	0	0	RTN NC
RETURN	1	1	1	1	1	0	0	0	RTN
PERI [N] (N=Q-15)	N	N	N	N	1	0	0	1	SELPRF
C DATA [N] (N=0 15)	N	N	N	N	1	0	1	0	REG N=C
IF FLAG N = 1 (N=0)→13	N	N	N	N	1	0	1	1	?FN=1
C→N	0	0	0	1	1	1	0	0	N=C
N→C	0	0	1	0	1	1	0	0	C = N
C↔N	0	0	1	1	1	1	0	0	CN EX or NC EX
PUSH C	0	1	0	1	1	1	0	0	STK = C
POP→C	0	1	1	0	1	1	0	0	C = STK
KEY→ROM	1	0	0	0	1	1	0	0	GOKEYS
C ADDRESS	1	0	0	1	1	1	0	0	DADD = C
CLEAR DATA REGISTORS	1	0	1	0	1	1	0	0	
C→DATA	1	0	1	1	1	1	0	0	DATA = C
C→ISA	1	1	0	0	1	1	0	0	CXISA
*C+A C	1	1	0	1	1	1	0	0	C = CORA
*C.A→C	1	1	1	0	1	1	0	0	C = C.A
DATA→C	0	0	0	0	1	1	1	0	C = DATA
DATA [N] C (N=1-15)	N	N	N	N	1	1	1	0	C = REGN
ROTATE "C" RIGHT D DIGITS	D	D	D	D	1	1	1	1	RCRD where D is digit
LLD	0	1	0	1	1	0	0	0	LOW LEVEL DETECT
LDI	0	1	0	0	1	1	0	0	LOAD IMMEDIATE

				MODEL	STK NO SEE TABLE
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	REVISIONS				

1. Use Table 1 to select correct codes for D.
2. POWOFF is a two byte instruction, Byte #2 = ØØØØ.
*3. Cannot be used immediately after an arithmetic (type 2) instruction.

TABLE I

Digit position and N for the pointer and status bits are related as follows; to Set or Test the "P" and "Q" pointers at digit D; use code N to Set, Reset or Test the status bits D; use code N

D	CODE N
0	E - 1 1 1 0
1	C - 1 1 0 0
2	8 - 1 0 0 0
3	0 - 0 0 0 0
4	1 - 0 0 0 1
5	2 - 0 0 1 0
6	5 - 0 1 0 1
7	A - 1 0 1 0
8	4 - 0 1 0 0
9	9 - 1 0 0 1
10	3 - 0 0 1 1
11	6 - 0 1 1 0
12	D - 1 1 0 1
13	B - 1 0 1 1
	F - 1 1 1 1
Illegal	7 - 0 1 1 1

TYPE 10 (2) INSTRUCTIONS
ARITHMATIC INSTRUCTIONS

		19	18	17	16	15	MASM MNEMONICS	14	13	12	TIME ENABLE
		OP CODE				TIME ENABLE		1		0	
0	A	0	0	0	0	0	A=0	0	0	0	on pointer P
0	B	0	0	0	0	1	B=0	0	0	1	exp & sign X
0	C	0	0	0	1	0	C=0	0	1	0	word thru PTR W
A	B	0	0	0	1	1	AB EX or BA EX	0	1	1	whole word W
A	B	0	0	1	0	0	B=A	1	0	0	PTR P thru Q PO
A	C	0	0	1	0	1	ACEX or CA EX	1	0	1	exp sign X
B	C	0	0	1	1	0	C=B	1	1	0	mantissa only M
B	C	0	0	1	1	1	BC EX or CB EX	1	1	1	mantissa sign S
C	A	0	1	0	0	0	A=C				
A +B	A	0	1	0	0	1	A=A+B				
A+C	A	0	1	0	1	0	A=A+C				
A+1	A	0	1	0	1	1	A=A+1				
A-B	A	0	1	1	0	0	A=A-B				
A-1	A	0	1	1	0	1	A=A-1				
A-C	A	0	1	1	1	0	A=A-C				
C+C	C	0	1	1	1	1	C=C+C				
A+C	C	1	0	0	0	0	C=A+C				
C+1	C	1	0	0	0	1	C=C+1				
A-C	C	1	0	0	1	0	C=A-C				
C-1	C	1	0	0	1	1	C=C-1				
0-C	C	1	0	1	0	0	C= -C				
-1-C	C	1	0	1	0	1	C=-C-1				
IF B	0	1	0	1	1	0	? B 0				
IF C	0	1	0	1	1	1	? C 0				

				MODEL	SIK NO SEE TABLE
				DETAILED DESCRIPTION - CPU	
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TYPE 10 (2) INSTRUCTIONS CONT'D

	19	18	17	16	15	MNEMONICS	14 13 12
IF A C	1	1	0	0	0	? A C	
IF A B	1	1	0	0	1	? A B	
IF A 0	1	1	0	1	0	? A 0	
IF A C	1	1	0	1	1	? A C	
SRA	1	1	1	0	0	A SR	
SRB	1	1	1	0	1	B SR	
SRC	1	1	1	1	0	C SR	
SLA	1	1	1	1	1	A SL	

ADDRESSING

The address field (of ISA) is 16 bits long giving a maximum addressable system of 64K words. Return addresses, for BRANCH and JUMP SUB instructions, are stored in a 4 deep by 16 bit wide register STACK which operates on a first in last out principal.

There is a one word relative branch that can reach 64 locations relative to the program counter. There is also a two word absolute JUMP that can reach any place in 64K of ROM. All branches and jumps are conditional and depend on the state of the carry flip-flop. Branches and jumps can be "if carry" or "if no carry".

	19	12	11 10
TYPE 3 BRANCH INSTRUCTIONS	2's compl.	C/NC	1 1

BRN C ADDRESS (branch on carry to address)
One word branch instruction that will cause a branch to +63, -64 locations relative to the program counter if the carry flip flop has been set by an arithmetic or a "compare" instruction.

TYPE 3 BRANCH INSTRUCTIONS CONT'D

If the carry flip flop has not been set, the branch is not taken, and the instruction following the branch is executed. The 2's complement number is added to the address producing the new address. BRN NC ADDRESS (branch on no carry to address)

Same as above except branch is taken if carry flip flop has not been set.

TYPE 1 ADDRESS INSTRUCTIONS

JUMP INSTRUCTIONS

	19	11	10
Bits Ø-7 of 16 bit address		Ø	1
Bits 8-15 of 16 bit address		1	C/NC

JMP C ADDRESS (jump on carry to address)

Two word jump instruction that will cause an absolute jump to anywhere in 64K of ROM if the carry flip flop has been set by an arithmetic or a "compare" instruction. If the carry flip flop has not been set, the jump is not taken and the instruction following the jump is executed. This instruction does not affect the address stack. During execution of the second word sync is suppressed.

JUMP SUB INSTRUCTION

	19	11	1Ø
Bits 0-7 of 1t bit address		Ø	1
Bits 8-15 of 16 bit address		Ø	C/NC

JSB C ADDRESS (jump sub on carry to address)

Two word jump-sub instruction to anywhere in 64K or ROM if the carry flip flop has been set by an arithmetic or a "compare" instruction. If the carry flip flop has not been set, the JSB is not executed and the instruction following the JSB is executed. This instruction will push the program counter onto the return address stack. During execution of the second word sync is suppressed.

JSB NC ADDRESS (jump sub on no carry to ADDRESS)

Same as stated before except JSB is executed if carry flip flop has not been set.

III HARDWARE RESET

The 1LF5 incorporates circuitry to sense when the por input and either the key connecting key column Ø (KCØ) to key row input 3 (KR3) or the key connecting KC4 to KR3 are both active. If these conditions are met the reset flip-flop within the CPU will be set, forcing the PWO output to the active state; the clocks to stop, etc. If the display is off when the reset circuitry is activated, the CPU will, following the reset, wake up with the carry set - i.e. from the deep sleep state, if the display was on when the reset occurred, the CPU will go into deep sleep following the reset. The metal mask for the IC can be easily modified to select KCO.AND.KR4 rather than KCO.AND.KR3, or to remove the reset function.

IV. RETURN INSTRUCTIONS

RETURN (return from sub routine)

When this instruction is executed, the bit return address in the stack drops into the program counter and the program execution begins at that point. Note that a "NOP" at the beginning of a subroutine or a ROM not installed will cause a "RETURN".

RETURN C (return on carry)

This instruction follows an arithmetic or a "compare" instruction. If the carry FF has set, the program returns from subroutine uaing the first 16-bit return address in the stack. Otherwise the return C is skipped and the following instruction is executed.

RETURN NC (return on no carry)

Same as above execept the RETURN is executed if the FF has not been set.

V. ADDITIONAL ADDRESS AND STACK MODIFIERS

KEYS → ROM ADDRESS

The eight-bit key code is used as the address for the next instruction in the current 256 word stack of ROM. The key code gets substituted into the least significant 8-bits of the program counter.

C →ROM ADDRESS

Digits 3 and 4 of the C register are put into the least significant eight bits of program counter.

POP

Subroutine stack is popped once without branching to return address.

PUSH → C

Digits 3, 4, 5, & 6 of Reg. C are pushed onto the subroutine stack. The program counter is incremented as usual.

POP → C

The subroutine stack is popped with the lower address on the stack going into digits 3, 4, 5, & 6 or register C. The program counter is incremented as usual. The other digits of the C-register remain unchanged.

VI. IF INSTRUCTIONS

The IF instruction is a one word test that causes the carry FF to be set, if the test is true, or reset if the test is false. The IF instruction will be followed by a BRANCH, JUMP. JUMP-SUB or a conditional RETURN instruction which follows for branching (or RETURNS) depending on the state of the carry FF.

The instructions are:

IF FLAG N =1

IF POINTER "P" = POINTER "Q"

IF POINTER = N(N=0→13)

IF STATUS BIT N=1 (N=0→13)

IF C≠0

IF B≠0

IF A≠0

IF A≠C

IF A<B

IF A<C

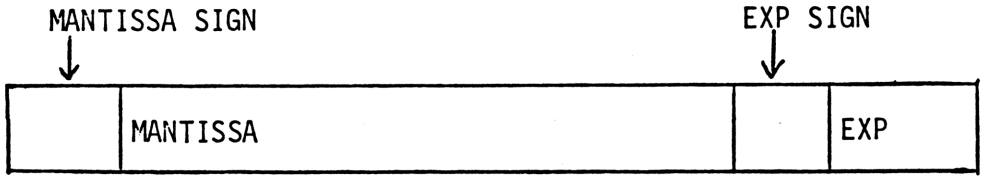
The carry FF, when set by an FF instruction, will remain set for one word time and then be reset. The carry FF is always reset during non-arithmetic instructions.

VII. PROCESSOR REGISTER

The major registers in the CPU are the A, B and C registers which comprise thr working registers.

In addition there two memory registers, M and N.These are 14 digit register that can be copyed into or exchanged with the C register.There is no arithmetic capability with the M and N registers.

The registers are organized into different time enable fields to allow manipulation of different fields within the register.



Digits 0 and 1 are the exponent. Digit 2 is the exponent sign. Digits 3-12 comprise the mantissa. Digit 13 is the mantissa sign.

The following instructions manipulate the five registers on the CPU. These are in addition to the arithmetic instructions.

CLEAR REGISTERS

Clears A, B and C registers. Does not clear M or N.

M/N EXCHANGE C

EXchanges contents of M and N with contents of C. All 14

digits.

M/N → C

Copies contents of M or N into C.

C → M/N

Copies contents of C into M or N.

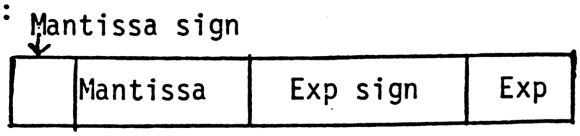
RCR D

Rotate C right the amount the of digits specified by D. Left rotate may be accomplished by specifying D equal to 14 minus the number of left shift.

VIII. ARITHMETIC INSTRUCTIONS

Arithmetic instructions use registers A, B and C as sources and registers A and C as destinations fir the data. In each arithmetic instruction, there is a TIME ENABLE field that specifies the part of the registers (digits) to be operated on. Sums, differences, complements and shifts can be performed on different fields of the registers as defined by TIME ENABLE.

The following are the TIME ENABLE fields:



On pointer	PT
Pointer P thru pointer Q	PQ
Exponent sign only	XS
Exponent and sign	X
Mantissa sign	S
Mantissa only	M

Whole word W

Word through pointer WPT

The 32 arithmetit instructions are:

Ø → A [TE]

The TE field in the A register is reset to zeros.

Ø → B [TE]

The TE field in the B register is reset to zeros.

Ø → C [TE]

The TE field in the C register is reset to zeros.

A ↔ B [TE]

The TE fields are exchanged between the A & B registers.

A ↔ C [TE]

The TE fields are exchanged between the A & C registers.

B ↔ C [TE]

The TE fields are exchanged between the B & C registers.

A → B [TE]

The TE field in register A is loaded into register B.

C → A [TE]

The TE field in register C is loaded into register A.

B → C [TE]

The TE field in register B is loaded into register C.

A + B → A [TE]

Sums the TE fields of A and B and puts result into A.

A + C → A [TE]

Sums the TE fields of A and C and puts result into A.

A + C → C [TE]

Sums the TE fields of A and C and puts result into C.

C + C → C [TE]

Doubles the contents of the TE field in register C.

A + 1 → A [TE]

Increments the TE field of A.

C + 1 → C [TE]

Increments the TE field of C.

A - B → A [TE]

Subtracts the TE field B from A and puts results in A.

A - C → C [TE]

Subtracts the TE field of C from A and puts result in C.

A - C → A [TE]

Subtracts the TE field of C from A and puts results in A.

A - 1 → A [TE]

Decrements the TE field in register A.

C - 1 → C [TE]

Decrements the TE field in register C.

Ø - C → C [TE]

Forms 10's complement in DEC mode (16's in HEXMODE), in TE field of C.

Ø - C - 1 → C [TE]

Forms 9's complement of DEC mode (15's in HEXMODE), in TE field of C.

SLA [TE]

Shift the TE field in register A left by one digit.(0's shifted into end.

SRA [TE]

Shift the TE field in register A right by one digit. (0's shifted into end.

SRB [TE]

Shift the TE field in register B right by one digit. (0's shifted end.

SRC [TE]

Shift the TE field in register C right by one digit. (0's shifted into end.

IX. IF INSTRUCTIONS; (also arithmetic)

The if instructions are followed by a branch, jump or return on carry or a brahch, jump of return on no carry instruction.

The sense of the IF instruction used is decided by which kind of conditional branch, jump or return follows it.

IF B≠0 [TE]

If the TE portion of B is not equal to zero, the carry FF is set.

IFC≠0 [TE]

If the TE portion of C is not equal to zero, the carry FF is set.

IFA≠0 [TE]

If the TE portion of A is not equal to zero, the carry FF is set.

IF A C [TE]

If the TE portion of A is less than C, the carry FF is set.

IF A B [TE]

If the TE portion of A is less than B, the carry FF is set.

IF A≠ C [TE]

If the TE portion of A is not equal to C, the carry FF is set.

X. DECIMAL and HEXADECIMAL MODES

There is a HEXIDECIMAL/DECIMAL flip flop which determines the mode of arithmetic operations. Two instructions set the FF to its two states.

DECIMAL-Sets the FF enable decimal calculations.

HEXADECIMAL-Sets the FF to enable hexadecimal calculations. The carry (borrow) bit is associated with the TE field operated on by the arithmetic instruction. A carry is generated if the most significant digit of the TE field goes from 9 to Ø in the DECIMAL mode of from 15 to Ø in the HEXADECIMAL mode after an addition. A borrow is generated if the most significant digit in the TE field goes from Ø to 9 in the DECIMAL mode or from Ø to 15 in the HEXADECIMAL mode after a subtraction.

NOTE: If a register transfer, shift, rotate, "and" or "or" instruction is made in the decimal mode, the CPU operates in HEXADECIMAL mode long enough to make the transfer and then shifts back to DECIMAL.In this manner, non BCD digits are not destroyed during a register transfer.

XI. Other instructions

AND

Register A is "ANDED" to C with the result in register C. This instruction operates on the whole word.

OR

Register A is "ORED"to register C with the result in register C. This instruction operates the whole word.

CXISA (C exchange ISA)

This is a two word time instruction that provides for reading ROM instructions and for pitting them into the "C" register.

During the first word after CXISA is issued the ROM address residing in digits 3, 4, 5 and 6 of the C register is output; the instruction at its referenced ROM location is now read back.Note that SYNC is suppressed during this word time.

During the second word time the instruction is loaded into digits Ø, 1 and 2 of the register C.

XII. KEYBOARD

The key code matrix consists of 7 column lines and 9 row lines. The columns are scanned one at a time from digit time Ø to digit time 6. when a key is pressed the keyboard flag is set and the 4 bit row and column codes are stored in the keyboard buffer. When this code is called for, by a KEYS→ROM or KEYS→C the codes are sent out at digit times 3(row) and 4 column. For codes use Table 1.

Keyboard instructions:

CHK KB

Checks to see if the keyboard FLAG is set; if so, the carry FF is set. If the keyboard FLAG has been reset, then this instruction must be given before the FLAG can be set by a new closure.

RST KB

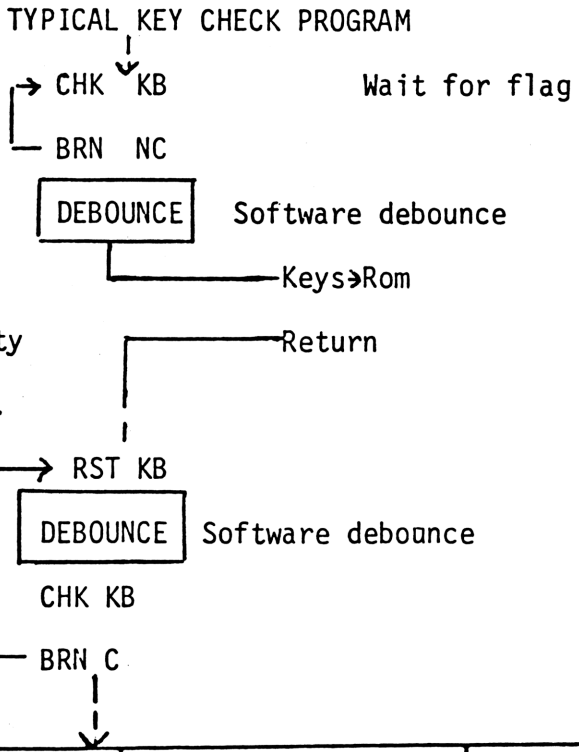
Resets the keyboard FLAG if the key has been released. If the key is still down at the time this instruction is issued, the bit cannot be reset.

KEYS→C

The keyboard buffer is loaded into digits 3 & 4 of the C register.

KEYS→ROM

The keyboard buffer is loaded into the least significant bits of the program counter.



NOTE: This program provides the capability of a two key rollover.

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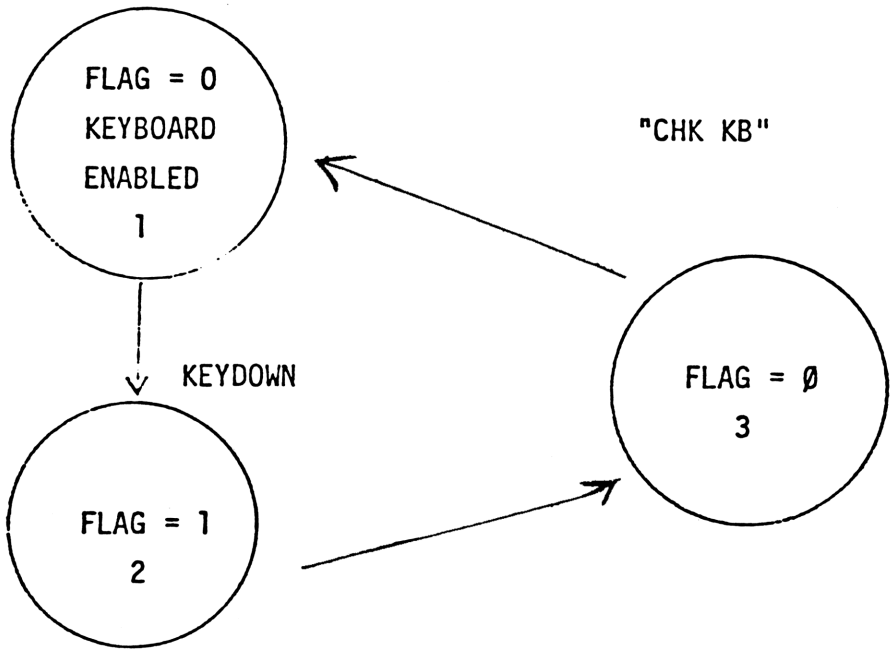
C REG DIGIT⟶	4	3
TIME	COLUMN	ROW
D0	KC0 0001	KRØ 0000
D1	KC1 0011	KR1 0001
D2	KC2 0111	KR2 0010
D3	KC3 1000	KR3 0011
D4	KC4 1100	KR4 0100
D5	KC5 1110	KR5 0101
D6	KC6 1111	KR6 0110
		KR7 0111
		POR 1000

When a key is depressed the row and column line are stored in the keyboard buffer and the key flag is set.

KEYBOARD CODES

TABLE 1

KEYBOARD SCANNER
STATE DIAGRAM



("RST KB") AND (KEY CODE KEY NOT DOWN) AND
(TWO KEYS ON SAME COLUMN ARE DOWN)

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XIII. POINTER OPERATIONS

The processor has two pointers (P and Q), each of which can be shifted, initialized and tested. A pointer select is used that determines which of the two pointers will be operated on the pointer operations. once a pointer is selected all operations will be on that pointer until the other pointer is selected.

The following instructions are used for pointer operations:

SELECT POINTER P

After giving this command, all pointer operations will be on pointer P until pointer Q is selected.

SELECT POINTER Q

After giving this command, all pointer operations will be on pointer Q until pointer P is selected.

LOAD CONSTANT N

Loads a constant character (N) into the pointer position of the C register. The pointer is decremented by one position.

IF POINTER "P" OR "Q"=N (If pointer at N)

A conditional branch instruction follows this instruction. The carry FF is set if the selected pointer is positioned at digit N. (N=Ø 13) The pointer used is the pointer that was last selected.

IF P+Q (If pointer P = pointer Q)

A conditional branch, jump or return follows this instruction.If pointer P is equal to pointer Q set the carry FF.

PT=N

Sets selected pointer to N (N=Ø-13), uses last pointer selected.

DEC PT

Decrements pointer, if at digit Ø the pointer will wrap around to digit 13. Use last pointer selected.

INC PT

Increments pointer, if at digit 13 the pointer will wrap around to digit Ø. Uses last pointer selected.

XIV. USE OF POINTERS FOR TIME ENABLE

The pointer time enable field is pointer P→ pointer Q.

POINTER P THROUGH POINTER Q

(A) If pointer Q is to the left of pointer P, then time enable is from pointer P through pointer Q with the carry out being fron pointer Q position.

(B) If pointer P is to the left of pointer Q, then the time enable is between pointer P and the left end of the register; (digit 13) with the carry out from the left end of the register.

(C) If pointers are at the same position, pointer operation is on that digit.

ON POINTER

All operations are performed on digit position indicated by pointer.

WORD THRU POINTER

The time enable is from the beginning of word thru the selected pointer with the carry out from the pointer position.

XV. STATUS BITS

There is a 14 bit status register that privides 14 bits for the programmer to store additional information.

Bits Ø through 7 can be transferred to or from digits Ø and 1 of the C-register or the output flag register.

The following instructions will test and manipulate the status bits:

SET STATUS N

Causes status bit N to be set to "1".

RESET STATUS N

Causes status bit N to be reset to"Ø."

CLEAR STATUS

Clears 8 of the 14 status bits. (Bits Ø-7).

IF SB N =1 (If status bit N to 1)

A conditional branch, jump or return instruction follows this instruction. The carry FF is set if status bit N is set or equal to 1. (N Ø→13)

C↔ Status

Status bits Ø-7 are exchanged with the C regieter at digits 0,1.

C → STATUS

Digits Ø and 1 of the C register is transferred into status bits Ø-7 of the status register.

STATUS → C

Status bits Ø-7 are moved into digits Ø and 1, of the C register.

XVI. G - REGISTER

There is an 8 bit G-register that communicates with the C-register. Instructions are as follows:

G→C

G is copies into the current pointer and pointer + 1 locations in the C-register.

C→G

The current pointer and pointer + locations of the C-register are copied into the G-register.

C↔G

The current pointer and pointer +1 locations of the C-register are exchanged with the G-register.

NOTE:

If the selecter pointer is positioned at digit 13, then C register digits Ø and 13 will be used.

XVII. DATA STORAGE

The following instructions operate on the data storage registers;

CLEAR DATA REGISTERS

Clears all 16 data storage registers on selected chip. Some chips ignore this instruction, i.e. Sleeper chip.

C→DATA ADDRESS

Digit Ø in C-register is used to select a specific data register and digit 1 is used to select a register chip if more than one is used in the system. The register remains selected until unselected by a REGN→C or C→REGN or another C→DATA ADDRESS instruction.

C→DATA

The contents of register C are loaded into the data register on the selected chip selected by the previous REGN→C, C→REGN, or C→DATA ADDRESS instruction.

DATA→C

The contents of the data register on the selected chip selected by the previous REGN→C, C→REGN or DATA ADDRESS instruction gets loaded into register C.

REGN→C

The contents of data register N on the selected chip are loaded into C. N can be from 1→15.

C→REGN

The contents of register C are loaded into data register N on the selected chip. N can be from Ø → 15.

NOTE:

All of these instructions are at least partially implemented in the data storage chip used, and are therefore subject to change or other uses without affecting the NUT CPU chip.

XVIII. INPUTS, OUTPUTS AND PERIPHERALS

The NUT CPU has capability for seventeen flag inputs and eight flag outputs to allow increased interfacing to switches, lamp drivers, etc.

In addition, there is a PWO output that tells the other chips to wakeup or go to sleep.

There is also capability to turn over control to 16 different 'smart' peripherals.

FLAG INPUT

There is a single Flag Input line whose state during each of the 14 digit times represent one of the 14 Input Flags. This line is tested during the "IF FLAG N" instruction and result is true, if the FI line is LOW during and Ø1 clock of the digit time N. The flags are not stored by the hardware. The flag in line is pulled high by the CPU when open.

A flag input can be realized by making connection between one or more of the seven column lines of the keyboard scanner (KC0-KC6) and the FLGIN (FI) port, or with a switch, a transmission gate or a negative pulse at the appropriate digit time between digits 0-13. The input flags are

not stored and cannot be reset from the CPU. The flag resets as soon as the input stimulus ceases. The true states of the KC0-6 lines and F1 input port are "0:"or low. During PWOF KCØ-6 are all in the low state.

FLAG OUTPUTS

A Flag output can be realized by controlling a transister driver, transmission gate, etc. between one or more of the seven column lines of the keyboard scanner KCØ-KC6 and the FLGOUT (FO) Port.

The peripheral being driven has to look for the output flag during the time the appropriate column line is being scanned. If all flags are either high or low the flag output line will be either high or low for the entire word time.

XIX INSTRUCTIONS

FOXSB

Exchange flag out register with bits 0-7 or status register.

FO→SB

Copy flag out register into bits 0-7 of status register.

SB→FO

Copy bits 0-7 of status register into flag out register.

PWO OUTPUT

The PWO output is a control to tell the chips in the system to power on or off. When PWO is high, the chips connected to the PWO line are on.

When PWO is low, the external chips are off, the CPU clocks turn off and Sync pulses stop. (If in the FFLY MODE then a one bit pulse will be output at every T55 time on the Sync line, if in the NUT mode the Sync output will equal the DPWO Input. If the PWO line is forced low during any Ø pulse the chip will immediately power off, all clocks will stop, and the timing circuits will reset to their off status. This feature is provided to allow a hardware shut down.

PWO LINE:

PWOF (Power Off)

The end of the next T53 time after this instruction marks the time when PWO goes low and turns off the external chips, as well as the greater portion of the CPU. The keyboard lines (KCØ-KC6) all go to their true state. NOTE: That the clocks stop at T55 time. Refer to Fig. 2.

PWOF is a two byte instruction the second byte is sync will be present during the second byte.

DPWO INPUT

Holding this line high allows the processor to wake up (assumes a PWOF was previously issued) in response to any key closure of the pulling of ISA line high.

If DPWO is low (and the CPU has received a PWOF instruction) the only way to start operation again is to bring POR input low,

or ISA high; this will cause PWO to go high at the next T54 time. Note the clocks start at T52. Refer to Fig. 2.

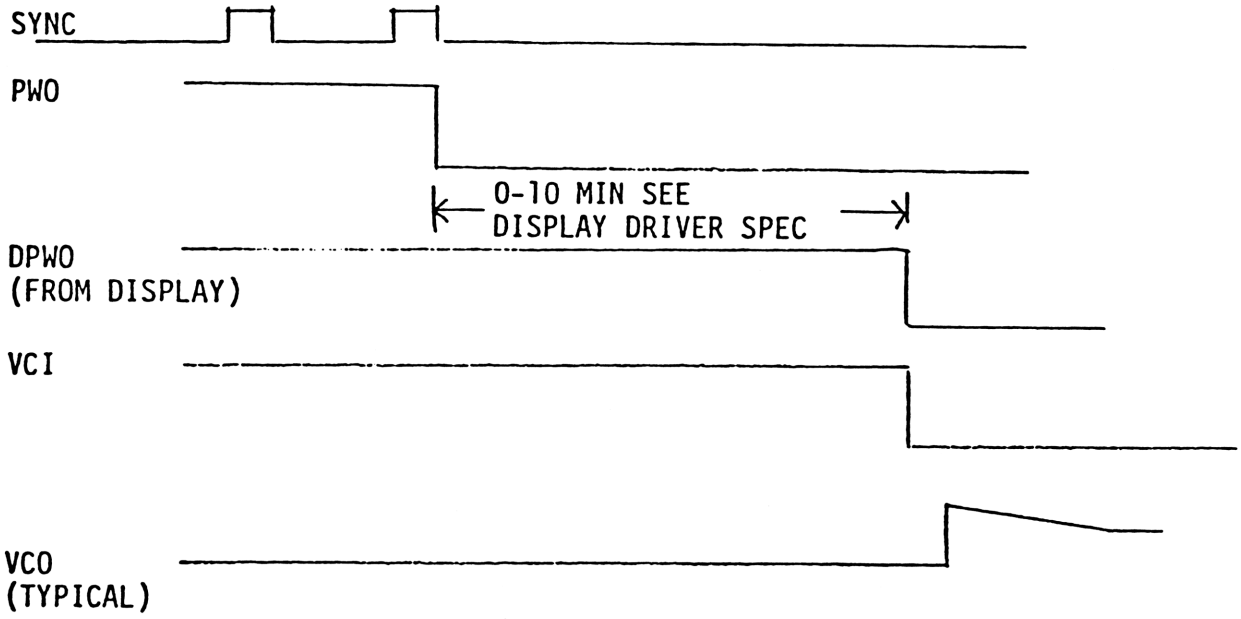
If the DPWO line goes low at any time, then the carry FF will be set during the next work time.

POR INPUT

If the POR input goes low (when the CPU has previously powered down) the CPU wakes up, setting the PWO line high at the next T54 time and waking up the other chips. The system powers up at ROM location ØØØ and does a wake routine. (Operation is the same for DPWO low). Note that the clock start at T52 time.

The POR input is also a key row line with row code =1ØØØ.

NUT POWER OFF



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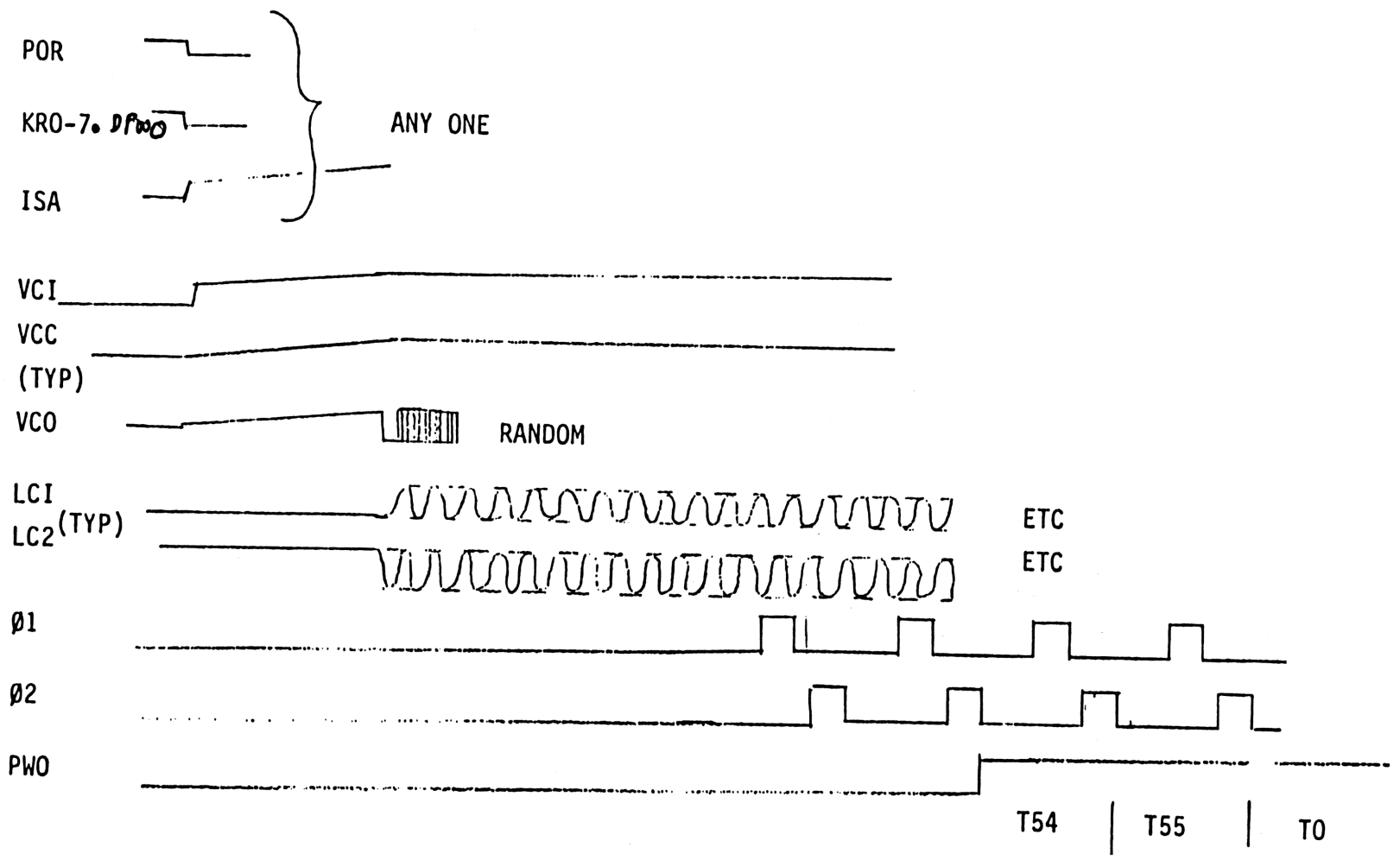
WAKE UP "NUT" MODE TEST LO



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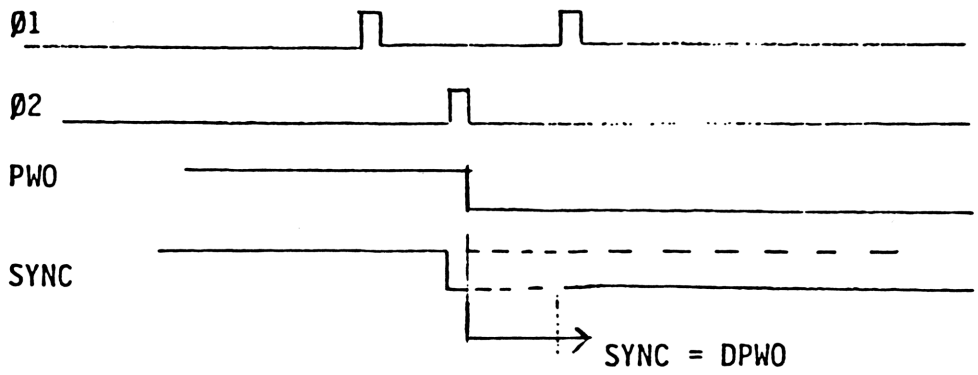
		REVISIONS							
ITR	P.C. NO								

8220-2788 (FORMERLY 0-70020)

HARDWARE SHUT DOWN TIMING



The states of Sync and VCI after shut down are dependent on the DPWO Input level.

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POWER OFF SEQUENCE

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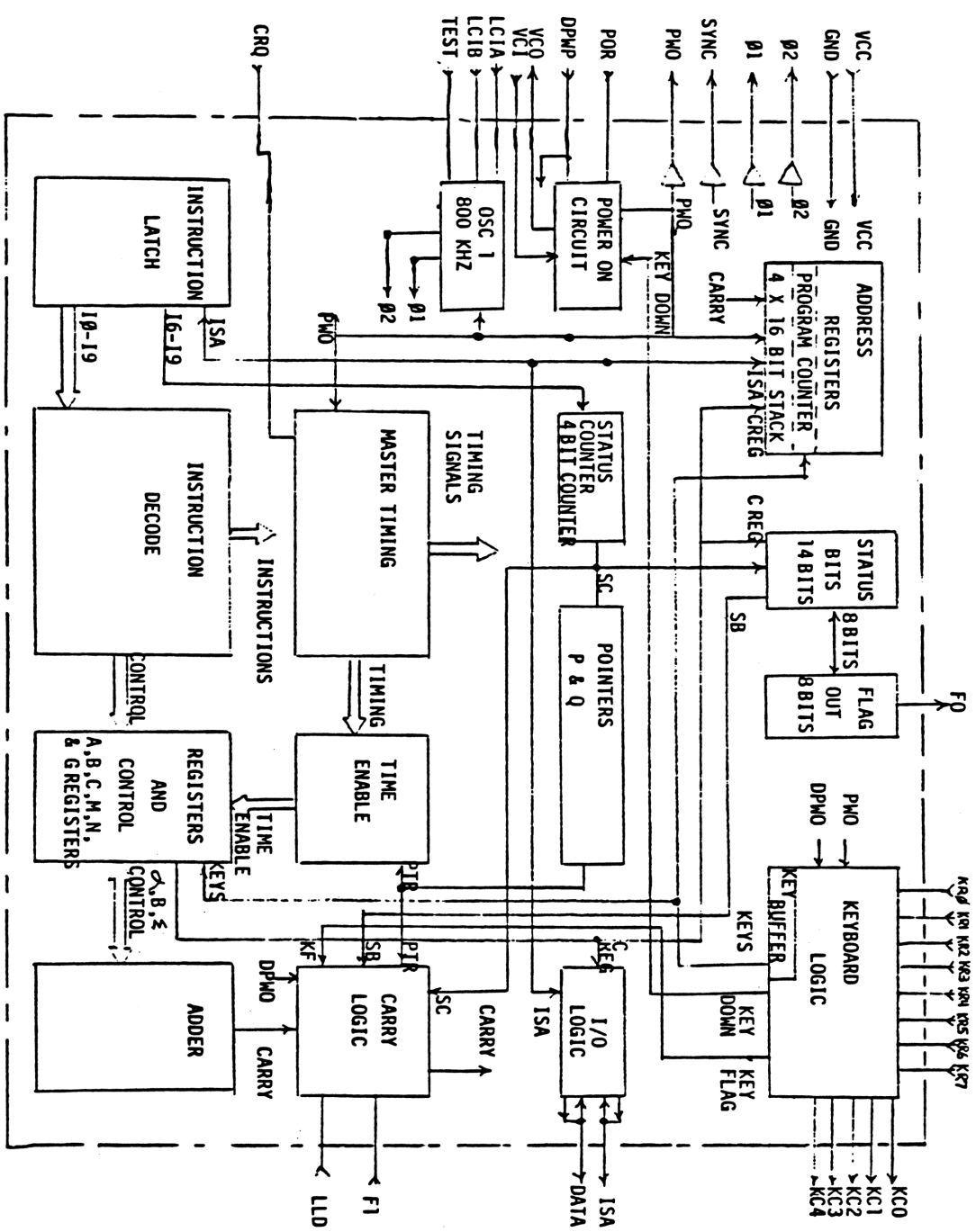
9320-2788 (FORMERLY D-700024)



				MODEL	STK. NO.
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	REVISIONS				

VCI

VCO

The VCI and VCO PINS are provided to interface with a power supply. When the CPU wishes to wake up it will pull the VCI line HIGH. When in NUT MODE the wake up will then wait until VCO is pulled LOW by the power supply circuitry indicating that VCC has reached the desired level. In FFLY mode this function is bypassed, however, VCI will still be active.

XX. MANAGEMENT OF SMART PERIPHERALS

A smart peripheral will be a chip with a board processing capability. This chip may look like more ROM to the CPU, and it may be given control with a subroutine call from the CPU. The subroutine may consist of instructions, but will also have a PERI (N) instruction which caused the SYNC pulses to cease and the CPU to ignore further instructions. The selected peripheral (N) will decode further instructions as well as manipulate data for further operations. Note the contents of the "C" register is continuously output on the data line except during a DATA C instruction.

Control may be returned to the CPU with any instruction that has BIT Ø=1 which will reinstate the SYNC pulse at the next work time.

PERIPHERAL INSTRUCTIONS:

19	18	17	16	15	14	13	12	11	10
N	N	N	N	I	0	0	I	0	0

PERI N (N=0-15)

Selects peripheral (N) for control, manipulation and/or processing of data.

IF PFLAGN=1 If peripheral flag N=1 (N=Ø-15)

19	18	17	16	15	14	13	12	11	10
N	N	N	N	0	0	0	0	1	1

Each peripheral may have up to 16 flags that can be tested and multiplexed onto the ISA line at time T0. The CPU test this flag and sets the carry FF accordingly. This instruction returns control to the CPU.

LOAD CHARACTER

19	11	10
8 Bit Character	Ø	X

This instruction is used to transmit 8 bit characters (such as ASCII) to the selected peripheral.

If 10=1 control is returned to the CPU.

DATA (Np)C

19	16	15	14	13	12	11	1Ø
N		1	1	1	0	1	0

The data line is read into the C register. N may be used to select a register on the peripheral, or any other data storage chip.

If 1Ø=1 control is returned to the CPU.

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XXI. TEST FACILITIES

There is a "Test input provided on the CPU that provides two functions:

(A) If "Test" is driven high when POR is low, then an external clock can drive the CPU through the LC inputs.

(B) If "Test" is driven high when POR is driven high/low all output pins are put in tri-state mode. This allows a test CPU to be put in parallel with the tested CPU without opening lines.

HP 41 DISPLAY DRIVER

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As issued	11/20/78	HK / [illegible]

Tel No.		Stock No.	1LA4-4001
Title	DETAILED DESCRIPTION		
Description	Display Driver	Date	11-20-78
By	Hank Koerner	Sheet No.	1 of 23
Supersedes	Norm Johnson 6-5-79	Drawing No.	A-1LA4-4001-2

I. GENERAL DESCRIPTION

This integrated circuit is an LSI CMOS LCD driver. It will drive six digits of display, each consisting of a 3 x 6 matrix of segments (see figure 1). Thirty-nine of its 57 pads are outputs for display driving. It is designed to interface directly with the HP-41C processor. It may be daisy chained to configure any length display, although the HP-41C is defined with a 12 character, 2 chip display system.

Broken into blocks (see figure 2), the display driver consists of control and timing, instruction decode, internal registers, a character decode ROM, display timing, and display outputs. Ø1, Ø2, SYNC, and PWO provide clocks and synchronization. Instructions are issued from ROM on the ISA line, and data to and from the registers is transferred via the DATA, DATA IN and DATA OUT lines. There are four internal registers; the A and B registers are organized in a 6 x 4 bit array, the C and E registers in a 6 x 1 array. The flip-flops making up the registers are pseudo non-volatile cells which allow retention of data when clocks are stopped. The character ROM is addressed by seven bits which originate from data stored in the registers. The ROM outputs segment information which is stored in three bit recirculating latches connected to the column drivers. Display timing is initialized by power on and instruction sequences and produces the appropriate drive waveforms which, when gated with all possible segment data, create the HP-41C character set (see figure 3). Annunciators are controlled independently of the other display characters. Note that this circuit is designed expressly to drive the HP-41C display; to make use of its annunciator and punctuation control, a non HP-41C display must be laid out correctly.

An internal oscillator circuit, which requires an external capacitor allows display while the rest of the system is dormant. The oscillator, in conjunction with internal status and a mask programmable delay, controls the state of the DPWO line which is used in controlling the system power modes. Two features included on the chip but not used by the HP-41C system

are a voltage divider to derive the drive voltages for the LCD and a temperature compensation circuit that adjusts the duty cycle through pulse width modulation of display outputs and which requires three external components.

II. SIGNALS

2.1 Ø1 and Ø2 are non-overlapping, positive clock inputs. See the electrical specification for timing requirements. At 6 volts, this IC will operate typically from 400 KHz to 10 KHz.

2.2 PWO - The rising edge and high state of PWO initializes the master timing and enables the internal clocks, respectively, thus synchronizing the display driver with the rest of the system. The leading edge must occur during T54 before Ø1 but after Ø2. See figure 4a. The low state of PWO resets the master timing and gates off the internal clocks. If internal status is appropriate, it turns on the "light sleep" oscillator. The falling edge of PWO may occur asynchronously as long as it occurs a minimum of two word times after the last display instruction.

2.3 SYNC is a 10 bit positive pulse expected from the rising edge of T44 to the falling edge of T53. See Figure 4a. Sync gates the ISA line and its absence causes a NOP to be decoded. This signal is used by the HP-41C chip set to discriminate a one byte instruction from a two byte instruction in which the second byte is additional bits of address needed to complete a long jump.

2.4 DATA is a bidirectional system line over which the majority of data transfer takes place. In the HP-41C system, the CPU drives the data line by outputting its C-register at all times except

those word times when a type $XX70_8$ instruction is in effect. During $XX70_8$ instructions some enabled device—a data storage chip (Ram) display driver, card reader chip, etc.—will take control of the data line and output data appropriate to the $XX70_8$ instruction issued. This data is written into the CPU's C-register.

On the display driver, DATA is connected to the system data line and is used to input its peripheral address (see figure 4b) and to compare against two other lines—DATA IN and DATA OUT—to determine its position in a string of display drivers. On the display driver, DATA has no output capability.

2.5 DATA IN and DATA OUT are bidirectional lines that the display driver uses to transmit and receive data. The display driver responds to 37 instructions, 33 of which cause the input or output of data. This data is either buffered in or read from the internal registers. The 33 read/write instruction specify the direction of information flow which determines DATA IN and DATA OUT as input or output pins. The internal registers have DATA IN connected to their left end and DATA OUT to their right. Left shifted reads and writes occur with DATA IN operating as an output and DATA OUT operating as an input. Right shifted reads and writes cause DATA OUT to be an output and DATA IN to be an input.

Display drivers are cascadable as one would cascade shift registers. The normal convention is to connect DATA OUT of the preceeding stage to DATA IN of the succeeding stage. The left-most chip has its DATA IN connected to the DATA OUT of the right-most chip which are both connected to DATA. Figure 5 shows three possible configurations. Besides establishing the necessary data link, interconnection of DATA to DATA IN/OUT sets internal status which controls output onto the system DATA line and enables the internal oscillator.

"I am first" (IAF) is high when DATA and DATA IN are connected together; "I am last" (IAL) is high when DATA and DATA OUT are connected together. The start up (PWO) sequence presets IAF and IAL high; any exclusive or condition on the respective pairs of lines clears the status bits low. The compare is synchronous and inhibited upon reception of the first read instruction. IAF high, with appropriate time out status, enables the internal oscillator. Note, for proper operation, some non-zero data should be placed on DATA. Otherwise, in multichip systems IAL and IAF may not clear correctly which would cause incorrect operation of the internal oscillator and loss of row synchronization.

2.6 ISA—The display driver reads 10 bits serially, least significant bit first, from the ISA line during SYNC time. The display driver responds to 37 instructions:

2.6.1 DISPLAY OFF (1340_8)—This instruction resets the display status flip-flop to zero. With DSTAT zero, all display outputs are driven to ground, a non-destructive DC off condition for the LCD. If DSTAT is set to one, then all rows and columns free run with the appropriate 4 voltage waveforms (V3V, V2V, V1V and GND).

2.6.2 DISPLAY TOGGLE (1440_8)—DTOG toggles DSTAT: If DSTAT is high, DTOG will toggle it low; if DSTAT is low DTOG will toggle it high.

2.6.3 COMPENSATION INSTRUCTION (1774_8)—CI prompts the temperature compensation circuitry to begin a compensation cycle. With no external components present CI will reinitialize the duty cycle to 100%. If TC1 and TC2 are connected for internal compensation then CI should be issued after each block of display instructions and should not be

followed by a display instruction for at least 24 word times. This instruction is not tested or guaranteed.

2.6.4 C→PFAD (1760_8)—PFAD causes the display driver to gate in the first 2 digits appearing on DATA immediately following the issuance of the instruction (see figure 4b). It treats these 8 bits as chip address, least significant bit first. If the correct address is issued at this time (FD_{16}) the chip enabled flip-flop is set high, otherwise CE is set low. All except the above instructions are disabled when CE is low.

2.6.5 WRITE ANNUNCIATORS (1360_8)—WA causes the first 12 bits, bit time 0 through bit time 11, appearing on DATA IN to be right shifted through the E-register and output by DATA OUT if IAL is low, and into the bit bucket if IAL is high (see figure 4c). There are 6 bits in the E-register, each corresponding to an annunciator segment on the display. Storing ones in the E-register causes the annunciators to be activated.

2.6.6 READ ANNUNCIATORS (570_8)—During the same window as WA, RA causes information stored in the E-register to be right shifted, output by DATA OUT irregardless if IAL, and to input data appearing at DATA IN. Besides driving DATA OUT independently of IAL, RA differs from WA in the way the HP-41C CPU interprets the instruction. The CPU tri-states its data line and buffers whatever it sees on data in its C-register. When connected in one or two chip configurations (see figure 5), RA performs a non-destructive read of the E-register.

2.6.7 The other 31 read/write instructions address the registers and transfer data to them in a number of different modes. Right shifted operations cause data flow from DATA IN to DATA OUT; left shifted operations are the reverse of right shifted instructions. During writes, $XX50_8$ instructions, the output pin will be driven if the corresponding status (IAF for DATA IN, IAL for DATA OUT) is low, otherwise the output is tri-stated. During reads, $XX70_8$ instructions (excluding 570_8), the output pin is driven irregardless of status and the chip assumes that any other devices connected to the outputs are tri-stated.

There are four fields during which transfers occur: 4 bit (1 Hexidecimal digit), 8 bits (2 digits), 12 bits (3 digits), 48 bits (12 digits). See figure 4c. Each of the fields begins at the rising edge of the valid word time. All 4 bit transfers operate on one register. All eight bit transfers operate on the A- and B- registers only. All twelve bit transfers operate on A-, B-, and C-. 48 bit transfers may operate on a single register, on A- and B-, or on A-, B-, and C-. Operations involving all three repeat the A-, B-, C- sequence gating digits to each register as many times as the field permits (as with all transfer instructions). A- and B- can each buffer 6 hexidecimal digits of data, every digit corresponding to a character position which it is displaying. C- has capacity for only six bits; each digit written to C- has the first bit buffered and the other three ignored. When read, C- outputs a bit into the least significant of the appropriate digit. The other three bits are meaningless.

Lumping the A-, B-, and C-registers together, a 6 x 9 bit organization can be assumed. The 6 corresponds to the 6 character positions. Seven of the 9 bits are used to provide ASCII form addresses which are input to the character Rom. The remaining 2 bits comprise the punctuation field; the four punctuations yield no punctuation (00), decimal point period (01), colon (10) and comma (11). See figure 3 for the character set and figure 6 for the data structure. The seven bits are stored in the 4 bits of A-, the 2 least significant bits of B-, and the one bit of C-. C- is the most significant bit of the address, the least significant bit of A- is the least significant bit of the address. The 3 registers are independently addressable so that when a numerical display is desired, a mask may be set up and the entire display can be changed with one instruction. When displaying alpha, several instructions may be required to update the entire display.

2.7 The WRITE INSTRUCTIONS are:

SRLAD	0050_8	Store right long (48 bits) in display register A.
SRLDB	0150_8	Store right long in display register B.
SRLDC	0250_8	Store right long in display register C.
SRLDAB	0350_8	Store right long in display registers A and B.
SRLDABC	0450_8	Store right long in display registers A, B, and C.
SLLDAB	0550_8	Store left long in display registers A and B.
SLLDABC	0650_8	Store left long in display registers A, B, and C.

SRSDA	0750_8	Store right short (4 bits) in display register A.
SRSOB	1050_8	Store right short in display register B.
SRSDC	1150_8	Store right short in display register C.
SLSDA	1250_8	Store left short in display register A.
SLSDB	1350_8	Store left short in display register B.
SRSDAB	1450_8	Store right short (8 bits) in display registers A and B.
SDSDAB	1550_8	Store left short in display registers A and B.
SRSDABC	1650_8	Store right short (12 bits) in display registers A, B, and C.
SLSDABL	1750_8	Store left short in display registers A, B, and C.

2.8 The READ INSTRUCTIONS are:

FLLDA	0070_8	Fetch left long (48 bits) from display register A.
FLLDB	0170_8	Fetch left long from display register B.
FLLDC	0270_8	Fetch left long from display register C.
FLLDAB	0370_8	Fetch left long from display registers A and B.
FLLDABC	0470_8	Fetch left long from display registers A, B, and C.
FLSDC	0670_8	Fetch left short (4 bits) from display register C.
FRSDA	0770_8	Fetch right short from display register A.
FRSDB	1070_8	Fetch right short from display register B.
FRSDC	1170_8	Fetch right short from display register C.

FLSDA	1270_8	Fetch left short from display register A.
FLSDB	1370_8	Fetch left short from display register B.
FRSDAB	1470_8	Fetch right short (8 bits) from display registers A and B.
FLSDAB	1570_8	Fetch left short from display registers A and B.
FRSDABC	1670_8	Fetch right short (12 bits) from display registers A, B, and C.
FLDABC	1770_8	Fetch left short from display registers A, B, and C.

2.9 DPWO is a display driver output which when combined with PWO, determines the HP-41C system power modes. The three modes are:

PWO	DPWO	POWER MODE
0	0	System dormant.
0	1	System clocks off; system receptive to wake up. Display on.
1	0	Illegal state.
1	1	System running.

DPWO itself is described by the following truth table:

PWO	CE	DSTAT	TOUT	DPWO
0	0	X	X	1
0	1	0	X	0
0	1	1	0	1
0	1	1	1	0
1	X	X	X	1

2.9 CE = Chip enabled flip-flop
DSTAT = Display status flip-flop
TOUT = Time out flip-flop, output of a mask programmable delay.

DPWO is provided so that an HP-41C system calculator may save energy. This is accomplished by turning off high power clocks when an operation is complete and assuming a standby mode in which the display supplies its own clock throughout the delay period. When the display times out, it stops its onboard oscillator, grounds the display outputs and notifies the rest of the system by dropping DPWO. The mask programmable delay is presently set to approximately 11 minutes. The delay is calculated by the formula Delay = 9 x 2^{16+n} x internal oscillator period, where n= 0, 1, 2, 3 (presently n = 3). The rising edge of DPWO is coincident with PWO.

2.10 OS1 and OS2. These two pins are input and output for the internal oscillator. OS1 is the input and should be connected to a capacitor to ground. The frequency varies proportionally to the value of the capacitor. OS2 is a tristate output which during standby mode also serves as the clock input to counters controlling the display timing. The oscillator is enabled only when PWO is low, DPWO and IAF are high. Otherwise OS1 is high and OS2 is tristated. In the HP-41C system, OS1 of the first chip is connected to a capacitor; OS2 of both chips are tied together.

2.11 TC1 and TC2 are inputs to temperature compensation circuitry. In multi-chip system, only the chip doing the compensation needs its TC1 connected; however, all TC2's must be connected together. Components required for the temperature compensation are a trimmer resistor, a thermistor, and a capacitor to ground. See figure 7. Note this circuitry is not tested and not guaranteed to be functional.

Compensation is accomplished through pulse width modulation of the display outputs. The RC time constant of the compensation network is inversely proportional to temperature as are the drive requirements of the LCD.

A compensation instruction (CI) initiates a compensation cycle. The RC network is allowed to charge up. When the voltage on TC2 passes an N-channel threshold, a compensation counter is reset, thus providing an endpoint to the pulse width. At 25°C, the compensation network should be adjusted to give just 100% duty cycle. When no components are present, a CI will cause 100% duty cycle. Every time a read or write instruction is issued, the duty cycle is reset to 100%. Compensation instructions should not be issued with fewer than 24 word times between cycles so that the circuitry will be in a known state.

2.12 V_{CC} and GND provide power for the display driver.

2.13 V3V, V2V, and V1V are the voltage levels, in addition to ground, required by the LCD drive scheme.

2.14 ROW 0, ROW 1, and ROW 2 are the row outputs from the display driver. The row outputs are connected to the backplane of the display and their waveforms are constant irregardless of the desired segment pattern. In a multi-chip display, the rows are synchronized, which permits bussing the three rows together (in general, bussing is required because individual row outputs were not designed to drive the loads of large displays).

The LCD is driven by a one-third multiplexed, four level scheme that maximizes the on-to-off RMS voltage ratio which in turn maximizes the contrast ratio of the LCD. See figure 8.

When the display driver is turned off, either through software control or time out, all display outputs are grounded. Read/write instructions initiate a display update which occurs the word immediately following the issuance of the instruction. During the update, all display outputs are grounded. The update lasts 30 bit times and at its finish the rows start up. The rows and columns derive their timing from an internally generated SYNC while the system is running and from the internal oscillator while the system is timing out. One frame (half period) of a row waveform lasts 72 periods (mask programmable to 36) of the input signal.

The HP-41C LCD is a twisted-nematic, field-effect device. Attached to the front glass plate is a polarizer; a polarizer and reflector are attached to the back plate. The directions of polarization are perpendicular. Translucent indium oxide conductors are placed on the front (columns) and back (rows) planes. With no electric field applied across the liquid crystal, a 90° shift in polarization is imparted to the light passing through it. Thus, light will pass through the display and be reflected back with little loss. Applying an electric field greater than the threshold (ideally V_{th} = V1V) of the LCD causes, roughly speaking, the molecules to orient themselves in parallel with the field, and light passing between the polarizers is absorbed. This appears as a dark region on a light background.

The contrast of the LCD is proportional to the RMS voltage driving it. A four level drive produces a higher RMS voltage than does a three level drive for the same duty cycle.

2.15 C_{00} - C_{55}. There are 36 column outputs; 6 columns per character times 6 characters per chip. Each column is identified by 2

numbers; the first denotes its character position, the second its column position within the character. For example, C45 refers to the sixth column of the fifth character. A column waveform is determined by the segment pattern. The character "H" has one of column 0's segments on, two of column 1's segments on, zero of column 2's segments on, etc. See figure 8. During a frame an on column will be driven to the on voltage, V3V or V0V, that the corresponding row is not to achieve the greatest differential voltage. The same is true for an off column except the driving voltages are V2V and V1V. See figure 8. Columns Cx5 are dedicated to displaying punctuation on the HP-41C display. Columns Cx4 have the third segment dedicated to displaying annunciators.

III IDIOSYNCRACIES

3.1 When clocks are shut off, display counters are reset but segment patterns are left unchanged. It is unlikely that the segment patterns will be synced up with the counters. To refresh the correct synchronization, merely rotate the display 1 character right and then 1 character left after start up.

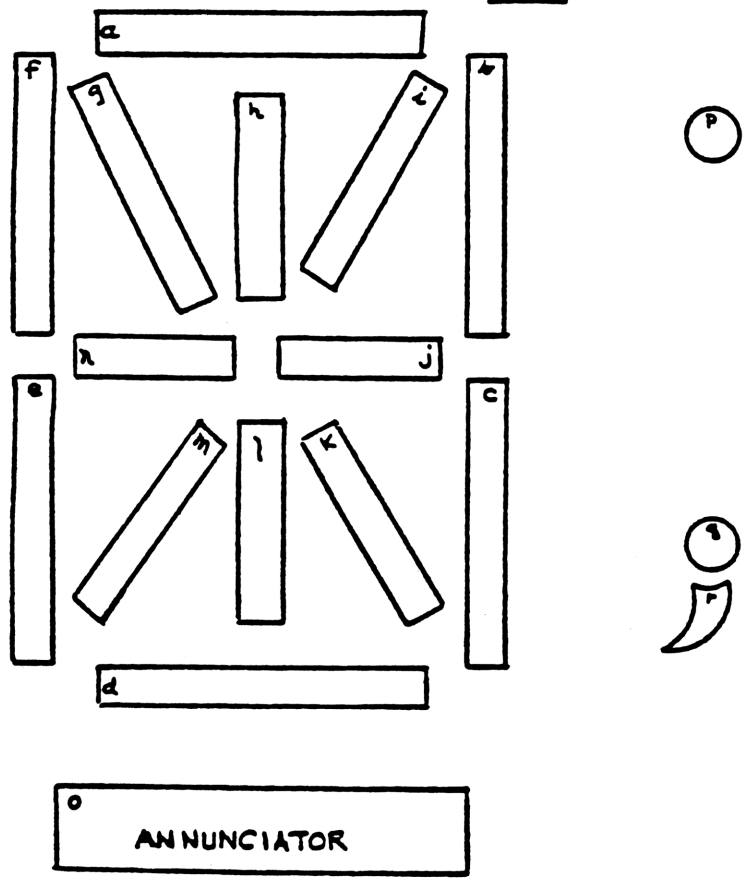
3.2 When in peripheral mode (DPWO always high), the oscillator runs regardless of display status.

3.3 If an address outside the 80 possible is issued to the character ROM, then a blank is displayed.

3.4 IAF and IAL are preset high every start up (PWO). If there is more than 1 display driver in a display system and 2 or more have IAF status bits high, then those with IAF high will try to drive the on board oscillator. This "fight" causes row

synchronization to be lost and the display to be garbled. In normal operation, 1's and 0's will appear on DATA, DATA IN, and DATA OUT causing IAF and IAL to be cleared to their proper states. The compare occurs until the first fetch instruction after which it is inhibited. If no "1's" occur on DATA between start up and standby, then IAF and IAL are never reset properly and the fight will occur.

Note also that if a slow device is connected to the DATA line, it may cause IAF and IAL to change state unexpectedly. If a device grabs hold at the data line and then tristates during part of its allotted time, the same thing may occur.



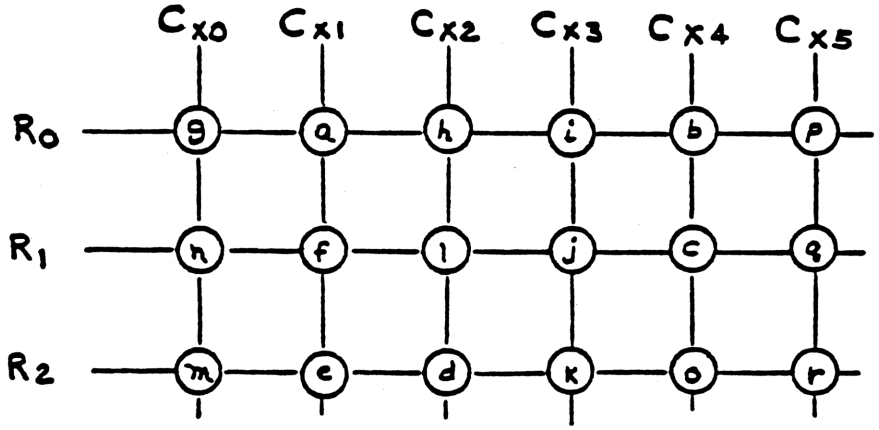


FIGURE 1

				MODEL	STK NO. 1LA4-4001
				DISPLAY DRIVER - DETAILED DESCRIPTION	
				BY Hank Koerner	DATE 11-20-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 16 OF 23
	REVISIONS			SUPERSEDES	DWG NO A-1LA4-4001-2

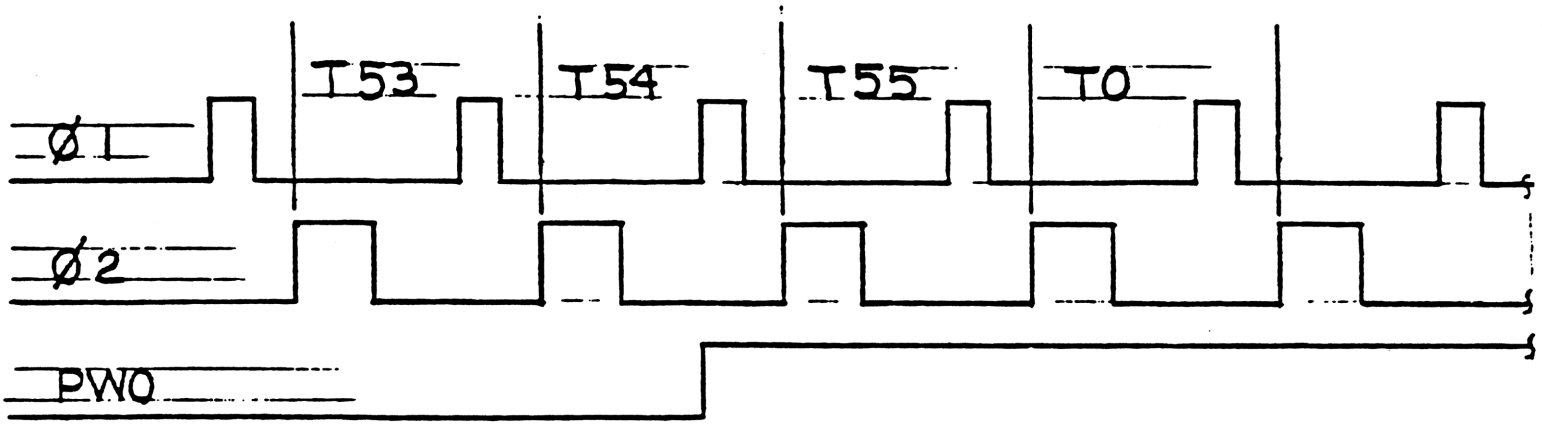
ADDRESS	CHARACTER
000	
001	
002	
003	
004	
005	
006	
007	
008	
009	
00A	
00B	
00C	
00D	
00E	
00F	
010	
011	
012	
013	
014	
015	
016	
017	
018	
019	
01A	
01B	
01C	
01D	
01E	
01F	
020	
021	
022	
023	
024	
025	
026	
027	
028	
029	
02A	

ADDRESS	CHARACTER
02B	
02C	
02D	
02E	
02F	
030	
031	
032	
033	
034	
035	
036	
037	
038	
039	
03A	
03B	
03C	
03D	
03E	
03F	
100	
101	
102	
103	
104	
105	
106	
107	
108	
109	
10A	
10B	
10C	
10D	
10E	
10F	

FIGURE 3

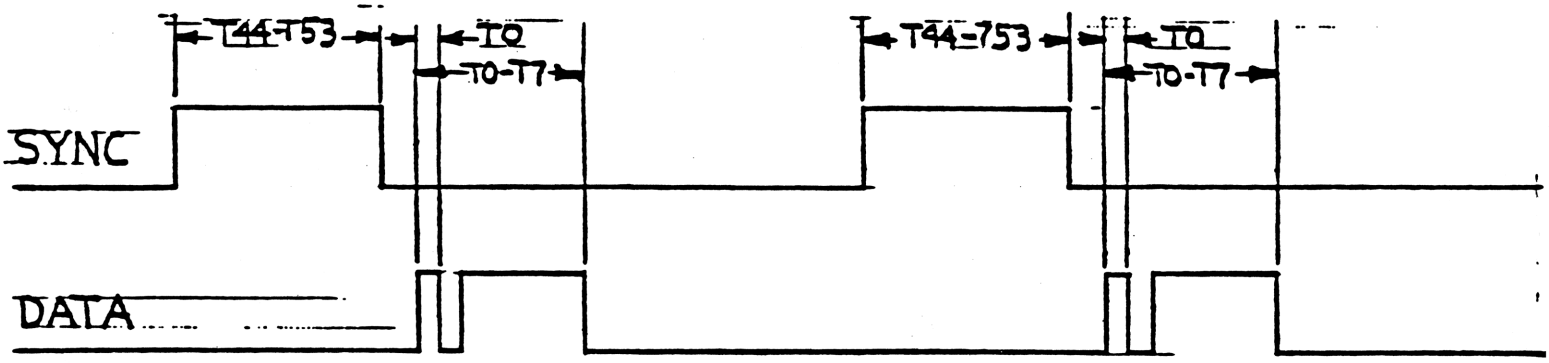
LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL	STK. NO 1LA4-4001
DETAILED DESCRIPTION - DISPLAY DRIVER	
BY Hank Koerner	DATE 11-20-78
APPD	SHEET NO 17 OF 23
SUPERSEDES	DWG NO A-1LA4-4001-2



START UP SEQUENCE - RISING EDGE OF PWO INITIALIZES TIMING, FROM EDGE TO EDGE OF Ø2 DEFINES 1 BIT TIME.

FIGURE 4A

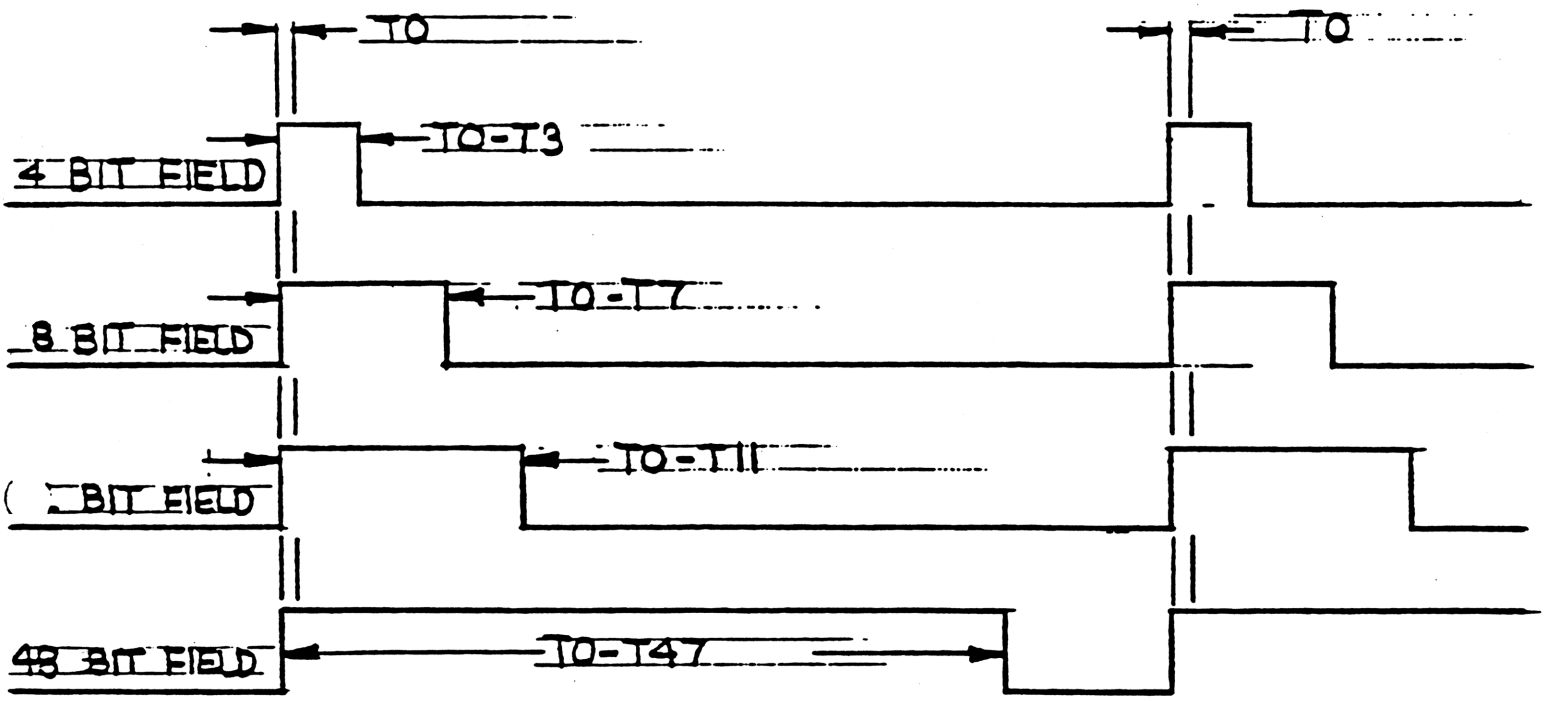


SYNC AND PERIPHERAL ADDRESS TIMING - SYNC OCCURS FOR 10 BIT TIMES FROM T44 THROUGH T53. PERIPHERAL ADDRESSES OCCUR FROM TO THROUGH T7. THE. ADDRESS FOR THE DIAPLAY DRIVER, FD_{16}, IS SHOWN IN THIS EXAMPLE.

FIGURE 4B

LTR	P C NO	APPROVED	DATE
		REVISIONS	

MODEL	STK NO 1LA4-4001
DISPLAY DRIVER - DETAILED DESCRIPTION	
BY Hank Koerner	DATE 11-20-78
APPD	SHEET NO 18 OF 23
SUPERSEDES	DWG A-1LA4-4001-2



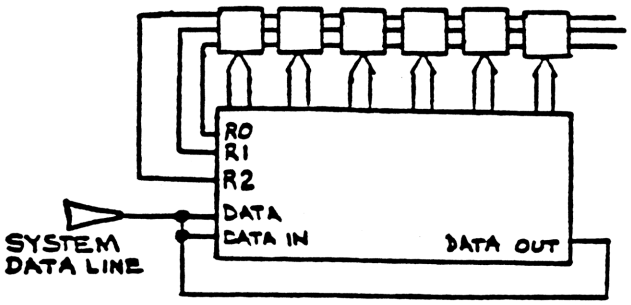
RELATIVE TIMING OF DIFFERENT LENGTH TRANSFERS FOR FETCH AND STORE INSTRUCTIONS

FIGURE 4C

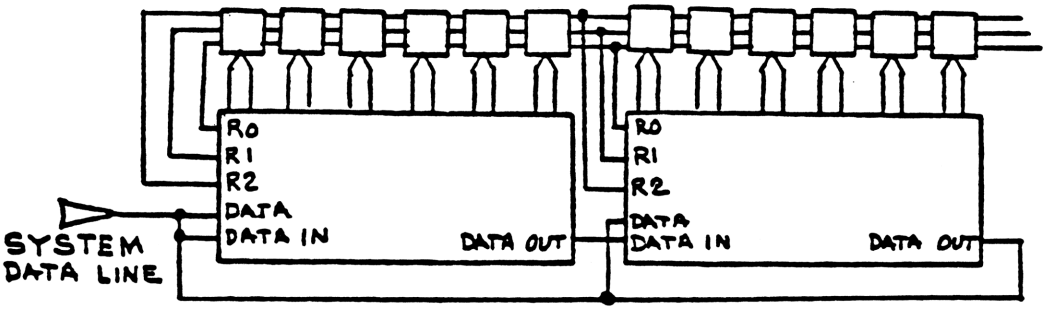
LTR	P C NO	APPROVED	DATE
REVISIONS			

MODEL	STK NO 1LA4-4001
DISPLAY DRIVER - DETAILED DESCRIPTION	
BY Hank Koerner	DATE 11-20-78
APPD	SHEET NO 19 OF 23
SUPERSEDES	DWG NO. A-1LA4-4001-2

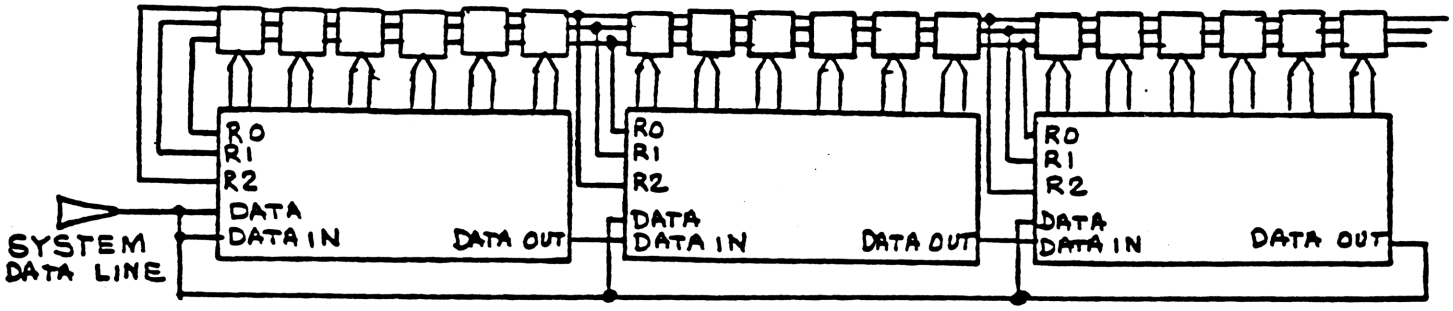
EACH BOX REPRESENTS 1 STARBURST CHARACTER



1 CHIP, 6 CHARACTER SYSTEM



2 CHIP, 12 CHARACTER SYSTEM



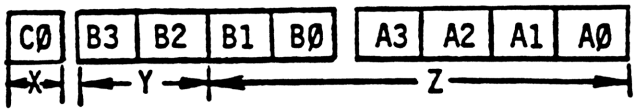
3 CHIP, 18 CHARACTER SYSTEM

INTERCONNECTION FOR 3 DIFFERENT SIZE DISPLAY SYSTEMS

FIGURE 5

LTR	P C NO	APPROVED	DATE
		REVISIONS	

MODEL	STK NO 1LA4-4001
DISPLAY DRIVER - DETAILED DESCRIPTION	
BY Hank Koerner	DATE 11-20-78
APPD	SHEET NO 20 OF 23
SUPERSEDES	DWG NO A-1LA4-4001-2



X Register C stores the first bit of a digit; it is used for upper/lower half ROM select.

Y B3, B2 of the B register determine punctuation as follows:

B3	B2	
0	0	No punctuation
0	1	period or decimal point
1	0	colon
1	1	comma

Z Character definition - 1 of 64 possible

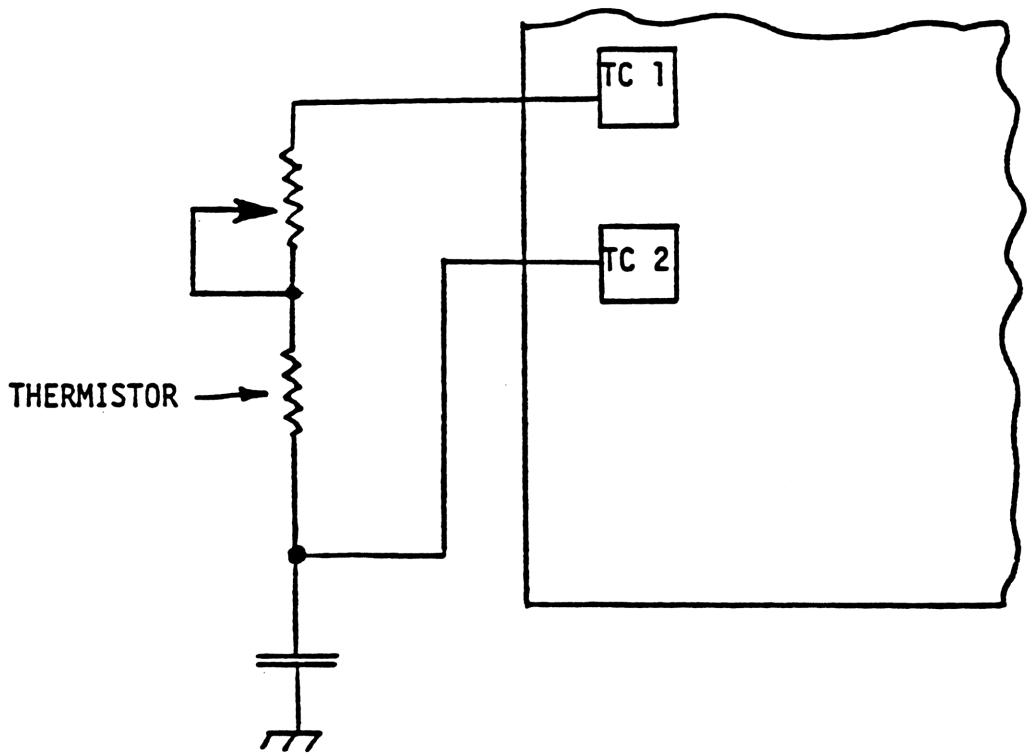
ANNUNCIATORS: Annunciators are specified by the contents of the E register. There is 1 annunciator bit per character.

CHARACTER DEFINITION

FIGURE 6

LTR	P.C. NO	APPROVED	DATE
		REVISIONS	

MODEL	STK. NO 1LA4-4001
DETAILED DESCRIPTION - DISPLAY DRIVER	
BY Hank Koerner	DATE 11-20-78
APPD	SHEET NO 21 OF 23
SUPERSEDES	DWG. NO A-1LA4-4001-2

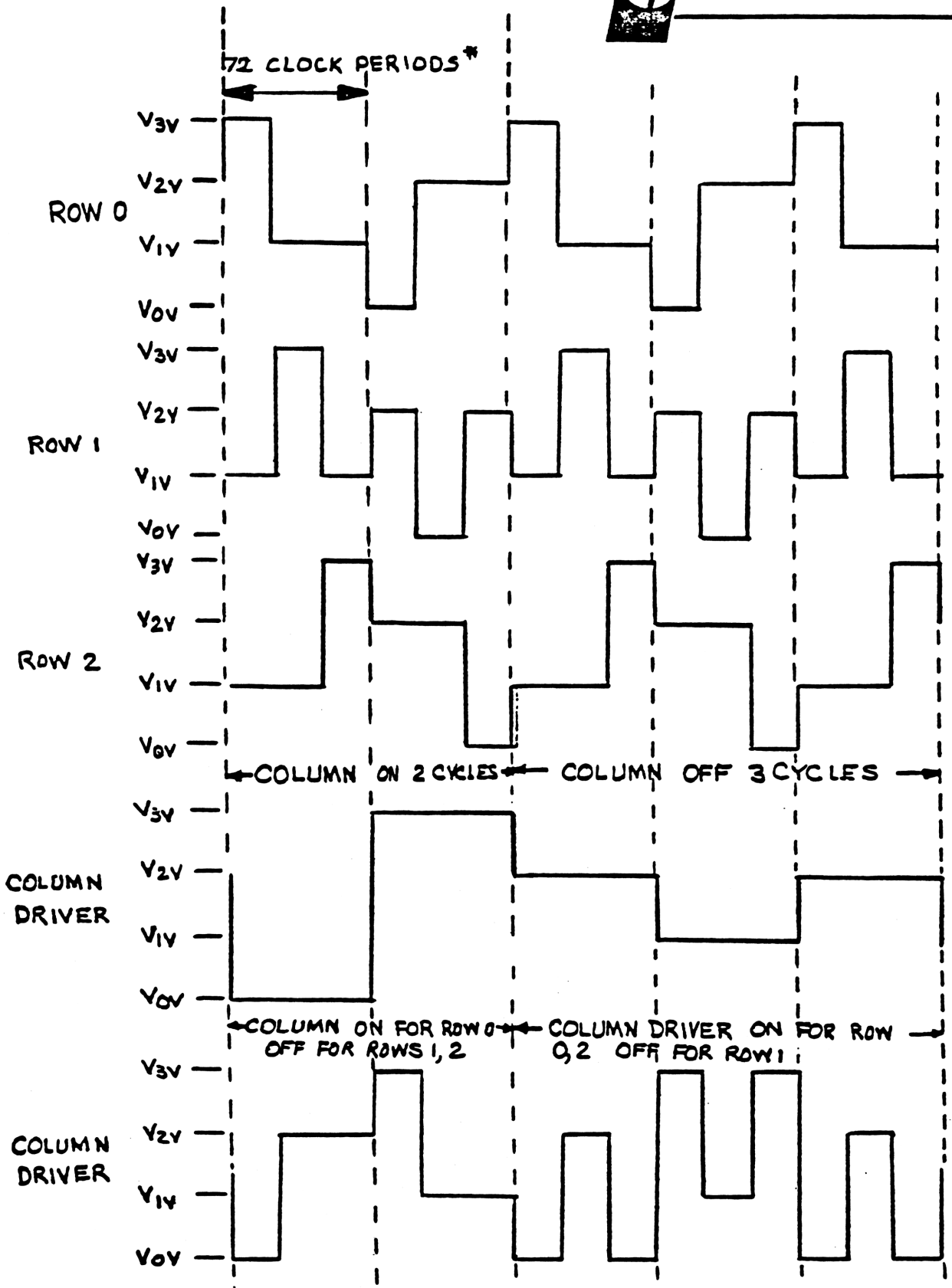


COMPONENT CONNECTION TO TEMPERATURE CONPENSATION CIRCUITRY

FIGURE 7

				MODEL	STK NO 1LA4-4001
				DISPLAY DRIVER - DETAILED DESCRIPTION	
				BY Hank Koerner	DATE 11-20-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 22 OF 23
	REVISIONS			SUPERSEDES	DWG NO A-1LA4-4001-2

HEWLETT-PACKARD CO.



* 72 WORD TIMES WITH SYSTEM RUNNING ~ 10.6 ms @ 380 KHZ
72 INTERNAL OSCILLATOR CYCLES.

FIG. 8

LTR	P C NO	APPROVED	DATE	MODEL	STK NO. 1LA4-4001
				DISPLAY DRIVER - DETAILED DESCRIPTION	
				BY Hank Koerner	DATE 11-20-78
				APPD	SHEET NO 23 OF 23

HP 41 RAM CHIP

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As Issued	3-19-79	JW

Model No.	Stock No. SEE PAGE 6
Title DATA STORAGE	
Description DETAILED DESCRIPTION	Date 6-5-78
By John Wong	Sheet No. 1 of 6
Supersedes Shashi Iyengar 6/14/79	Drawing No. A-1LA7-9002-1

9320-3246 (6/75)

I DETAILED DESCRIPTION

The CMOS Data Storage circuit (DS2D) is a modified circuit of the existing part (5061-0493). DS2D contains 16 registers of 56 bits ling. The Ø1 and Ø2 clocks have been inverted to work with the 41C and the 30's CPU's. The chip address has been increased to 6 bits ling to allow up to 64 chip addresses in the system. B6 is internally programmed to "0" level, while B1, B2, B3, B4 and B5 are brought out for external programming. Internal pulldown circuit has also been added on these pins so that they are normally at a "0" level. To program the bit to a "1", simply connect the pad to V_{CC} (or die attach area).

II DS2D SIGNAL DESCRIPTION

2.1 CLOCKS (Ø1, Ø2) - The clocks are active high clocks originated from the CPU. Ø1 is the input strobe clock, while Ø2 starts the output transfer. A bit time is defined from the leading edge of Ø2 to the next leading edge of Ø2.

2.2 ISA - Instructions generated by the ROM'S are read in from the ISA line during SUNC time. The chip decodes 5 instrucitons and ignores the rest.

2.3 SYNC - The SYNC signal is used to synchronize DS2D to the rest of the system. When SYNC is not present, instructions on ISA are ignored.

2.4 DATA - data is a bi-directional line used to transfer data between the processor chip and DS2D. The DATA line remains tri-stated at all times except during read instruction.

2.5 PWO - PWO is a power on indication coming from the CPU. After PWO goes high, DS2D goes active at the falling edge SYNC. As soon as PWO goes low, DS2D stops it's internal clocks and locks out everything to preserve the memory data.

2.6 TEST - TEST is a normally pulled high input for test purpose. When TEST is pulled low (to GND). The DATA line is forced into tri-state through a minimal amount of logic. This prevents bad chips from effecting others.

2.7 B1, B2, B3, B4, B5 - Externally programmable pins for DS2D chip select. These are internally pulled low.

III INSTRUCTIONS

There are five instrucitons that DS2D responds to.

3.1 DADD=C,A 10 bit address is loaded into the DS2D chip from the DATA line during the next word time. The 10 bits comes in during $T_{\emptyset}$ to T_9. Register address of 0 to 15 corresponds to $T_{\emptyset}$ - T_3 ($T_{\emptyset}$ = LSB). Chip address of 0 to 63 corresponds to T_4-T_9 (T_4 = LSB). A DATA word is defined from $T_{\emptyset}$ to T_{55}. Once addressed, the chip remembers both addressed, the chip remembers both addresses until a new one is issued or with a new power on. If a chip is not selected, it ignores the following instructions.

3.2 DATA=C,The contents of the C register on the CPU is written into the previously addressed register during the next word time ($T_{\emptyset}$- T_{55}) via the DATA line.

3.3 C=DATA,The contents of the previously addressed register is read out into the C register during the next word time.

3.4 REGN=C,Contents of the C-register is written into register N (where N=0 to 15) of DS2D during the next word time. N is the 4 MSB's of the instructions, which overwrites the previous register address information. REGN=C is a direct write instruction for the enabled chip.

3.5 C=REGN, Contents of register N (where N=1 to 15) of DS2D is read out into the C register during the next wordtime. C=REGN is a direct read instruction for the enabled chip, except for register 0. Note that C=REGØ is equivalent to C=DATA. Therefore, register 0 can only be addressed indirectly.

HEWLETT-PACKARD CO.

USED ON

1LA7-0001

1LA7-0001

1LA7-0002

1LA7-0003

1LA7-0004

1LA7-0005

1LA7-0006

	See Sheet 1			MODEL	STK NO SEE ABOVE
				DETAILED DESCRIPTION - DATA STORAGE	
				BY John Wong	DATE 6-5-78
LTR	P C NO	APPROVED	DATE	APPD	SHEET NO 6 OF 6
-	-	REVISIONS		SUPERSEDES	DWG NO A-1LA7-9002-1

9320-2782 (FORMERLY 0-700024)

HP-IL CHIP

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	AS ISSUED	12-17-80	

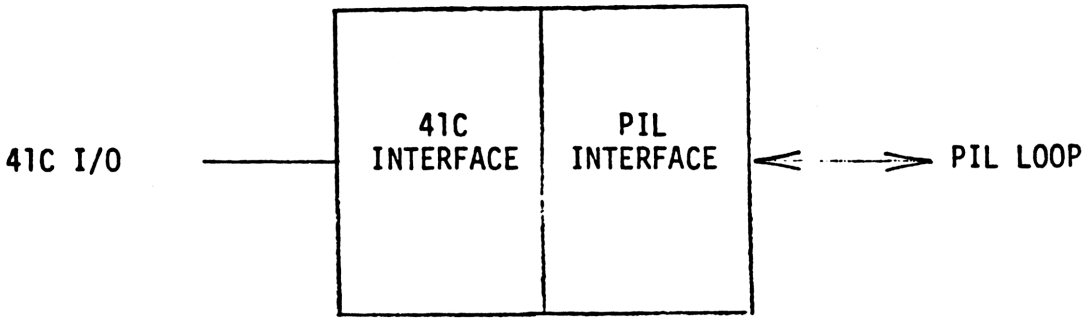
Model No.		Stock No.	1LB6-4001
Title	41C PIL INTERFACE CHIP		
Description	DETAILED DESCRIPTION	Date	8-21-80
By	CARL LANDSNESS	Sheet No.	1 of 9
Supersedes		Drawing No.	A-1LB6-4001-2

I. GENERAL DESCRIPTION

This document describes the PIL Interface Chip. The PIL Interface chip communicates directly to the 41C I/O bus and to the PIL loop through several discrete components and 2 pulse transformers. The PIL Interface Chip, discrete components, and 2 41C ROMs are packaged in a PC hybrid. The PC hybrid, pulse transformers, and mechanical connectors are packaged in a 41C plug-in module.

The PIL Interface Chip consists of 2 major portions, the 41C interface and the PIL interface:

PIL Interface Chip



The PIL interface portion is very similar to the PIL interface for the 85A and General Purpose interfaces as described in "PIL Chip ERS" by Dave Sweetser, June 1978. This document will describe the 41C interface portion and any differences in the PIL interface from the above mentioned ERS. Therefore, it is very important that the reader first read and understand that ERS.

II. CHIP ARCHITECTURE

Shown in Figure 1, is a block diagram of the 41C PIL interface portion. The function of the major blocks will be described later. Communication with PIL is done by reading and writing to 1 of 8 PIL registers. These Registers are defined in FIGURE 2 and differences from the GP chip.

register difinition are noted. Note that some registers are read or write only.

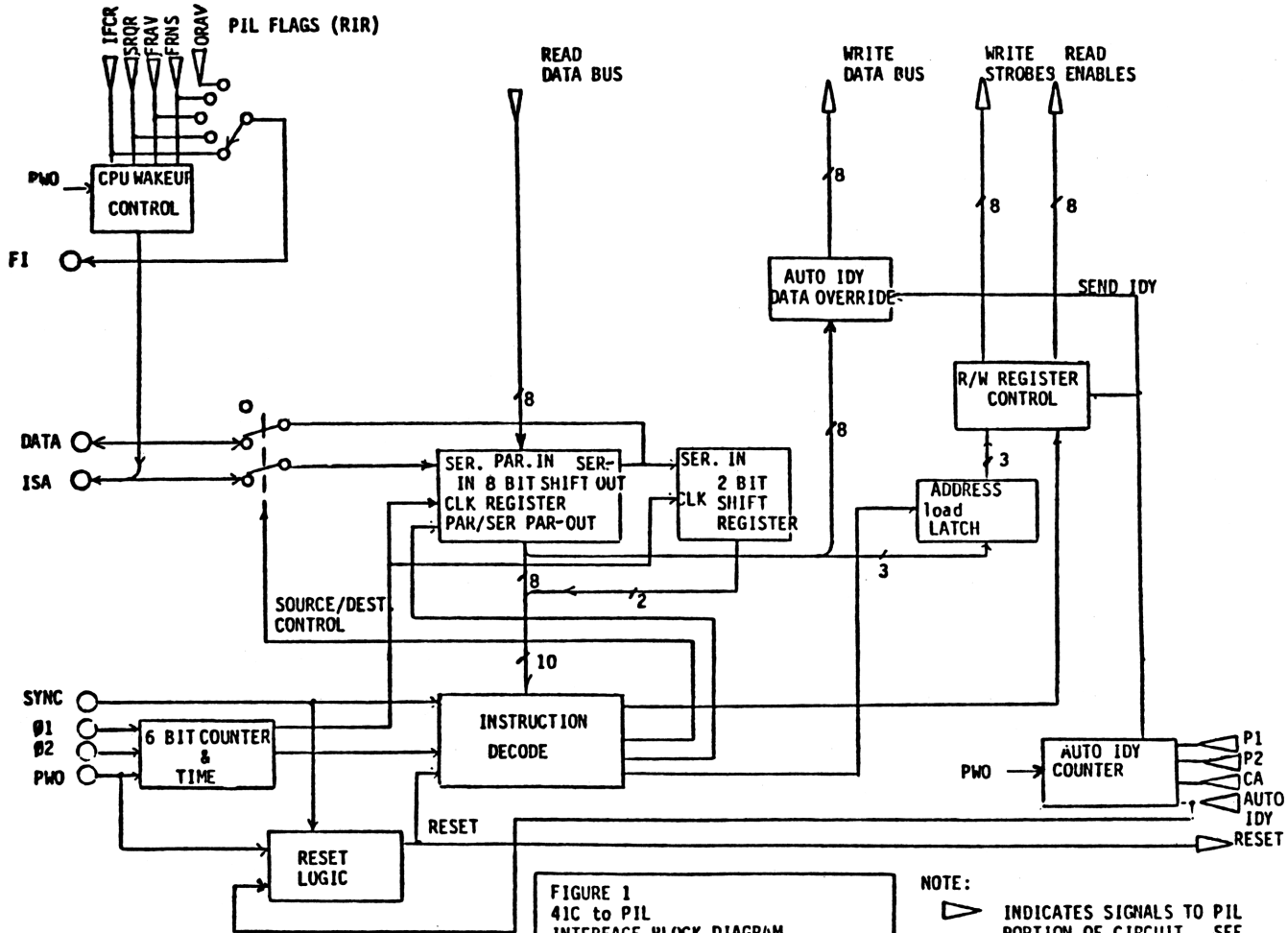


FIGURE 1
41C to PIL
INTERFACE BLOCK DIAGRAM
(INTERFACE PORTION ONLY)
C. LANDSNESS 2/80

NOTE:
▷ INDICATES SIGNALS TO PIL PORTION OF CIRCUIT. SEE PIL ERS BY DAVE SWEETSER FOR DETAILS.

				MODEL	STK NO
				41C PIL INTERFACE DETAILED DESCRIPTION	
				BY CARL LANDSNESS	DATE 8-21-80
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		REVISIONS			

FIGURE 2: PIL REGISTERS

		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
STATUS REGISTER	ROR/W	SC	CA	TA	LA	SSRQ	RFCR	CLIFCR (NOTE1)	MCL	READ
							SLRDY	CLIFCR		WRITE

SC - System Controller
CA - Controller Active
TA - Talker Active
LA - Listner Active
SSRQ - Send Service Request
RFCR - RFC Received
MCL - Master Clear
SLRDY - Set Local Ready
CLIFCR - Clear 'Interface Clear Received'

NOTE: SLRDY and CLIFCR are self-resetting bits (resetting occurs 1-2 uSec after end of write pulse). Reading ROR/W returns the value of CLIFCR (which is always a logic 0 if reading occurs 2 uSec after any write of a 1 to the bit).

CONTROL INTERRUPT REGISTERS	RIR	C13	C12	C11	IFCR	SRQR	FRAV	FRNS	ORAV	READ
	RIW	C03	C02	C01	*	*	*	*	FLGENB*	WRITE

C13-C11 - Input Control bits from received frame.
IFCR - Interface Clear Received.
SRQR - Service Request Received.
FRAV - Frame Available.
FRNS - Frame Received Not as Sent.
ORAV - Output Register Available
FLGENB - Flag Enable. Writing a Ø to FLGENB disables (tri-states) the FI line.
C03-C01 - Output Control bits to be transmitted.

DATA INPUT-OUTPUT REGISTERS	R2R	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	READ
	R2W	D08	D07	D06	D05	D04	D03	D02	D01	WRITE

D18-D11 - Input Data bits from received frame.
D08-D01 - Output Data bits to be transmitted.

PARALLEL POLL REGISTER	R3R/W	OSCDIS*	AUTO IDY*	PPIST	PPEN	PPSENSE	P3	P2	P1	READ / WRITE

OSCDIS - Oscillator Disable. Writing a 1 to OSCDIS sets OSCEN=Ø if MCL=1. See CHIP INTIALLIZATION.
AUTO IDY - Automatic IDY sourcing when 41C is in light sleep if CA=1
PPIST - Parallel Poll Individual Status.
PPEN - Parallel Poll Enable.
PPSENSE - Parallel Poll Sense.
P3-P1 - Parallel Poll Response bit designation.

LOOP ADDRESS REGISTER	R4R/W				ADR4	ADR3	ADR2	ADR1	ADR0	READ/WRITE
SCRATCHPAD REGISTER	R5R/W									READ/WRITE
SCRATCHPAD REGISTER	R6R/W									READ/WRITE
SCRATCHPAD REGISTER*	R7R/W									READ/WRITE

* Denotes differences from 85A/GP chip.

III. INSTRUCTIONS

The following instructions are used to communicate with the PIL interface. Refer to NUT CPU description for 41C instruction formats and timing.

INSTRUCTION	41C CODE I9 I0	MASM MNEUMONIC
C⟶PIL(N)	1NNN000000	PIL=C M1
CHAR⟶PIL(N)	ONNN100100 CCCCCCCC01	HPL=CH M1 CH= M2
PIL(N)⟶C	1NNN100100 0000111010 0000000011	C=PIL M1
IFCR?	0101101100	1FCR?
SRQR?	1010101100	SRQR?
FRAV?	0100101100	FRAV?
FRNS?	1001101100	FRNS?
ORAV?	0011101100	ORAV?

C⟶PIL(N)

A one word CPU instruction C⟶PIL(N) will transfer digits 0 and 1 of the 41C register to one of the eight 8 bit PIL registers selected by N.

CHAR⟶PIL(N)

A two word instruction CHAR⟶PIL(N) transfers an 8 bit constant directly from ROM to one of the eight PIL registers selected by N. The first instruction word is a CPU PERI(N) instruction where PIL registers are treated as 8 separate peripherals out of a possible 16. The second

instruction word contains the 8 bit constant in bits I2-I9 (I2=LSB) and returns decode control to CPU (IO=1).

PIL(N)→C

A three word instruction PIL(N)→C reads the contents of one of eight PIL registers selected by N into digits 0 and 1 of 41C C register. The remainder of the C register is filled with zeros. The first instruction word is a CPU PERI(N) instruction where N selects one of eight PIL registers and passes decode control to PIL. The second instruction word is a CPU DATA→C instruction which reads the data from the selected register into C. The third instruction word returns decode control to the CPU. The third instruction word is only needed because the 41C CPU cannot presently execute a DATA→C and RETURN (IO=1) as described in CPU description.

FLAG TESTS

The five PIL interruptbits (IFCR, SRQR, FRAV, FRNS, and ORAV) located in R1R (Register 1 Read) are multiplexed onto the FLGIN line during digit times 6-10 to allow interrogation by CPU instructions:

IFCR? sets carry if "Interface Clear Received" = 1 (Flag 6)
SRQR? sets carry if "Service Request Received" = 1 (Flag 7)
FRAV? sets carry if "Frame Available" = 1 (Flag 8)
FRNS? sets carry if "Frame Received Not as Sent" = 1 (Flag 9)
ORAV? sets carry if "Output Register Available" = 1 (Flag 10)

These flags may be disabled (FLGIN line tri-stated) by writing a Ø to FLGENB (LSB of R1W).

IV. AUTOIDY MODE

If the 41C is in light sleep (SYNC•$\overline{PWO}$=1) and if CA=1 and if AUTOIDY=1 (bit 6 of R3), then the PIL chip hardware will generate an IDY frame every 10mS to allow loop devices to insert a service request. No hand-shaking is performed. If SRQR goes true, ISA will be pulled high. This will wake-up the CPU and a serial or parallel poll may then be performed. The 8 data bits of the automatically generated IDY are undefined, so it should not be used for a parallel poll.

If 41C is in light sleep and CA=0 and AUTOIDY=1, the PIL chip will remain running, but it will not generate IDY frames. However, it may still receive and transmit frames. If IFCR or FRAV or FRNS go true, ISA will be pulled high waking up the 41C CPU.

AUTOIDY (bit 6 of R3) is not affected by MCL. However, AUTOIDY will power on low when power is first applied to the chip.

V. CHIP INITIALIZATION

This section replaces section 17 (Chip Initialization) in "PIL CHIP ERS" by Dave Sweetser.

The 41C PIL chip provides for several levels of initialization. Complete chip initialization occurs when an internal signal RESET goes true when:

1) 41C is in deep sleep ($\overline{PWO}$·$\overline{SYNC}$=1), or
2) 41C is in light sleep ($\overline{PWO}$·SYNC=1) and PIL chip is not in AUTOIDY mode (bit 6 of R3=0), Boolean equivalent: RESET=$\overline{PWO}$·$\overline{SYNC}$+$\overline{PWO}$·$\overline{AUTOIDY}$.

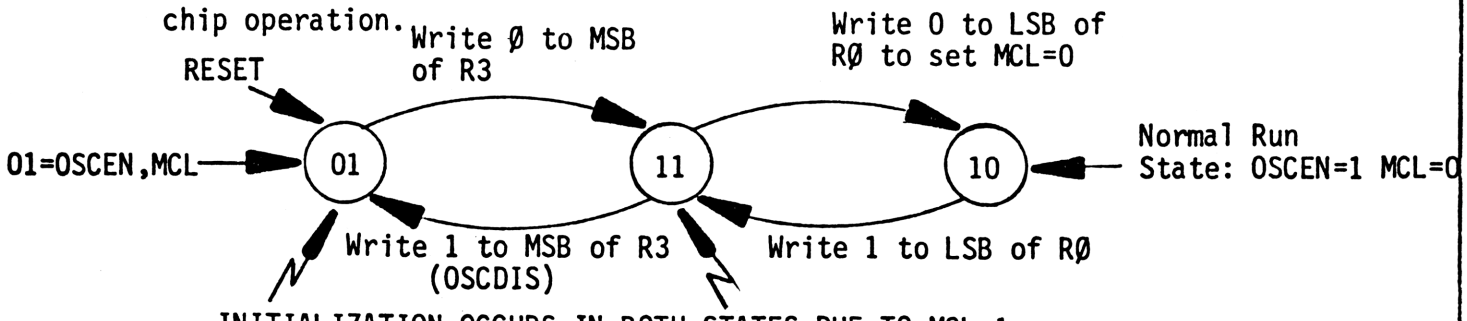
RESET provides the following initialization:

1) Initializes 41C timing and decode logic.
2) Turns off the PIL oscillator by resetting the oscillator enable signal, OSCEN, to Ø.
3) Resetting OSCEN also forces MCL (LSB of RØ) to be set to 1. This signal resets all the PIL Interface section logic.

MCL provides the following initialization:

1) IFCR=SRQR=FRNS=FRAV=0
2) ORAV=1
3) FLGENB bit in R1W reset to Ø.
4) The SC (System Controller) bit in RO is set to the state defined by external input SCTL. Input is internally pulled low.
5) The internal latch RTSR is reset.
6) Driver and Acceptor PLA's set to DIDS and AIDS.

Shown below is a state diagram relating RESET, MCL, and OSCEN. The use of three states permits an orderly transition after power-on, i.e., first the oscillator is enabled and then MCL is set to Ø to permit chip operation.



				MODEL	STK NO
				41C PIL INTERFACE DETAILED DESCRIPTION	
				BY CARL LANDSNESS	DATE 8-21-80
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		REVISION		SUPERSEDES	DWG NO A-11B6-4001-2

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	AS ISSUED	11-27-79	

Model No.	Stock No. 1LB6-4001
Title 1LB6 (PIL)	
Description ELECTRICAL SPECIFICATION	Date 11-27-79
By CARL LANDSNESS	Sheet No. 1 of 14
Supersedes	Drawing No. A-1LB6-4001-1

I. ABSOLUTE MAXIMUM RATINGS:

1.1 SUPPLY VOLTAGE V_{CC} (GND = V) ..... +10 VOLTS
1.2 STORAGE TEMPERATURE ..... -50°C to +150°C
1.3 OPERATING TEMPERATURE ..... 0°C to 65°C
1.4 HUMIDITY ..... 0 to 90%
1.5 VOLTAGE AT ANY INPUT OR OUTPUT PIN ..... GND -0.3V to V_{CC} +0.3V
1.6 INPUT TRANSIENT PROTECTION STANDARD ..... 500 VOLTS (SEE FIG. 1)
1.7 INPUT TRANSIENT PROTECTION ON RXDO,RXD1,TXDO,TXD1.... 5000 VOLTS

II. OPERATING CONDITIONS: $0°C \leq T_A \leq 45°C$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENTS
GND	GROUND	0.0	0.0	0.0	V	
V_{CC}	SUPPLY VOLTAGE (SUBSTRATE)	6.0	6.25	7.0	V	
ICCOP	V_{CC} OPERATING CURRENT			2.5	mA	V_{CC}=6.5V OUTPUT LOADS=MAX. FREQ.=MAX RXDO,RXD1,$\overline{SCTL}$=0
ICCST	V_{CC} STANDBY CURRENT			1.0	uA	V_{CC}=5.0V, GND=0V ISA, DATA, RXDØ, RXD1, Ø1, Ø2. SYNC PWO=0V. All other pins open.
ICCTR	V_{CC} OPERATING CURRENT WHILE RETRANSMITTING			3.5	mA	V_{CC}=6.5V FREQ.=MAX 1.6K LOAD BETWEEN TXDO, TXD1; Output loads=max; Frame retransmitted every other frame time.
	INPUT PARAMETERS:					
VIH	INPUT LOGIC "1" VOLTAGE LEVEL	V_{CC} -1.25	.8V_{CC}		V	All inputs except RXDØ, RXD1
VIL	INPUT LOGIC "0" VOLTAGE LEVEL		.2V_{CC}	GND+1.25	V	

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENTS
VRXH	INPUT LOGIC "1" ON RXDO, RXD1	4.2			V	PIL FREQ=MIN.
VRXL	INPUT LOGIC "0" ON RXDO, RXD1			GND+1.25V	V	PIL FREQ=MIN. TRPW=MIN.
VRXTH+	HIGH LEVEL THRESHOLD ON RXDO, RXD1	2.2	3.3	4.2	V	
VRXTH-	LOW LEVEL THRESHOLD ON RXDO, RXD1	1.25	2.3	3.3	V	
VRXHYS	INPUT HYSTERISIS ON RXDO, RXD1	0.5V			V	
ILIN	INPUT LEAKAGE CURRENT ON INPUT PINS			0.1	uA	AT 6.5V to GND AND V_{CC}, EXCEPT TSTCLK, $\overline{SCTL}$
ILIO	INPUT LEAKAGE CURRENT ON I/O PINS			1.0	uA	AT 6.5V to GND V_{CC}. PINS TRI-STATED EXCEPT LC1, LC2 V_{CC}=6.5V
	INPUT CURRENT					V_{CC}=6.5V
IHTCLK	TSTCLK HIGH CURRENT			+50	nA	AT 6.5V
ILTCLK	TSTCLK LOW CURRENT	-0.15		-0.01	mA	AT ØV
IHSCTL	$\overline{SCTL}$ HIGH CURRENT	0.05		+0.5	mA	AT 6.5V
ILSCTL	$\overline{SCTL}$ LOW CURRENT	-50			nA	AT ØV
CIN	INPUT CAPACI-TANCE			8	pF	ALL INPUT AND I/O PINS
	OUTPUT PARAMETERS:					
VOH	OUTPUT LOGIC "1" VOLTAGE LEVEL	V_{CC} -1.0	Ø.83V_{CC}		V	ALL OUTPUTS EXCEPT LC1, LC2

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MODEL | STK NO 1LB6-4001

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BY CARL LANDSNESS | DATE 11-27-79

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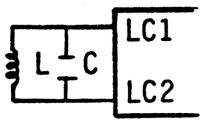
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENTS
VOL	OUTPUT LOGIC "0" VOLTAGE LEVEL		$\emptyset.17V_{CC}$	GND+1.0	V	ALL OUTPUTS EXCEPT LC1, LC2
COUT	OUTPUT CAPACITANCE DRIVE CAPABILITY					THESE OUTPUTS WILL DRIVE THE SPECIFIE CAPACITANCE BE-TWEEN VOL AND VOH WITHIN TDV. (SEE FIG. 2 & 4)
	DATA	200			pF	
	FLGIN	150			pF	
OUTPUT CURRENT (DC)						V_{CC}=MIN.
IHISA	ISA HIGH SOURCE CURRENT	0.5			mA	AT V_{OH}
ILFIN	FLGIN LOW SINK CURRENT			-0.35	mA	AT V_{OL}
IHTXD	TXDO,TXD1 HIGH SOURCE CURRENT	8.5		65.0	mA	AT V_{CC} -0.5V
ILTXD	TXDO,TXD1,LOW SINK CURRENT	-65.0		-8.5	mA	AT 0.5V
41C TIMING PARAMETERS:						
TP	CLOCK PERIOD	2.63	2.78	2.95	uS	SEE FIG. 2
TPW1	Ø1 PULSE WIDTH	500	2/8 of TP	750	nS	SEE FIG. 2
TPW2	Ø2 PULSE WIDTH	500	2/8 of TP	750	nS	SEE FIG. 2
TCD	Ø1 to Ø2 DELAY	900	3/8 of TP	1200	ns	SEE FIG. 2
TR, TF	CLOCK RISE, FALL TIME		50		nS	SEE FIG. 2

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENT
TDV	OUTPUT DATA VALID		3/8 of TP	1000	nS	AFTER TRAILING EDGE OF Ø2. SEE FIG.2 FOR ALL LINES EXCEPT ISA AT A ZERO LEVEL AND DATA AT EITHER LEVEL.
			3/8 of TP	800	nS	FOR ISA AT A ZERO LEVEL AND DATA AT EITHER LEVEL.
TSU	INPUT DATA SETUP TIME	550	2/8 of TP		nS	BEFORE TRAILING EDGE OF Ø1. SEE FIG. 2. ISA,DATA, SYNC,PWO INPUTS.
	PIL TIMING PARAMETERS:					
	THE FOLLOWING TIMING SPECIFICATIONS ARE FOR L AND C AS SHOWN.					
C	CAPACITANCE	114.0	120	126.0	pF	
L	INDUCTANCE	53.2	56	58.8	uH	
R_L	INDUCTOR SERIES RESISTANCE			6	Ω	
TLC	OSCILLATOR PERIOD	475	500	550	nS	MEASURED AT LC1 AND LC2 (MEASURING PROBE C<1pF)
TCLK	TSTCLK INPUT PERIOD	450	500	550	nS	
TCLKR TCLKF	TSTCLK RISE & FALL TIME		50		nS	
TRXPW	RXDO,RXD1 PULSE WIDTH	650		1.5	ns	SEE FIG.4
TRXTR	RXDØ,RXD1 TRANSITION TIME			300	nS	
TRXSU	RXDO,RXD1 SETUP TIME	50			nS	BEFORE TRAILING EDGE OF TCLK. SEE FIG.4

LTR	P C NO	APPROVED	D
	REVISIONS		

MODEL | STK NO 1LB6-4001

1LB6 ELECTRICAL SPECIFICATION

BY CARL LANDSNESS | DATE 11-27-79

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SUPERSEDES | DWG NO A-1LB6-4001-1

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	COMMENT
TRXHD	RXDØ,RXD1 HOLD TIME	50			nS	AFTER TRAILING EDGE OF TCLK. SEE FIG.4
TRXLO	RXDØ,RXD1 LOW TIME BETWEEN PULSES	1.3			uS	
TRXOV	RXDØ,RXD1 OVER-LAP TIME	0		300	nS	
TTXPW	TXDØ,TXD1 PULSE WIDTH	950	2xTLC OR 2xTCLK	1200	nS	MEASURED WITH 470pF LOAD. SEE FIG.5
TTXTR	TXDØ,TXD1 TRANSITION TIME			120	nS	MEASURED WITH 470pF LOAD. SEE FIG.5
TTXOV	TXDØ,TXD1 OVERLAP TIME	0		120	nS	MEASURED WITH 470pF LOAD. SEE FIG.5

III. SUMMARY OF SIGNALS:

SIGNAL	I/O	DESCRIPTION
Ø1, Ø2	IN	41C SYSTEM CLOCKS
SYNC	IN	PROVIDES SYSTEM TIMING AND INDICATES THE PRESENCE OF A SYSTEM INSTRUCTION ON THE ISA LINE. WHEN PWO IS LOW, SYNC=DPWO.
DATA	I/O	USED TO TRANSFER 56 BIT SERIAL DATA (LSB FIRST) TO AND FROM CPU C REGISTER. DATA SOURCED FROM PIL ONLY DURING WORD TIMES FOL-LOWING 2nd AND 3rd WORD TIMES OF A C=PIL INSTRUCTION (READ FROM PIL). TRI-STATED AT ALL OTHER TIMES AND ALWAYS DURING Ø2.
ISA	I/O	USED TO RECEIVE ROM DATA (INSTRUCTIONS) AT T44-T53. ISA IS PULLED HIGH WHEN REQUESTING CPU TO WAKE UP FROM LIGHT SLEEP IN RESPONSE TO PIL FLAGS-IFCR+SRQR+FRNS+FRAV. TRI-STATED BY PIL WHEN PWO IS HIGH.
PWO	IN	HIGH WHEN IN RUN MODE. USED ALONG WITH SYNC FOR INITIALLIZING CIRCUITS.

SIGNAL	I/O	DESCRIPTION
FLGIN	OUT	PULLS LOW DURING FIRST 3 BIT TIMES AND PULLS HIGH DURING LAST BIT TIME OF DIGITS 6-10 IF PIL FLAGS ARE SET AND FLAGS ARE ENABLED (PROGRAMMABLE). OTHERWISE THIS LINE IS TRI-STATED. IT IS ALWAYS TRI-STATED DURING Ø2.
V_{CC}	IN	POSITIVE VOLTAGE SUPPLY (SUBSTRATE).
GND	IN	NEGATIVE VOLTAGE SUPPLY.
LC1, LC2	I/O	PINS FOR PARALLEL LC CONNECTION FOR PIL 2MHz OSCILLATOR. OSCILLATOR IS UNDER PROGRAM CONTROL.
TSTCLK	IN	ALLOWS EXTERNAL CLOCK TO BE FED TO CHIP IN LIEU OF 2 MHz OSCILLATOR. INTERNALLY PULLED HIGH. WHEN USED, LC2 MUST BE PULLED HIGH AND EXTERNAL LC DISCONNECTED.
RXDO,RXD1	IN	RECEIVER INPUTS FROM RECEIVER TRANSFORMERS. SCHMITT TRIGGER BUFFERS ARE USED TO PROVIDE NOISE IMMUNITY.
TXDØ,TXD1	OUT	TRANSMITTER OUTPUTS TO DRIVER TRANSFORMERS.
$\overline{\text{SCTL}}$	IN	WHEN TIED LOW, CHIP WAKES UP AS SYSTEM CONTROLLER. INTERNALLY PULLED LOW.

IV. IC TEST CONDITIONS:

The preceeding pages show specifications for the 41C chips for an operating range of 0 to 45 degrees C. To insure proper operations at these temperatures, V_{CC} should be adjusted to compensate for room temperature testing as well as providing enough guard band on the part during wafer and package tests for both high and low V_{CC}.

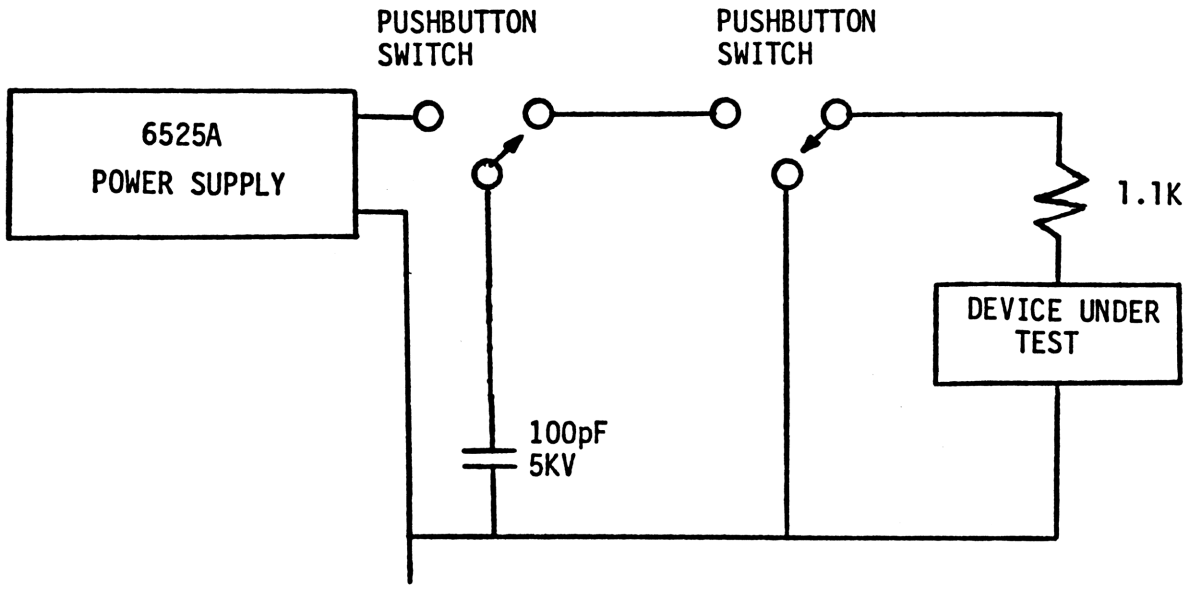
OPER. PT. 1 MIN. V. MAX F	VCC=5.5V 41C FREQ=380K PIL FREQ=2.2M	VCC=5.5V 41C FREQ=380K PIL FREQ=2.2M	VCC=5.7V 41C FREQ=380K PIL FREQ=2.2M
OPER. PT. 2 MAX.V, MIN.F	VCC=7.2V 41C FREQ=340K PIL FREQ=1.8M	VCC=7.1V 41C FREQ=340K PIL FREQ=1.9M	VCC=7.0V 41C FREQ=340K PIL FREQ=1.8M

The above table shows the different test conditions for the wafer test

package test, and thepart spec. (QA) test. All test programs should do functional tests on the part for both operating points. The table below shows a detailed breakdown of recommended values for these operating points, and a general guide for DC parametric test guard banding.

PARA	WAFER	PKG	QA	WAFER	PKG	QA
	LOW VOLTAGE			HIGH VOLTAGE		
VHRX	4.1	4.1	4.2	4.1	4.1	4.2
VLRX	1.25	1.25	1.25	1.25	1.25	1.25
VCC	5.5	5.5	5.7	7.2	7.1	7.0
VIH	4.25	4.25	4.45	5.95	5.85	5.75
VIL	1.25	1.25	1.25	1.25	1.25	1.25
VOH	4.5	4.5	4.7	6.0	6.0	6.0
VOL	1.0	1.0	1.0	1.0	1.0	1.0
	HIGH FREQUENCY			LOW FREQUENCY		
TP	2630	2630	2630	2950	2950	2950
TPW1	500	500	500	750	750	750
TPW2	500	500	500	750	750	750
TCD	900	900	900	1200	1200	1200
TDV	1000	1000	1000	1000	1000	1000
TSU	550	550	550	550	550	550
TCLK	450	450	450	550	550	550
	DC PARAMETRIC			TEST CONDITIONS		
ICCOP	2.0	2.25	2.5	VCC=6.5V, FREQ=MAX		
ICCST	0.8uA	0.9uA	1uA	VCC=5.0V, STATIC		
ILIN	90nA	100nA	--	VCC=10V, VIN=GND and VCC		
ILIO	.8uA	.9uA	1uA	VCC=6.5V, VIN=GND and VCC		
ICCTR	2.8	3.15	3.5mA	VCC=6.5V FREQ=MAX		

PARA	WAFER	PKG	QA	WAFER	PKG	QA
	DC PARAMETRIC			TEST CONDITIONS		
ILTCLK	-120uA	-135uA	-150uA	@ØV		
IHSCTL	400uA	450uA	500uA	@6.5V		
IHISA	500uA	500	500uA	@VOH @VCC (MIN)		
ILFIN	-350uA	-350	-350uA	@VOL @VCC (MIN)		
IHTXD (MIN)	9.0mA	8.7mA	8.5mA	@VCC -0.5V		
ILTXD (MAX)	-9.0mA	-8.7mA	-8.5mA	@0.5V		
IHTXD (MAX)	60mA	62mA	65mA	@VCC-0.5V		
ILTXD (MIN)	-60mA	-62mA	-65mA	@0.5V		
	STRESS TEST			COMMENTS		
VSTRESS	10V	---	---	OPERATE PARTS AT MAX. FREQ. WITH VCC= VSTRESS FPR 1 LMLOAD. IGNORE FAILURES.		



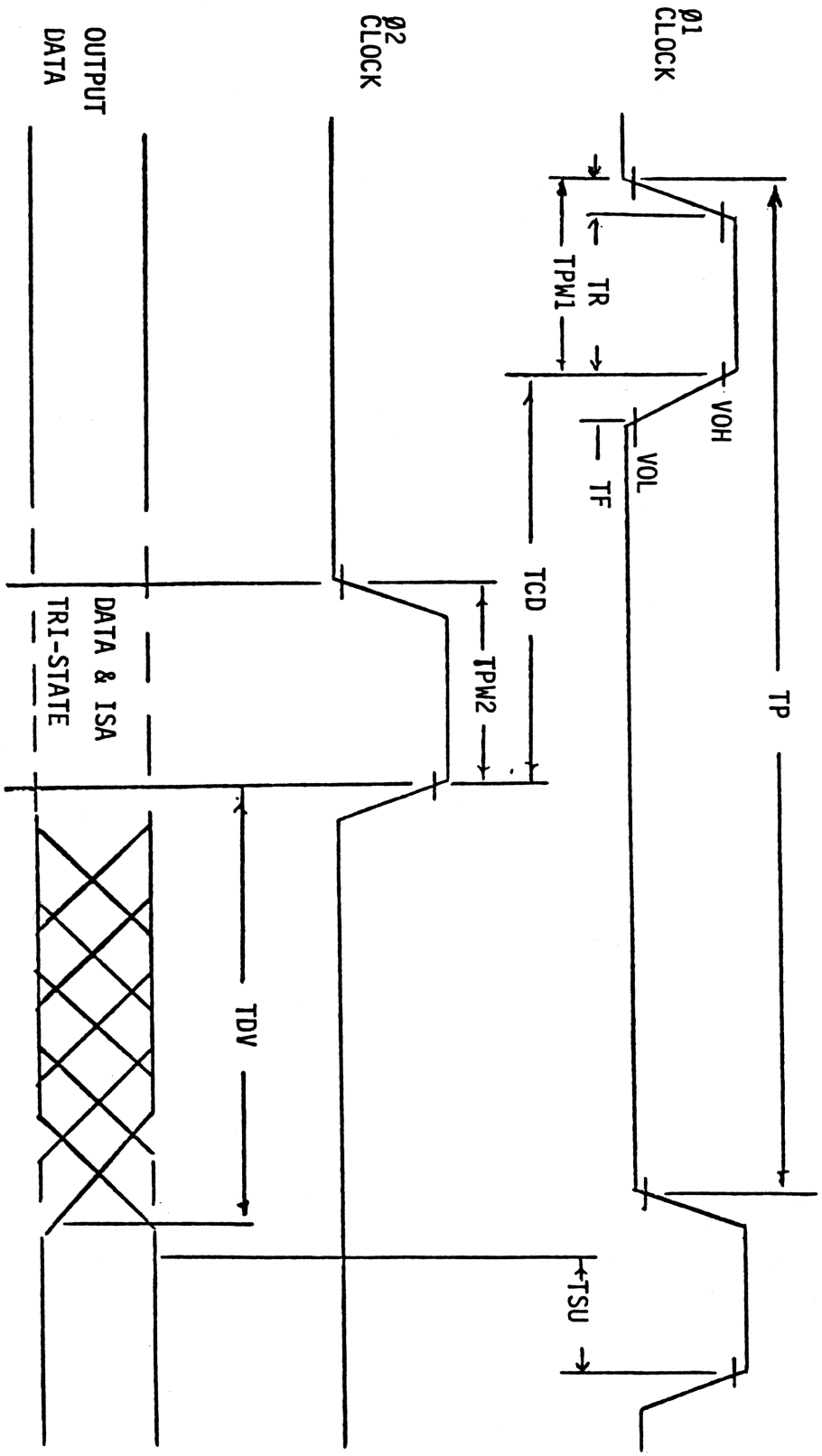
GATE PROTECTION TEST CIRCUIT

FIGURE 1

LTR	P.C. NO	APPD	DATE
	REVISIONS		

MODEL	STK. NO 1LB6-4001
1LB6 ELECTRICAL SPECIFICATION	
BY CARL LANDSNESS	DATE 11-27-79
APPD	SHEET NO 10 OF 14
SUPERSEDES	DWG. NO A-1LB6-4001-1

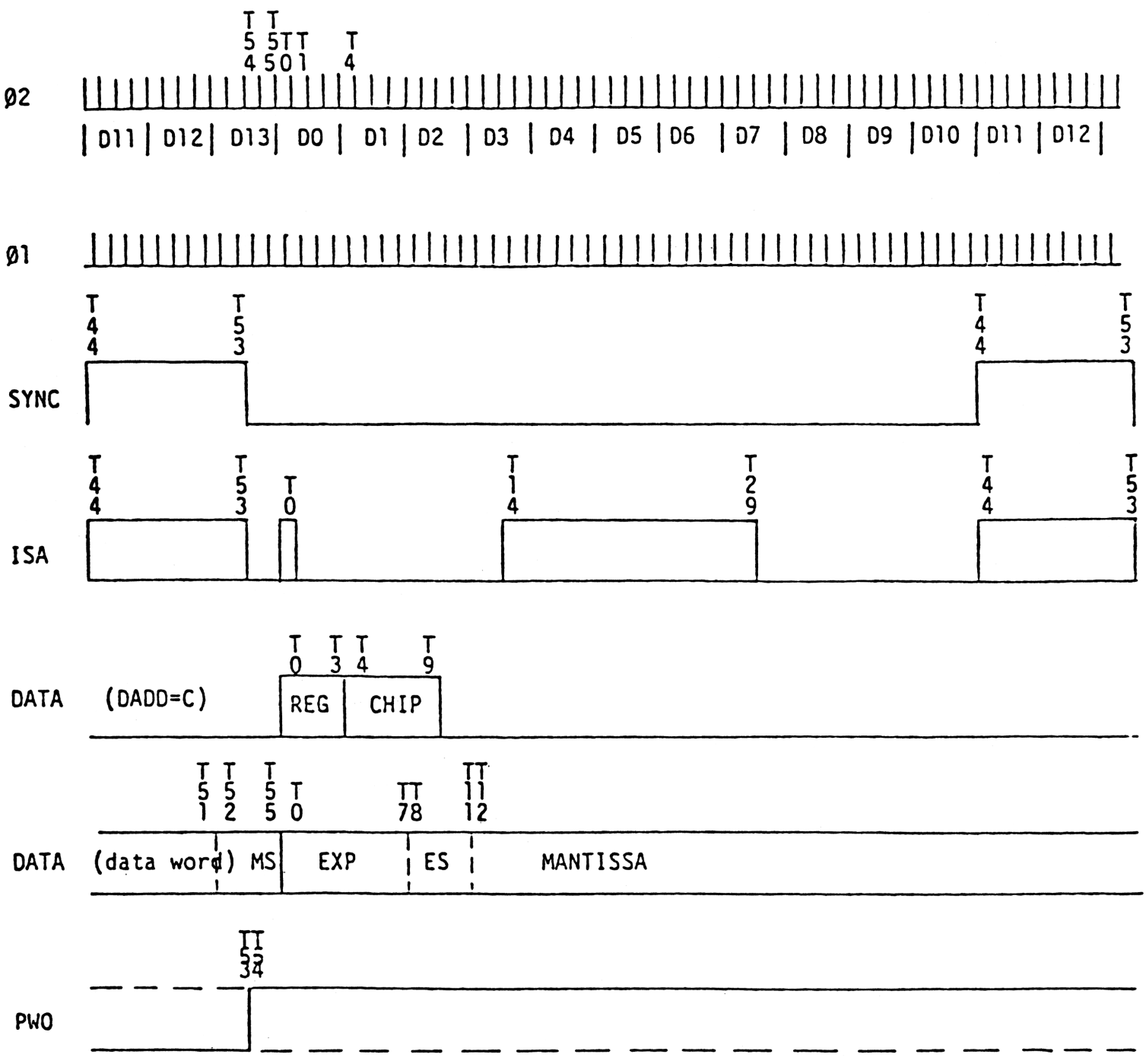
HEWLETT-PACKARD CO.



NUT SYSTEM CLOCK WAVEFORMS (FIGURE 2)

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL	STK NO 1LB6-4001
1LB6 ELECTRICAL SPECIFICATION	
BY CARL LANDSNESS	DATE 11-27-79
APPD	SHEET NO 11 OF 14
	DWG NO A-1LB6-4001-1



NUT SYSTEM TIMING

(Figure 3)

	SEE	SHEET 1		MODEL	STK NO. 1LB6-4001
				1LB6 ELECTRICAL SPECIFICATIONS	
				BY CARL LANDSNESS	DATE 11-27-79
LTR	P C NO	APPROVED	TE	APPD	SHEET NO. 12 OF 14

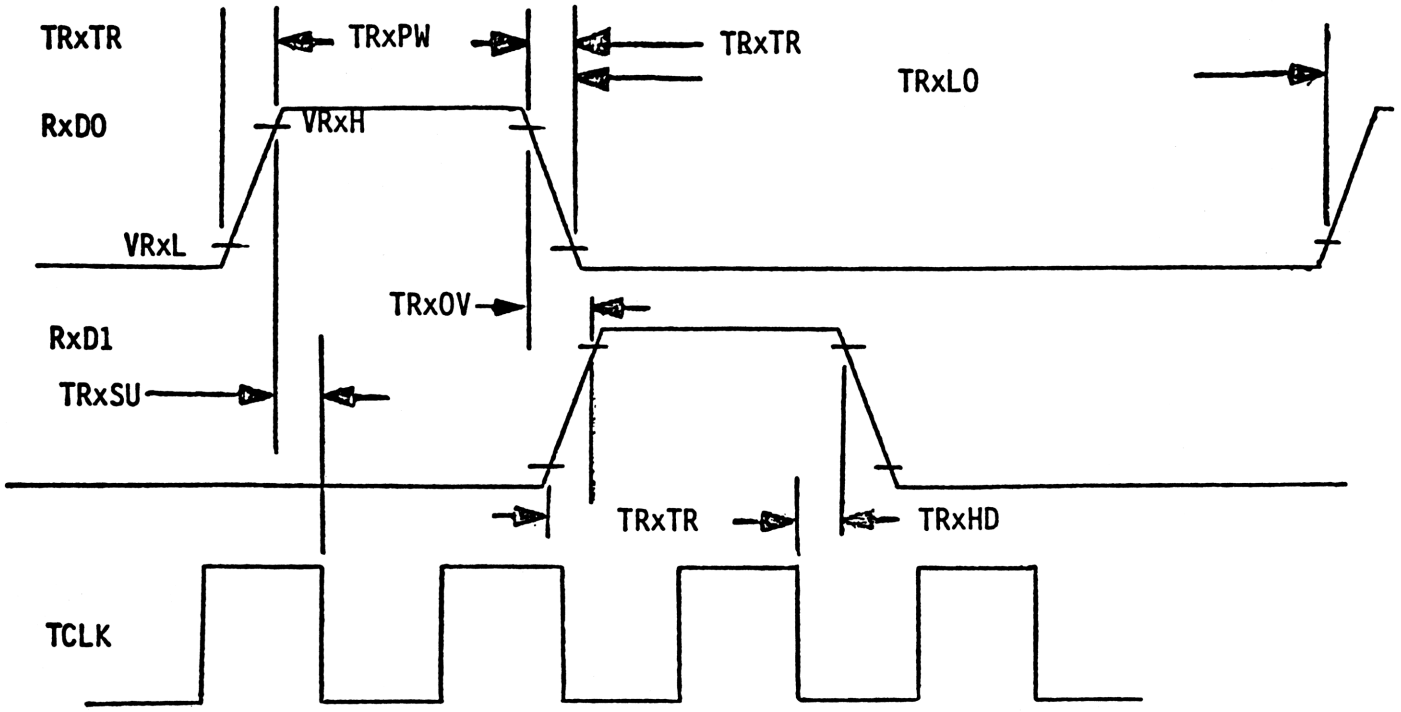


FIGURE 4 - PIL RECEIVER TIMING

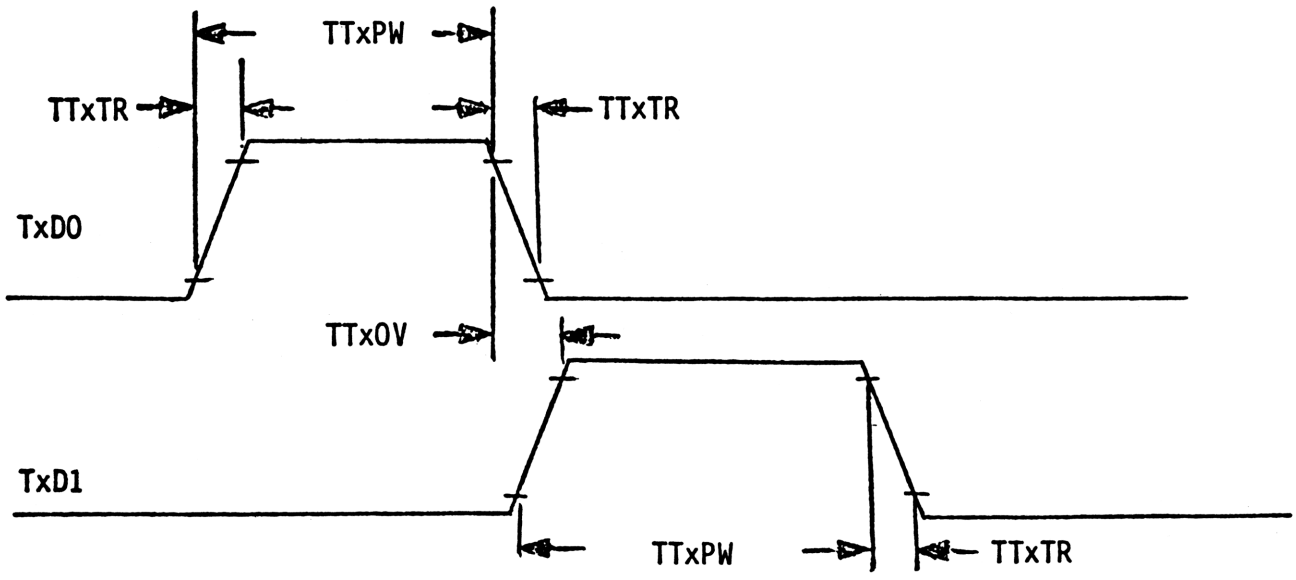
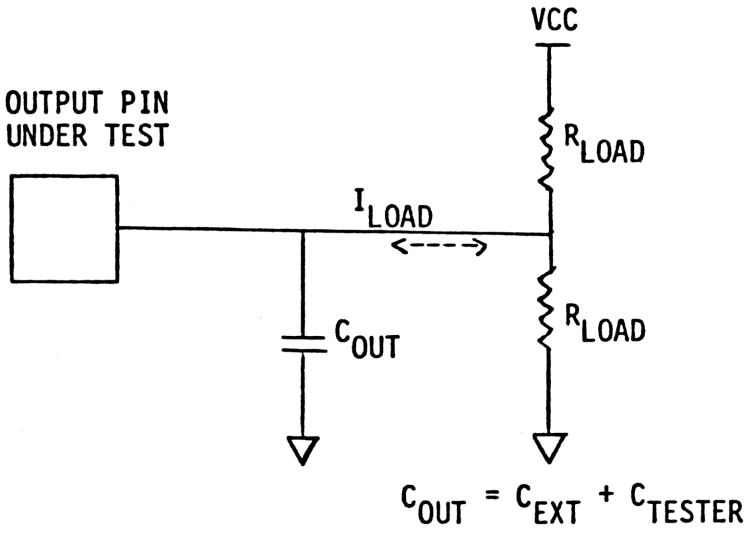


FIGURE 5 - PIL TRANSMITTER TIMING

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL	STK NO 1LB6-4001
1LB6 ELECTRICAL SPECIFICATION	
BY CARL LANDSNESS	DATE 11-27-79
APPD	SHEET NO 13 OF 14
SUPERSEDES	DWG NO A-1LB6-4001-1



TEST CONDITION FOR OUTPUT PINS
(Figure 4)

I_{LOAD} for specified C_{out} is 0. For testers with I_{LOAD} 0, modify C_{OUT} to C_{NEW} with the following formulas to compensate for the load. Also I_{LOAD} should maintain an equal sinking and sourcing level to make the modification valid.

$$I_{AVE} = C \frac{dV}{dT}$$ Basic formula

$$I_{AVE} = C_{OUT} \times \frac{VOH - VOL}{TDV}$$ Normal device drive

$$I_{LOAD} = C_{MOD} \times \frac{VOH - VOL}{TDV}$$ Calculate C_{MOD} for extra load current required for the device.

$$C_{NEW} = C_{OUT} - C_{MOD}$$

$$C_{NEW} = C_{OUT} - \frac{I_{LOAD} \times TDV}{VOH - VOL}$$ Modification formula

---

	SEE	SHEET 1		MODEL	STK NO 1LB6-4001
				1LB6 ELECTRICAL SPECIFICATIONS	
				BY CARL LANDSNESS	DATE 11-27-79
LTR	P C NO	APP'D	DATE	APPD	SHEET NO 14 OF 14
		REVISIONS		SUPERSEDES	DWG NO A-1LB6-4001-1

HEWLETT-PACKARD CO.

TIME MODULE (+CX)
BUS INFO

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As Issued	02-09-82	HK
	I operating = 1 mA		
	· 24 µA standby		

Model No.	Stock No. 1LF6-4001
Title 1LF6 Timer Chip Detailed Description	
Description	Date 9 February 1982
By Hank Koerner	Sheet No. 1 of 30
Supersedes	Drawing No. A-1LF6-9005-1

1LF6 Timer Chip

Detailed Description

Hank Koerner

HP Corvallis Division

2 February 1982

Table of Contents

Introduction — CHAPTER 1

The 1LF6 (codenamed Phineas) is a general purpose CMOS LSI clock-chip. It is designed for Corvallis Divison's 6u CMOSV process and it measures 150 x 215 mils. The design of the 1LF6 was begun in December of 1979 and characterization of the circuit was complete in the fall of 1981.

The 1LF6 was designed as a peripheral chip for the HP 41-C handheld calculator. Its design is intended to allow it to implement any timekeeping function consistent with the 41-C system design. Specifically, the 1LF6 has been incorporated into a product known as the 'Time Module' which provides the 41-C with a large number of timekeeping functions. Among them are a 100 hour stop watch with extensive split capability, a clock with or without constant display, a 300 year calendar, and a sophisticated alarm system that allows from simple audible alarms to interrupting program alarms.

The 41-C system communicates via a 56 bit serial bus. Generally, peripheral chips will transfer the contents of registers during communication with the 41-C. The timer chip has nine of these registers: six are dedicated to timekeeping tasks and three provide general information. The six timekeeping registers consist of two independent 56 bit clocks, two companion alarms (also 56 bits), a 20 bit interval timer, and a 13 bit register that allows adjustment to the chip's internal timebase. The remaining three registers consist of two general purpose scratch registers and a 13 bit status register which indicates the state of the circuit.

A 32768 Hz quartz crystal provides the accuracy and stability for the the timer chip's timebase. The timer chip contains prescalers that scale the input by a factor of 175/57344; this results in a 100 Hz signal that provides .01 second resolution to all the time keeping functions. 5600 Hz clocks gate the 56 bit registers so that they are recirculated once every .01 seconds whenever the 41-C system is inactive. However, when the system is active, registers are recirculated by the system clocks once every .01 second, allowing communication with the 41-C to proceed without interruption.

In addition to the above, the timer chip has features which enhance its flexibilty and capabilty. There is a low voltage detect circuit that is active when voltage is first applied or when

it drops below a level not sufficient to maintain proper circuit operation of the clocks. There are four pins that give direct control over the operation of the clocks. The alarms are brought to external pads so that they can be monitored directly. Finally, there is circuitry to aid in the test of the part; specifically, the test options make access to certain internal nodes and bypass the prescalers to allow easy synchronization with the part during test.

The remainder of this document delineates the operation, conditions for operation, and function of the 1LF6 timer chip. Examples are given of how specific features are used within the context of the Time Module. Chapter 2 covers the 41-C bus, bus requirements of the 1LF6, and bus functions implemented by the 1LF6. Chapter 3 describes the non-system signals required and created by the timer chip. The instruction set is discussed in Chapter 4, as is the Status Register in Chapter 5. Figures and Tables referenced throughout the text are assembled in Chapter 6. Other useful documents are:

1. HP Drawing Number E-1LF6-9001-50 : 1LF6 Logic Diagram
2. HP Drawing Number A-1LF6-9002-1 : 1LF6 Electrical Spec
3. HP Drawing Number A-82182-69901-1: Hybrid Electrical Spec

The electrical specifications define timing, level, and supply limits and requirements.

The Phineas Chip and the 41-C System Bus — CHAPTER 2

2.1 Background.

The 41-C system bus and calculator chip set have evolved from earlier calculator designs. In particular, the 41 CPU is a CMOS implementation, with enhancements, of the Woodstock PMOS CPU which in turn was a derivation from the classic line processor circuits (eg. the HP 35). This section is not meant to be an exhaustive discussion of the 41-C bus, but to supply general information to help the user understand operation of the Phineas chip.

2.2 Bit times, wordtimes, and the two phase clock system.

The fundamental timing unit is the bit time. All timing specifications are made in reference to this unit. The 41-C bus uses a two phase clock system; the two clocks are called Phase 1 (Ph1) and Phase 2 (Ph2). The bit time has the same period (Tp) as each of the clocks; its boundaries are coincident with the rising edge of Ph2. Nominally, the clocks have a pulse width (Tpw) equal to 2/8's of the period; the clock delay (Tcd) is equal to 1/8 of the period. Operating freqqency is the reciprocal of the bit time period. Output data valid time (Tdv) is measured from the trailing edge of Ph2; output one/zero transitions will be valid within this time. Input set up time (Tsu) is measured from the trailing edge of Ph1 toward the beginning of the bit time; input one/zero transitions will be valid within this time. See figure 1 for a simple diagram and refer to the 1LF6 Electrical Specification for more information on these parameters. The Phineas chip inputs Ph1 and Ph2, enables them with PWO, and uses the results as its own internal clocks.

The 41-C system bus operates on a 56 bit (bit time and bit are equivalent) cycle known as a wordtime. The 56 bit length allows for a 14 bcd digit word. The 41-C performs internal computations in floating point; the 14 digit computational word consists of a 2 digit exponent, a 1 digit exponent sign, a 10 digit mantissa, and a

1 digit mantissa sign. All registers and Ram used in the 41-C system are designed in 56.bit chunks to accomodate a 14 digit bcd word. Each bit in the word is numbered in ascending order, the first or least significant bit is bit 0 (synonymous terms are bit 0, bit time 0, time 0, and T0), the last or most significant bit is bit 55. Whenever data, address, or instruction are transmitted on the 41-C's serial bus, it is transmitted least significant bit first.

2.3 PWO and system enable.

PWO is the line that informs the system that the bus is active. Its leading edge serves as initial timing synchronization. Its inactive or low state is used to reset system counters and clamp dynamic nodes. See figure 2 for PWO timing. PWO is also used to enable the clocks. An integrated pull down of approximately 200K ohms stabilizes PWO while power is first applied. In the Time Module, the pull down helps insure that internal clocks are inactive (assuming the calculator is off) during insertion which often causes contact bounce. This in turn guarantees that important initialization status, such as the Power Up Status bit, are not accessed until all system lines are stable.

2.4 ISA: instructions and addresses on the 41-C bus.

During bit times 14 through 29 the CPU issues a 16 bit serial address on the instruction and address (ISA) line. A Rom connected to the system bus will decode the address and output a ten bit serial instruction. The instruction is output on ISA during bits 44 through 53. All circuits other than Roms input the 10 bit instructions; it is the means by which the CPU controls actions and supervises data communication with other chips in the system.

There are a class of instructions known as peripheral/data storage instructions; the opcodes are represented by xx50 and xx70 octal. These instructions control both Phineas and data storage (Ram). To avoid contention, Ram and peripheral chips each have separate chip enable instructions and addresses; when enabling one of these chips, care must be taken to insure one and only one device is enabled at the same time.

As stated above, instructions are output for 10 bits during the latter part of the wordtime. However, only one instruction per

wordtime is issued; therefore, instructions are valid for an entire wordtime and their validity begins two bits after Rom has output the last bit of the instruction. So, the statement 'at the end of an instruction' refers to the last bit of the word for which the instruction applied. See figure 3.

When the system bus is inactive - PWO low - ISA has another system function. It is pulled high by peripheral chips to request service. In the 41-C this may occur when the calculator is fully off; before the CPU can respond, the switching power supply is started and the supply voltage Vcc is stepped up to normal operating levels. This process may take 50 mS or more. In any case, Phineas will drive ISA high until the system acknowledges its service request (signified by bringing PWO high). The timer chip will then tristate its ISA driver and drive Flag 13. Read the sction below on FLAG.

2.5 SYNC: periodic synchronization.

SYNC is a 10 bit wide pulse output by the CPU. The pulse occurs at instruction time (bit times 44 through 53). It has a number of purposes; two are discussed here. The first use of SYNC is to provide a periodic synchronizing signal to the rest of the system. Use of SYNC in this way allows recovery from disturbances causing temporary loss of communication. The second use of SYNC is to enable instructions appearing on ISA. The CPU will suppress SYNC for one word time when it executing a 16 bit goto or gosub; the data output on ISA while SYNC is suppressed is address, not instruction, and should not be decoded by chips other than the CPU. Phineas inputs SYNC and implements both functions stated above.

2.6 DATA: data transfer in the 41-C.

DATA is the line over which all data transfer takes place, data being distinct from either addresses or instructions. Normally, the CPU drives DATA with the contents of one of its registers; if instructed a peripheral device can buffer this data. However, a series of instructions may be issued, commanding the peripheral device to output its own data. At that time, the CPU tristates its DATA driver and inputs the information appearing on the DATA line.

Data transfer always occurs 56 bits at a time. The CPU always

outputs a full data word. If fewer than 56 bits are required by a peripheral, it simply ignors the extra bits. Similarly, the CPU always inputs a full data word. A peripheral device should drive DATA to a valid logic level for the entire word even if only a portion contains real data. Data transfer occurs with least significant bit first, most significant last. With bcd data this translates to least significant digit first, etc. A digit or digit time is defined as the four bits comprising a bcd digit. A word is devided into 14 digits in aseending order. See figure 3.

2.7 FLAG and system interrupt.

FLAG provides peripheral devices with a means of requesting service from and/or indicating status to the CPU. The protocol of FLAG has changed since the original design of the 41-C to allow greater flexibility and usage. There are 14 flags available; each is time multiplexed onto the FLAG line. Each flag is coincident with its corresponding digit time, ie. flag 8 occurs simultaneously with digit 8. To indicate a valid flag, a device should drive FLAG low at the appropriate time and then drive it high when it is done. The CPU has a high impedance pull up which can maintain state, but not change it. See figure 4 for FLAG timing. All flags but Flag 13 should be driven by a device only if that device is selected. This convention promotes maximum use of FLAG without contention.

Flag 13 is the system service request flag. This flag is checked at the end of every keystroke and program step. A peripheral device requesting service should drive this flag. Since there can be more than one device requiring service, Flag 13 requires a 'wired or' convention. That is, all chips with valid flags should pull flag low, but false flags must not pull it high. As before, FLAG should be returned to its inactive state at the end of Flag 13 time.

Phineas uses Flags 12 and 13. Flag 13, as stated above, is driven to request service whenever an alarm condition exists. Flag 12 is driven when the above condition is true and Phineas is enabled. This second flag reduces the service response time in a loaded system. Additional status is obtained by directly interrogating the chip.

2.8 Vcc and Gnd: system power supply.

The Phineas chip has two power supply connections, Vcc the positive lead, and Gnd the negative lead. All circuitry is run from this voltage, and all inputs and outputs are referenced to this level. See the 1LF6 Electrical Specifications, HP drawing number A-1LF6-9002-1, for operating limits on the supply voltage and input and output signals.

Non-system lines on the Phineas chip.	CHAPTER 3

There are eight pins on Phineas in addition to those described above. These pins are either necessary for correct the operation of the chip or provide special features not found within the 41-C system bus definition.

3.1 Osc In and Osc Out.

These two pads connect the chip's internal oscillator to the outside world. The 'Pierce' oscillator has been designed to accept a standard 32768 Hz watch crystal with a Cload of 12.5 pF (eg. NDK's MU 206). Each pad is connected to an integrated 22 pF phase shift capacitor to ground. P-Well source resistors of approximately 250K ohms have also been integrated to reduce power consumption and increase stability due to power supply variations. Osc Out, the output of the oscillator, is input to a Schmitt trigger which has been optimized for wide supply ranges, low power operation, and greatly reduced input levels. A high impedance bias resistor of 22M ohms is connected to both pads in parallel with the crystal. Refer to the 1LF6 logic diagram for a complete schematic of the oscillator. Typical performance of the oscillator at room temperature and with a 5 volt supply voltage is +- 0.5 seconds per day or approximately +- 6 ppm error using the crystal mentioned above. Supply variations of +- 2 volts introduce additional error of +- 5 to 10 ppm.

3.2 Alarm A and B.

The alarm pads serve two functions: 1. they provide external connections for Phineas' internal alarms, and 2. they serve as test pads. There are two clock registers, two alarm registers, and two alarms on the Phineas chip. This allows two completely independent timekeeping functions. Alarms become valid when the alarm register matches the clock register. The alarm pads will reflect the state of the alarms with the appropriate control status

(i.e. TESTA = TESTB = 0). In the Time Module the alarms will remain valid for only the time it takes the 41-C to service them; this interval is 1 - 50 mS in a normal system.

During functional testing of Phineas, the control status TESTA and TESTB is altered to bring certain internal nodes to the Alarm pads. This feature greatly facilitates verification of several blocks of logic including the prescalers and the Accuracy Factor. Read the sections on TESTA and TESTB for more information on the test facilities. In the Time Module the internal alarms are always brought out to the alarm pads. The alarm pads are inverter outputs with roughly half the drive capability of the DATA driver.

3.3 Start and Stop pins.

The four Start and Stop pins provide remote control over each of the clocks on the chip, one set of control pins for each clock. All pins assume positive true logic. Each set of inputs is connected to an asynchronous state machine that has several purposes. 1. The inputs are debounced for at least .01 seconds; the debounce period may not be long enough for noisy inputs. 2. The state machine insures operation of start/stop instructions even when stuck at zero/one faults exist on the start/stop pins. 3. A toggle function is implemented when stop and start are wired together allowing single pushbutton control of the clocks. Pulling Start A high sets CKAEN which starts Clock A. Pulling Stop A high clears CKAEN which stops Clock A. When Start A and Stop A are connected pulling them high results in the toggle function; pulling them high once will start Clock A, pulling them high again will stop Clock A. Start and Stop B have a similar effect on Clock B. The start and stop pins have integrated poly resistor pull downs of about 2.5K ohms connected to each pad.

The Phineas Instruction Set — CHAPTER 4

Phineas responds to 24 instructions. Twenty one of these are peripheral instructions, either type xx50 or xx70. The peripheral instructions fall into two categories, data transfer and control. Of the three non-peripheral or general system instructions, two are enable instructions and one is a power off instruction. Table 1 presents a summary of the instruction set. The instructions described below are followed by their octal representation in parenthesis.

4.1 Enable Instructions: CPFAD (1760) and CDADD (1160).

CPFAD (cpu C register to PeriFeral ADdress) is the instruction that enables and disables the Phineas chip as well as other peripheral chips. CPFAD enables Phineas in the following sequence: 1760 octal is output onto ISA at instruction time followed two bit times later by Phineas' chip address, FB hex, least significant bit first, at bit times 0 through 7 (chip address time) on DATA. This sequence sets the chip enable flip-flop; peripheral instructions are ignored unless chip enable is set. Chip enable is reset when CPFAD is issued with an address other than the Phineas address.

CDADD (cpu C register to Data storage ADDress) is the system instruction used to enable data storage chips or Ram. Because Ram and peripheral chips like Phineas share the same data transfer instructions, only one chip at a time may be enabled to avoid contention or 'bus fighting'. To insure that Phineas is never enabled at the same time as data storage, the CDADD instruction will reset chip enable regardless of the data appearing at chip address time.

4.2 The PWO low instruction, PWOFF (140).

PWOFF (PWo OFF) instructs the system that PWO will be driven low during the current wordtime (the wordtime directly after PWOFF

is sent) at bit time 54. See figure 6 for PWOFF timing. Phineas increments its clock registers every .01 seconds asynchronously with respect to system timing. However, when the system is active, the increment cycles, though triggered every .01 seconds, will be synchronized with word time boundaries. This feature allows simultaneous data transfer and incrementing. If the .01 second trigger occurs after PWOFF issues, incrementing takes place at once rather than waiting for the next word boundary to avoid losing an increment cycle.

4.3 Peripheral Instructions, xx50 and xx70.

There are thirty two peripheral instructions which may be used by all peripherals. Generally, the xx50 instructions are used to send data to the peripheral or inact a control function. xx70 instructions are used to receive data from the peripherals; in any case, an xx70 instruction causes the 41-C CPU to tristate its DATA driver and buffer into its C register whatever appears on DATA during this instruction. The xx represents the octal numbers 00 through 17.

Phineas uses twenty one peripheral instructions. These are broken into twelve data transfer and nine control instructions. The data transfer instructions access registers on Phineas, the control instructions either manipulate status on Phineas or command it to take an action.

4.3.1 Data transfer instructions.

4.3.1.1 Write Clock (50)

Causes the currently accessed clock register to buffer 56 bits appearing on DATA during this instruction. Read the section on CKAEN for more information on clock registers.

4.3.1.2 Read Clock (70)

Causes the currently accessed clock register to output its contents, least significant bit first, onto DATA during this instruction.

4.3.1.3 Write and Correct (150)

Causes the same action as Write Clock above. In addition it commands the correction circuitry to either reset or to add two to the clock on the next increment cycle. See Read and Hold below.

4.3.1.4 Read and Hold (170)

Causes the same action as Read Clock above. In addition it initiates a correct cycle. This feature is used when a time is to be read, modified, and restored to Phineas without loss of accuracy (e.g. when adjusting for daylight savings time). The correct circuitry allows the user .01 seconds to modify and restore the time. If an increment cycle occurs during this time, the correct circuitry compensates by adding two to the time on the next increment cycle. If no increment occurs during the modify/restore process the correct circuitry is reset. If modify/restore exceeds .01 seconds then two is added on the next increment cycle but accuracy cannot be guaranteed. In a normal 41-C there are at least 67 word times per .01 second period. The Read and Hold instruction initiates the correct cycle and it is concluded by Write and Correct. The correct state machine will not be reset to its at rest state unless a Write and Correct follows a Read and Hold.

4.3.1.5 Write Alarm (250)

Causes the currently accessed alarm register to buffer the 56 bits appearing on DATA during this instruction. Read the section on ALAEN for more information on alarm registers.

4.3.1.6 Read Alarm (270)

Causes the currently accessed alarm register to output its contents, least significant bit first, onto DATA during this instruction.

4.3.1.7 Write Status (350)

If the pointer is on A, this instruction causes the status register to be written. Actually, only the first six of the thirteen status bits can be written and these only to a zero level. To accomplish this the user must drive DATA low for the first six least significant bits of a word; all other bits are ignored during this instruction. Internal hardware sets these bits and the user resets them. Refer to the following chapter on the Status Register.

4.3.1.8 Read Status (370)

If the pointer is on A, this instruction causes the status register to be read. The status register ouputs its thirteen bits, least significant bit first, and then drives DATA low for the remaining 43 bit times.

4.3.1.9 Write Accuracy Factor (350)

If the pointer is on B, this instruction writes DATA to the Accuracy Factor. Note that the Accuracy Factor buffers only data appearing at bit times 4 through 16. The Accuracy Factor is a thirteen bit register that controls modification of Phineas' internal 10240 Hz timebase. The first twelve bits form three bcd digits which represent an interval in the form of +- nn.n seconds. This interval controls how often pulses are added or subtracted from the 10240 Hz reference. The thirteenth bit is a sign bit; a zero means pulses are added to the reference, a one means they are subtracted. For example, an accuracy factor of +00.1 causes a pulse to be added 10 times a second; therefore the 10240 Hz reference becomes 10250 Hz. The error of a product using the Phineas chip can be corrected through use of the Accuracy Factor. The following formulas relate the error to the Accuracy Factor setting.

$$\text{Intial Error} = 10^6 * \frac{(T_{indicated} - T_{actual})}{(T_{actual} - T_{initial})} = ERR_{ppm}$$

$$AF = \frac{-10^6}{10240 * ERR_{ppm}}$$

$$\text{Initial Frequency} = 10240 + (ERR_{ppm} * .0124)\ Hz$$

$$\text{Final Frequency} = \text{Initial Frequency} + 1/AF\ Hz$$

(AF rounded to one significant figure)

$$\text{Final } ERR_{ppm} = 10^6 * \frac{(\text{Final Frequency} - 10240)}{10240}$$

$$ERR_{spd} = ERR_{ppm} * .0864$$

where $T_{indicated}$ = time indicated by the Time Module
T_{actual} = the correct time when the error is measured
$T_{initial}$ = the time when time is first set

ERRppm = Error in parts per million
ERRspd = Error in seconds per day
AF = Accuracy Factor

4.3.1.10 Read Accuracy Factor (370)

If the pointer is on B, this instruction causes the Accuracy Factor to output its contents onto DATA at bit times 4 through 16, least significant bit first, sign bit last. DATA is driven low at all other times during this word.

4.3.1.11 Write Scratch (450)

Causes the currently accessed scratch register to buffer the 56 bits appearing on DATA during this instruction. There are two general purpose 56 bit scratch registers that are called A and B; access is controlled by the pointer. The intent of these registers is to provide the user with on chip storage for important status or variables.

4.3.1.12 Read Scratch (470)

Causes the currently accessed scratch register to output its contents, least significant bit first, onto DATA during this instruction.

4.3.1.13 Write Interval Timer and Start (550)

The Interval Timer is a five bcd digit register that may be used to create periodic alarms ranging from .01 to 999.99 seconds. The Write Interval Timer and Start instruction causes the Interval Timer to buffer the least significant five digits appearing on DATA during this instruction as its terminal count and to enable its interval counter by setting ITEN (see the section below on ITEN). The interval counter is cleared and started; the counter increments from zero towards the terminal count. When the terminal count is reached, the counter is reset and the process begins again. The terminal count state sets the Decrement Through Zero Interval Timer (DTZIT) status bit which will cause the Phineas chip to request service regardless of whether the bus is active. DTZIT will remain set until cleared by a Write Status instruction. The Interval Timer is used by the Time Module to generate service requests for its continuous display 'CLOCK' function; in this case the Interval Timer is set to either 1 second or 1 minute and the periodic service requests enable the Time Module to update the 41-C's display like a digital clock.

4.3.1.14 Read Interval Timer (570)

Causes the Interval Timer to be read. The Interval Timer outputs its 20 bits, least significant bit first, onto DATA and drives DATA low during the remaining 36 bit times.

4.3.2 Control Instructions.

4.3.2.1 Stop Interval Timer (750)

This instruction clears the ITEN status bit; ITEN is set only by the instruction Write Interval Timer and Start. Clearing ITEN disables the Interval Timer counter; it does not reset the counter or clear DTZIT.

4.3.2.2 Clear Test Mode (1050)

Causes the currently accessed Test Mode flip-flop to be cleared at the end of this instruction.

4.3.2.3 Set Test Mode (1150)

There are two Test Mode flip-flops that are called TESTA and TESTB; access is controlled by the pointer. The Test Mode bits are cleared for normal operation; setting Test Mode invokes special states that aid in testing the part. Test featurs are detailed below in the section on TESTA and TESTB.

4.3.2.4 Disable Alarm (1250)

Clears the currently accessed alarm enable status bit at the end of this instruction. The alarm enable status bit controls the comparison of the alarm register with its corresponding clock register. If alarm enable is set, the compare is enabled; if clear, the compare is inhibited. Disabling an alarm will gate off all clocks to the register; consequently, there is a slight decrease in power consumption. This instruction does not clear current alarms, it inhibits or disarms future alarms. See the section describing ALAEN for more detail.

4.3.2.5 Enable Alarm (1350)

Sets the currently accessed alarm enable status bit at the end of this instruction. This will arm future alarms, but will not set current alarms.

4.3.2.6 Stop Clock (1450)

Clears the currently accessed clock enable status bit at the end of this instruction. The clock enable bit determines the state of the clock. If the clock enable is set, the clock is on and incrementing; if clear, the clock is off. When clear, incrementing and alarm comparison are inhibited, and all clocks to the register are gated off, resulting in a slight decrease in power consumption.

4.3.2.7 Start Clock (1550)

Sets the currently accessed clock enable status bit at the end of this instruction. Start Clock enables the clock's incrementer.

4.3.2.8 Set Pointer to B (1650)

Sets the pointer flip-flop to the B state. Phineas has two clock registers, two alarm registers, and two scratch registers. There is one set of instructions to communicate with two sets of registers. To access a specific register, the user must indicate which set of registers he wants to communicate with. He does this by manipulating the pointer. To communicate with Alarm B, the pointer is set to B. To read or write the Status Register, the pointer must be set to A. Changing the state of the pointer simply redirects instructions to the register specified; it does not effect the machine in any other way.

4.3.2.9 Set Pointer to A (1750)

Sets the pointer flip-flop to the A state at the end of this instruction. See the paragraph above for additional information.

The Status Register — CHAPTER 5

The Status Register, a register of thirteen status bits, indicates to the user the state of correspooding hardware. Each status bit is physically located near the hardware it represents. Because of this, the register is actually a multiplexer which merges the bits onto a common line. However, representing the status bits as a register provides a straightforward means of describing their function.

The Status Register is accessed by Read and Write Status instructions. Note that the pointer must be set to A since these instructions share the same opcode as the Read/Write Accuracy Factor instructions. Refer to the paragraphs above describing the instructions. A read will caese the Status Register to output its 13 bits onto DATA beginning at T0. DATA is driven low for the remaining 43 bit times.

Writing the Status Register has a different effect than writing other registers. The Status Register contains two types of status, alarm and hardware status. Alarm status comprises the first six bits in the Status Register; these bits, when set, will generate service requests. The only way to clear one of these bits is by writing a zero to its bit locaton during a Write Status instruction. Alarm status is set only by the internal hardware of the timer chip. For example, the status bit ALMA is set only when a valid compare between Clock A and Alarm A occurs. The remaining seven status bits constitute the Hardware status. Hardware status informs the user how the part is set up; these bits are set and cleared only by the control instructions. Therefore, writing status resets only the first six bits in the register and has no other effect.

The following paragraphs describe the function of each status bit in detail. Note that positive true logic applies to each status bit. For a summary, please refer to table 2.

5.1 Alarm status, bits 0 through 5.

There are six alarm status bits; when set, each of these bits except the PUS bit will reqaest service by either pulling ISA high

when the system is inactive or pulling FLAG low when the system is active.

5.1.1 ALMA (ALarm A)

This bit is set when Alarm A matches Clock A. See ALAEN for more detail.

5.1.2 DTZA (Decrement Through Zero A)

This bit is set when Clock A overflows while incrementing. When this occurs, the register rolls over to all zeros and continues incrementing. If a negative ten's complement number is stored in the clock register, it will be incremented towards zero. When the count hits zero, the clock register overflows setting DTZA.

5.1.3 ALMB (ALarm B)

This bit is set when Alarm B matches Clock B. See ALAEN for more detail.

5.1.4 DTZB (Decrement Through Zero B)

This bit is set when Clock B overflows while incrementing. See the description for DTZA for more details.

5.1.5 DTZIT (Decrement Through Zero Interval Timer)

This bit is set when the Interval Timer reaches its terminal count. Note that the terminal count register is compared bit for bit with the interval counter which is incremented as bcd; the terminal count should also be stored as a bcd number. See ITEN for more detail.

5.1.6 PUS (Power Up Status)

This bit is set when Phineas first has power applied or whenever the supply voltage falls below a level sufficient to sustain proper circuit operation (characterization indicates that the average trip

voltage is 2.5 V +- 0.3 over a 0 to 65 degree C temperature range). Note that this bit does not generate a service request. PUS is used to inform the user that there may be meaningless data in the registers. In the Time Module the chip is initialized if PUS is set; the time and date are reset to the beginning of the calendar, (12:00 AM, January 1, 1900) and all other status is cleared. PUS uses a two threshold detection scheme coupled to a ratioed flip-flop designed to power up in a known state. Refer to the 1LF6 logic diagram for a full PUS circuit schematic. The PUS detection circuit is clocked to reduce power consumption; the duty cycle is 3.12% and the circuit is gated on for 15.3 uS. The average current drain at 6.5 V is 0.1 to 0.5 uA. When PUS is set, service requests via the ISA and FLAG lines are inhibited. This prevents the Time Module from disrupting the system when it is first inserted into a calculator.

5.2 Hardware Status, bits 6 through 12.

The hardware status bits reflect the state of the Phineas chip. Read Status interrogates the these bits, Write Status has no effect. Hardware status is set and cleared by each of the respective set and clear instructions. Refer to the chapter above on the Instruction Set.

5.2.1 CKAEN (ClocK A ENable)

CKAEN indicates whether Clock A is enabled and incrementing. Each of the two clock registers consists of 56 bits or 14 bcd digits. Every .01 seconds the registers, if enabled, are recirculated through a serial incrementer. The registers are bcd corrected every increment cycle. If non-bcd is stored to the register, it will be converted to bcd on the first increment cycle. When the system bus is dormant, the clock registers (and all timekeeping registers) are recirculated continuously at a 5600 Hz clock frequency, each increment cycle taking .01 seconds. When the system bus is active, the clock registers are recirculated at system clock frequency, 340 to 380K Hz. Any timekeeping registers may be accessed at any time without having to wait for an increment cycle. The increment process, as far as data transfer is concerned, is completely transparent to the user. An increment cycle lasts approximately 165 uS. The clock registers are static during the remainder of the .01 second period. The increment cycle is initiated at T0, the beginning of a wordtime, so that data transfers between Phineas and the CPU proceed without interruption. There are two asynchronous state machines that implement the clock switching function and the increment cycle synchronization

function; they are called the Clock Enable state machine and the Update In Progress state machine respectively.

5.2.2 CKBEN (ClocK B ENable)

CKBEN indicates whether Clock B is enabled and incrementing. Please read the paragraphs describing CKAEN for more detail.

5.2.3 ALAEN (ALarm A ENable)

ALAEN indicates whether Alarm A is enabled and sequentially compared to Clock A. There are two 56 bit alarm registers, each is linked to a specific clock register. The alarms are used to store 14 bcd digit times which are compared bit for bit with their respective clock register. If the alarm and clock match and the alarm register is enabled, then the alarm bit is set. Note that a non-bcd alarm cannot result in a valid compare with a clock register. When an alarm is disabled, the clocks to that register are inhibited minimizing power consumption by that section of logic.

5.2.4 ALBEN (ALarm B ENable)

ALBEN indicates whether Alarm B is enabled and sequentially compared to Clock B. Please read the paragraphs describing ALAEN for more detail.

5.2.5 ITEN (Interval Timer ENable)

ITEN indicates whether the Interval Timer is enabled and counting up towards the terminal count. The Interval Timer, a 20 bit, 5 bcd digit circuit, consists of two main components, a terminal count register and an interval counter. The terminal count is the register accessed by Read/Write Interval Timer instructions. It holds the number compared to the interval counter. When the terminal count matches the interval counter, DTZIT is set, and the interval counter is reset to zero and again counts up towards the terminal count. In function, the terminal count register is very similar to an alarm. Note that a non-bcd number stored as the terminal count will prevent the interval counter from matching.

5.2.6 TESTA

The two test mode status bits, TESTA and TESTB, serve as controls to test options on Phineas. These bits control the signals output to the Alarm A and B pads, and control bypassing input frequency prescalers. For a summary refer to the test opton truth table, table 3. In normal operation internal Alarm A and Alarm B are output to their respective pads and the input frequency is fully prescaled. When TESTA is set and TESTB is clear the logical 'and' of ITCMP and IT55 is output to Alarm A. 100Hz, the final output of the prescalers, is routed to Alarm B. This test mode does not bypass any prescalers. ITCMP*IT55 is a signal that is active during the last bit of an increment cycle if the terminal count register matches the interval counter (both are part of the Interval Timer). The duration of this pulse is one bit time when the system is active and approximately 178 uS when the system is inactive (assuming the input frequency is 32768 Hz). The period, on the average, is the same as the interval stored as the terminal count; jitter is induced into the period because the circuits used in the prescalers generate short term assymetrical waveforms. 100Hz triggers the entire increment cycle process. Its pulse width is the same as ITCMP*IT55 and its period on the average is .01 seconds, degraded also by the jitter phenomena outlined above.

When TESTB is set and TESTA is a 'don't care', mode #832, an Accuracy Factor output, is routed to Alarm A. 100Hz is again output to Alarm B, but since the prescalers are bypassed in this mode its frequency is the input frequency devided by 112. #832 is the signal that controls adding or subtracting a pulse from the 10240 Hz timebase. Nominally #832 has a pulse width of ten input cycles and a period of sixteen input cycles. However, as a pulse is added (subtracted) the pulse width of #832 varies to 12 (8) input cycles; the period remains the same. This will occur at an interval equal to that stored in the Accuracy Factor.

The input frequency is normally 32768 Hz and the prescalers devide it to create the signals 5600Hz and 100Hz. 5600Hz is used to clock the 56 bit timekeeping registers when the system bus is inactive. 100Hz is used to initiate the increment cycle. With all prescalers in place, the input is multiplied by the constant 175/57344 (multiplying 32768 by this constant results in 100). This constant is derived from several prescaler stages and the following symbolically represents the sequence of each stage: Finput x 1/2 x 5/8 x 5/8 x 7/8 x 1/56 = 100Hz. A synchronous counter, combinational feedback logic, and clocked decoded outputs comprise each stage. The output from the previous stage is rippled to its succesor. The 5/8 and 7/8 stages are mod 8 counters whose decoded outputs are pulses that have the same pulse width as as the numerators of the factors describing the stages. When these pulses

are used to generate the ripple outputs the resulting waveform, in the case of the 5/8 stage, is a pulse train of 5 pulses followed by 3 nulls. Two of these stages cascaded create short term assymetries that contribute to jitter. The absolute error caused by the jitter does not exceed +- 2.34% of .01 seconds and the average approaches zero in an interval as short as 1400 input cycles.

5.2.7 TESTB

For a description of TESTB read the paragraphs above in the section on TESTA.

Figures and Tables.	CHAPTER 6

The following figures and tables are those that have been refered to throughout the text of this description. In addition, a block diagram and 20x metal mask photo have been included for completeness. For detailed schematics, refer to the documents listed in Chapter 1. For more information on 41-C bus signals, refer to appropriate circuit descriptions and the other system documentation.

6.1 Table 1: The Phineas Instruction Set Summary.

Instruction	Octal	Description
Write Clock	0050	Data xfered from CPU to clock register.
Read Clock	0070	Data xfered from clock register to CPU.
Write Clock & Correct	0150	Same as above. Terminates correct cycle.
Read Clock & Hold	0170	Same as above. Initiates correct cycle.
Write Alarm	0250	Data xfered from CPU to alarm register.
Read Alarm	0270	Data xfered from alarm register to CPU.
Write Status	0350	Writing 0's clears alarm status. Ptr = A.
Read Status	0370	Interrogates state of chip. Ptr = A.
Write Accuracy Factr.	0350	Bits 4 thru 12 map to/from nn.n of AF. Bit
Read Accuracy Factor	0370	16 is sign bit: 0 = +, 1 = -. Ptr = B.
Write Scratch	0450	Data xfered from CPU to scratch register.
Read Scratch	0470	Data xfered from scratch register to CPU.
Write Int Tmr & Start	0550	CPU writes and start Interval Timer.
Read Int Tmr	0570	CPU reads Interval Timer. Pointer = x.
Stop Int Tmr	0750	Disables Interval Timer increment.
Clear Test Mode	1050	Clears/Sets the Test Mode flip-flop.
Set Test Mode	1150	Nomal mode, TESTA = TESTB = 0. Normal
Disable Alarm	1250	Inhibits but does not clear alarms.
Enable Alarm	1350	Arms but does not set alarms.
Stop Clock	1450	Disables clock incrementer.
Start Clock	1550	Enables clock incrementer.
Set Pointer to B	1650	Enables communication w/ B registers.
Set Pointer to A	1750	Enables communication w/ A registers.
Enable Peripheral	1760	Sets chip enable f-f w/ correct address.
Phineas Address = FB		Clears chip enable w/ non-Phineas address.
Enable Data Storage	1160	Clears chip enable regardless of address.
PWO Off	0140	System bus off command.

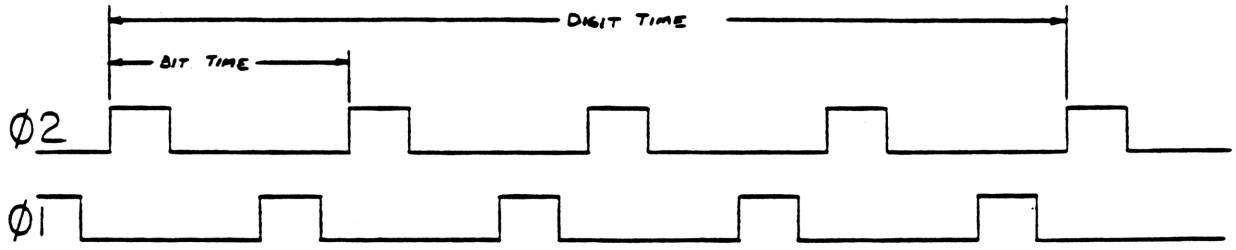
5.2 Table 2: Phineas Status Bit Assignment

Status Bit	No.	u-code set	Description
ALMA	0	no	A valid compare of Alarm A w/ Clock A sets this bit high.
DTZA	1	no	Set on overflow (or decrement of 10's complement) of Clock A.
ALMB	2	no	Set on valid compare of Alarm B w/ Clock B.
DTZB	3	no	Set on overflow of Clock B.
DTZIT	4	no	Set by terminal count state of Interval Timer.
PUS	5	no	Power Up Status: set when Vcc 1st applied or when Vcc falls below Vsustain.
CKAEN	6	yes	Enables Clock A incrementers.
CKBEN	7	yes	Enables Clock B incrementers.
ALAEN	8	yes	Enables comparator logic between Alarm A and Clock A.
ALBEN	9	yes	Enables comparator logic between Alarm B and Clock B.
ITEN	10	yes	Enables Interval Timer incrementing and comparator logic.
TESTA	11	yes	Enables Test A Mode.
TESTB	12	yes	Enables Test B Mode.

6.3 Table 3: Test Options

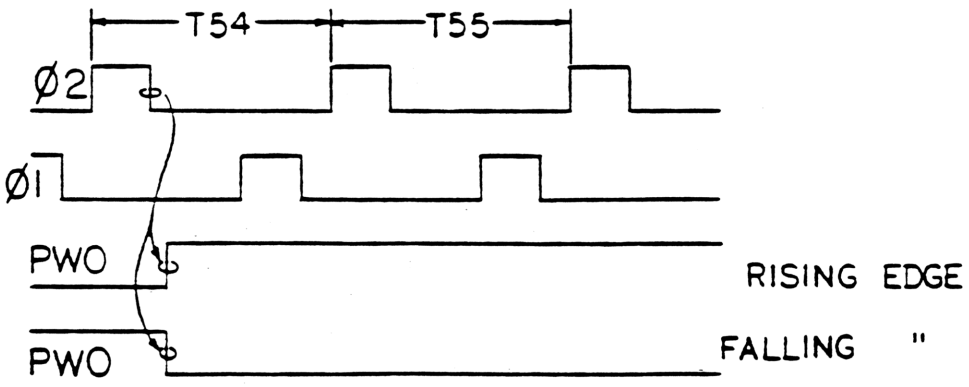
TESTB	TESTA	Alarm A	Alarm B	Freq of 100Hz
0	0	ALMA	ALMB	Finput * (175/57344)
0	1	ITCMP*IT55	100Hz	Finput * (175/57344)
1	0	832	100Hz	Finput * (1/112)
1	1	832	100Hz	Finput * (1/112)

6.4 Figure 1: Phineas Clocks.



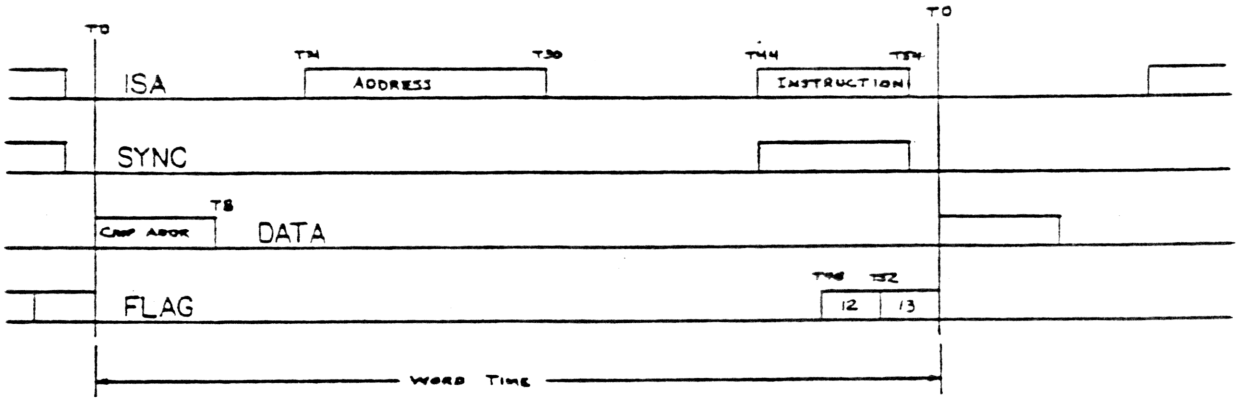
PHINEAS CLOCKS

6.5 Figure 2: PWO Timing.



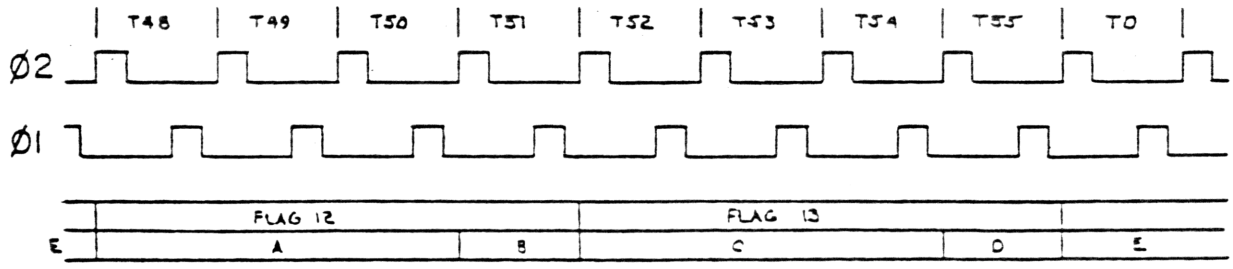
PWO TIMING SEQUENCE

6.6 Figure 3: 41-C System Signals.



SIGNAL RELATIONSHIPS

6.7 Figure 4: FLAG Timing.



A: If $(\overline{CE} + \overline{PWO} + PUS) = 1$ then A = Hi Z,
If $(\overline{CE} + \overline{PWO} + PUS) = 0$ AND ALMSTAT = 1, then A = 0; AND ALMSTAT = 1, then A = 1

B: If $(\overline{CE} + \overline{PWO} + PUS) = 1$ then B = Hi Z,
If $(\overline{CE} + \overline{PWO} + PUS) = 0$ then B = 1

C: If $(\overline{PWO} + PUS) = 1$ then C = Hi-Z
If $(\overline{PWO} + PUS) = 0$ AND ALMSTAT = 1 then C = 0; AND ALMSTAT = 0, then C = Hi Z

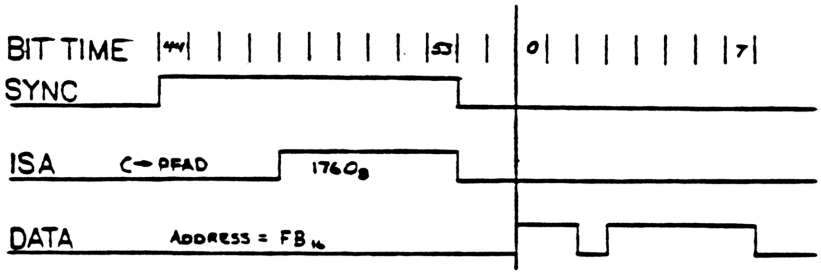
D: If $(\overline{PWO} + PUS) = 1$ then D = Hi-Z
If $(\overline{PWO} + PUS) = 0$ then D = 1

E: Hi Z

PHINEAS FLAGS

HK
4-29-81

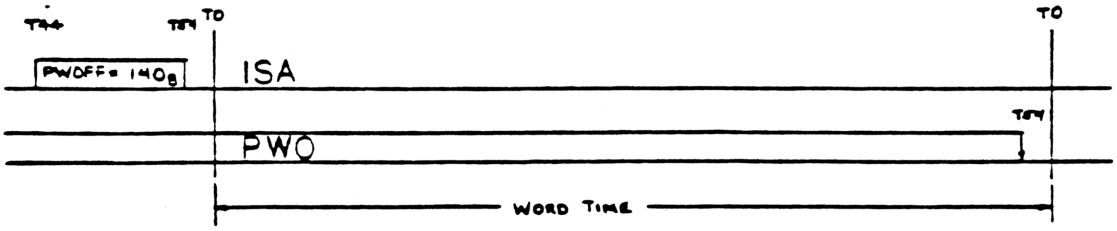
6.8 Figure 5: Chip Enable Timing.



CHIP ENABLE SEQUENCE

HK 9/3/80

6.9 Figure 6: PWOFF Timing.

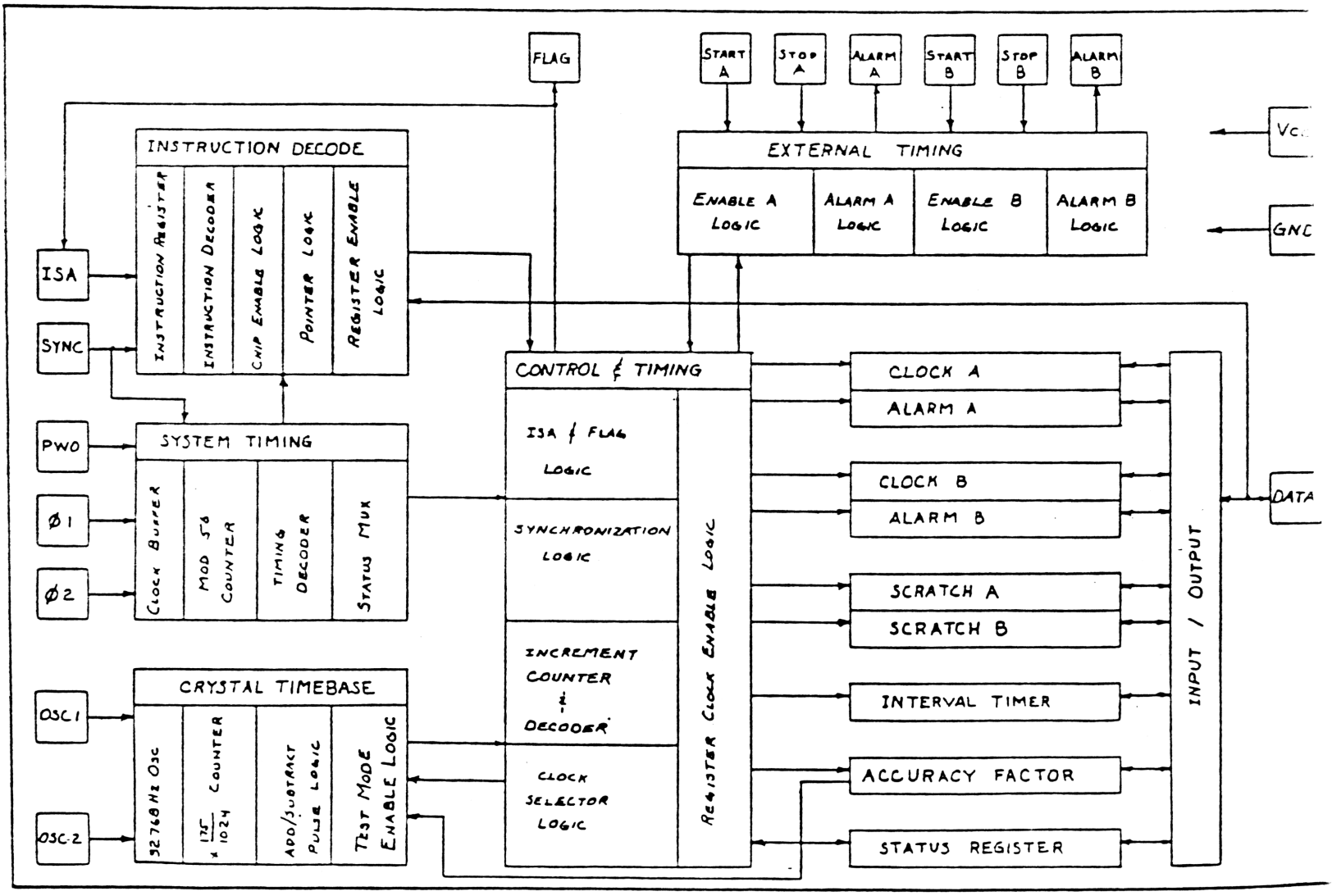


PWOFF TIMING

6.10 Figure 8: Block Diagram.

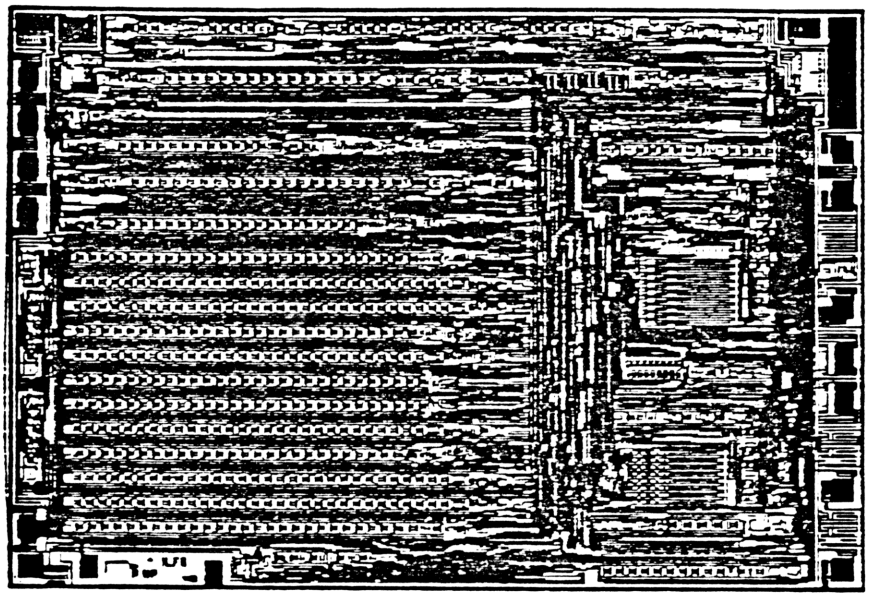
PHINEAS BLOCK DIAGRAM

HK 9/3/8



6.11 Figure 9: Metal Mask.

APRIL 8, 1981
1LF6-MSK



TECHNICAL DETAILS OF BUS TIME MODULE

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As Issued	01-08-82	HKIII
B	PCO#64-0423 - Include the 1LF6-0001 in a 20 pin plastic package and add Section VI for pinout listing for 20 pin pkg.	5/4/83	M. R.

Model No.		Stock No. Applies To:	1LF6-4001
Title	1LF6 Electrical Specifications		1LF6-0101
Description		Date	01-08-82
By	Hank Koerner	Sheet No.	1 of 7
Supersedes		Drawing No.	A-1LF6-9002-1

(B) The following specifications detail operating limits and conditions for for the 1LF6 Timer Chip (1LF6-4001) in a 28 pin ceramic package (1LF6-0101) and a 20 pin plastic DIP (1LF6-0001).

I. Absolute Maximum Ratings:

Supply Voltage Vcc (Gnd=0V)	+ 10 V
Storage Temperature	-50 C to +150 C
Operating Temperature	0 C to +65 C
Humidity	0 to 90%
Voltage at any pin	Gnd - 0.3 V to Vcc + 0.3 V
Input Transient Protection	600 Vdc

II. Recommended Operating Conditions: 0 C <= Ta <= 45 C

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Gnd	Ground	0.0	0.0	0.0	V	System & signal ground
Vcc	Pos. Supply	5.5	6.25	7.0	V	
Iccop	Operating current		0.5	1.0	mA	Vcc = 6.5 V Freq = 380 kHz
Iccsby	Standby current		0.2	1.0	uA	Vcc = 5.0 V System inactive Inputs grounded Outputs tristated Osc In high
Iccsop	Standby Operating current		10.0	24.0	uA	Vcc = 5.0 V System inactive Internal Oscillator active
	Input Parameters :					
Vih	Input high voltage level	Vcc - 1.25	.6 x Vcc		V	Typ value characterized
Vil	Input low voltage level		.4 x Vcc	Vcc + 1.25	V	Typ value characterized
Iinlk (note 1)	Input leakage current on input pins		5.0	100	nA	Protection diodes reverse biased to 6.5 V
Iiolk (note 2)	Input leakage current on I/O pins.		10.0	1000	nA	Protection diodes reverse biased to 6.5 V

II. Recommended Operating Conditions: 0 C <= Ta <= 45 C

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Cin (note 3)	Input Capacitance for input pins		3.0	6.0	pF	Protection diodes make up the load
Cinio (note 4)	Input capacitance for I/O & Output pins		5.0	10.0	pF	Protection diodes + output drivers make up the load
	Output Parameters :					
Voh	Output high voltage level	Vcc - 1.0	Vcc		V	Typ value characterized
Vol	Output low voltage level		Gnd	Gnd + 1.0	V	Typ value characterized
Cout	Output drive capability :					These outputs wil drive the specified capacitance
	DATA, FLAG	200	400		pF	between Vol and Voh within Tdv w/
	Alarm A & B	70	150		pF	no DC loads.
	ISA	100	200		pF	See figure 1. Typ values characterized.
	Timing Parameters (see figure 1 for parameter definitions) :					
Tphf	Clock Period - high frequency	2.63	1.05		uS	Typ value characterized
Tplf	Clock Period - low frequency		1.00	2.95	uS	Max value characterized = 5 uS, but 10KHZ operation not uncommon
Tpw1	Phase 1 clock width	500	2/8 of Tp	750	nS	Min and max specs reflect test limits. Margin indicated by characterization: Tpw1 min = 60 nS Tpw2 min = 200 nS
Tpw2	Phase 2 clock width	500	2/8 of Tp	750	nS	
Tcd	Clock delay	900	3/8 of Tp	1200	nS	

II. Recommended Operating Conditions: 0 C <= Ta <= 45 C

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Tr, Tf	Clock rise & fall times		50		nS	
Tdv	Output data valid time		500	1000	nS	Typ value characterized
Tsu	Input data setup time		110	550	nS	Typ value characterized

Note 1 : The Iinlk spec applies to: Phase 1, Phase 2, SYNC, PWO.
Osc In is connected, via the performance board, through a 22 M ohm resistor to Osc Out; consequently, its spec is +- 600 nA.
Start A & B and Stop A & B, all four are inputs, each have a 2.5 K ohm pull down; only their positive going diodes are measured at a leakage spec of 4 uA.
PWO has a 250K ohm integrated p-well pull down; only its positive going diode is measured for leakage.

Note 2 : The Iiolk spec applies to: Alarm A, Alarm B, Osc Out, FLAG, ISA, DATA.

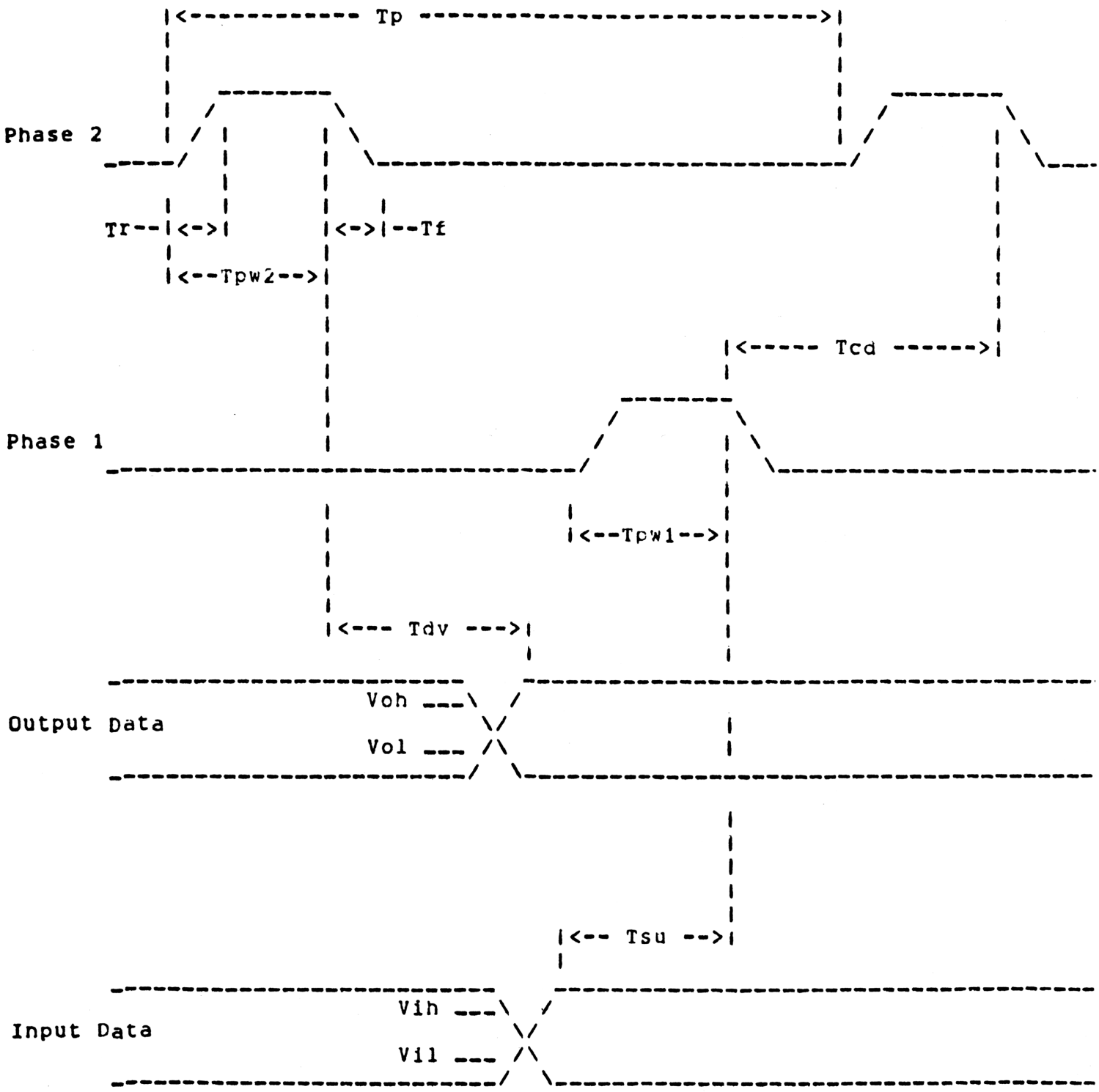
Note 3 : The Cin spec applies to: Phase 1, Phase 2, SYNC, Osc In, PWO, Start A, Start B, Stop A, Stop B.

Note 4 : The Cinio spec applies to: Alarm A, Alarm B, Osc Out, FLAG, ISA, DATA.

III. Test Specifications.

Parameter	Wafer	Package	QA	Wafer	Package	QA
	Low Voltage (Volts)			High Voltage (Volts)		
Vcc	5.5	5.5	5.7	7.2	7.1	7.0
Vih	4.25	4.25	4.45	5.95	5.85	5.75
Vil	1.25	1.25	1.25	1.25	1.25	1.25
Voh	4.5	4.5	4.7	6.0	6.0	6.0
Vol	1.0	1.0	1.0	1.0	1.0	1.0
	High Frequency (nS)			Low Frequency (nS)		
Tp	2630	2630	2630	2950	2950	2950
Tpw1	500	500	500	750	750	750
Tpw2	500	500	500	750	750	750
Tcd	900	900	900	1200	1200	1200
Tdv	1000	1000	1000	1000	1000	1000
Tsu	550	550	550	550	550	550
	DC Parametrics (uA)			Test Conditions		
Iccop	800	900	1000	Vcc = 6.5 V @ High Freq		
Iccsby	0.8	0.9	1.0	Vcc = 5.0 V, System inactive		
Iccsop	22.0	23.0	24.0	" " " "		
Iinlk	0.09	0.10	----	@ 10 V to Gnd and Vcc		
Iinlk	----	----	0.10	@ 6.5 V to Gnd and Vcc		
Iiolk	0.8	0.9	1.0	@ 6.5 V to Gnd and Vcc		
	Stress Test (Volts)			Comments		
Vstress	10.0	----	----	Functional test at high freq. Vcc = Vstress. Ignore fails.		

IV. Figure 1 - Timing Parameter definition and clock system waveforms.



V. 28 Pin ceramic package pinout listing:

Pin #	Signal	Pin #	Signal
1	Vcc	15	NC
2	NC	16	NC
3	NC	17	FLAG
4	NC	18	NC
5	Phase 2	19	ISA
6	Phase 1	20	PWO
7	Alarm A	21	Stop B
8	Alarm B	22	Start B
9	SYNC	23	NC
10	DATA	24	Start A
11	Osc Out	25	NC
12	NC	26	Stop A
13	Osc In	27	Gnd
14	NC	28	NC

VI. 20 Pin Plastic DIP pinout listing:

Pin #	Signal	Pin #	Signal
1	SYNC	11	NC
2	DATA	12	Start A
3	Osc Out	13	Stop A
4	NC	14	GND
5	Osc In	15	VCC
6	FLAG	16	NC
7	ISA	17	Phase 2
8	PWO	18	Phase 1
9	Stop B	19	Alarm A
10	Start B	20	Alarm B

82143A - INTERFACE CHIP -

HEWLETT-PACKARD CO.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As Issued	6-5-79	CT/RG

Model No.		Stock No.	1LB4-4001
Title	PERIPHERAL INTERFACE CHIP		
Description	DETAILED DESCRIPTION	Date	March 29, 1978
By	Charles Tan RJ Livingston 7/25	Sheet No.	1 of 7
Supersedes		Drawing No.	A-1LB4-4001-2

9320-3246 (6/75)

THE NUT-PERIPHERAL INTERFACE CHIP

ABSTRACT

The Nut-peripheral interface chip (NPIC) is a bidirectional serial in, serial out buffer. This chip will allow Nut-CPU to interface with microprocessor which has different system clock, bus structure and speed. Two sets of 56 bits of data or information can be simultaneously input to or output from the NPIC. With a single mask option, NPIC chip-select-addresses can be changed. With this option, two NPIC can be controlled independently by the same Nut-CPU. The NPIC will also include feature which enables the peripheral to wake up the Nut-CPU while Nut-CPU is in a "light-sleep" mode. Conversely, the Nut-CPU can wake up the peripheral through an assigned Nut-peripheral instruction. Providing that the Nut-CPU speed is not a problem or sufficient buffering is available, Nut-CPU will be able to interface with any general microprocessor in existence. The 95x100 mil^2 CMOS chip will have 13 bonding pads. Currently, the NPIC is designed to drive the Nut-peripheral printer (Helios).

CIRCUIT DESCRIPTION

The chip can be divided into four parts. They are timing generator, instruction decoder, Nut-data buffer and transfer logic and peripheral-data buffer & transfer logic.

The timing generator keeps the NPIC and the Nut-CPU in synchronization. It also generates bit time TØ and T55 from the "SYNC" line.

The instruction decoder detects the five NPIC instructions from the "ISA" line. They are ENPIC, LOAD, SAVE, SET, PRTON. Nut-CPU instruction (1144_8) ENPIC switches Nut-CPU mode to NPIC mode. Any instruction that follows after the ENPIC instruction is a Nut-peripheral instruction. During NPIC mode the 10 bit instructions are ignored by the Nut-CPU. LOAD, SAVE, SET, PRTON instructions can be executed only during the NPIC mode. Any odd number Nut-peripheral instruction

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL	STK NO 1LB4-4001
PERIPHERAL INTERFACE CHIP	
BY Charles Tan	DATE March 29, 1978
APPD	SHEET NO 2 OF 7
SUPERSEDES	DWG NO A-1LB4-4001-2

CIRCUIT DESCRIPTION (CONT.)

will switch NPIC mode back to the Nut-CPU mode. With a single mask option different chip-select-addresses can be built into different NPIC chips. Pre-assigned ENPIC instructions can be used to select different NPIC chips. (1044_8) ENPIC instruction is already assigned for the second NPIC chip. Command, status & data can be independently transferred using two NPIC chips.

NPIC INSTRUCTION SET

ENPIC (1144_8)

It enables NPIC mode and selects different NPIC chips.

LOAD ($XXX7_8$) X = Don't Cares

It loads data from CPU register C into NPIC buffer 1. "Busy Flip Flop" is set after the data transfer.

SAVE ($XX72_8$)

It saves data from NPIC buffer 2 into CPU register C. "Read Flip Flop" is reset after the data transfer. An odd number ($XXX5_8$) peripheral instruction must follow the save instruction to switch back to the Nut-CPU mode.

SET ($XQ03_8$); Q=0,1,2.

It selects one of the three flags from NPIC and sent it into the carry bit of the Nut-CPU . Q is the flag select bit

Q=0 selects "Busy" flag

Q=1 selects "RFF" flag

Q=2 selects "DD3" flag

"Busy" indicates that data from the Nut-CPU are still in buffer 1 of NPIC. "Busy" is cleared after the data from buffer 1 are transferred out to the peripheral. "Busy" is set after a "load" Nut-peripheral instruction. "Busy" can be read by both the peripheral and the Nut-CPU.

"RFF" indicates that data are ready to be saved into the Nut-CPU register C. "RFF" is set after the data from the peripheral are transferred into buffer 2. "RFF" is reset after a "save" Nut-peripheral instruction. "RFF" can be read by both the peripheral and the Nut-CPU.

NPIC INSTRUCTION SET CONT.

"DD3" indicates that the peripheral is switched "ON". When the peripheral is disconnected or switched "OFF", "DD3" will be low.

~~PRTON $(XXX1_8)$~~

~~It turns on the peripheral by pulling $\overline{PON}$ line low for one Nut word time.~~

NUT INTERFACE LINES

- SYNC, ISA, DATA are the Nut-CPU serial bus lines which can transfer data and instruction to and from the Nut-CPU. To the Nut-CPU, NPIC works like another memory chip.
- PWO clears all NPIC's internal Flip Flops, whenever the Nut-CPU wakes up from "Deep" or "Light-sleep" mode.
- $\emptyset_1$ & $\emptyset_2$ are the two-phase clock used by the Nut system.
- VCC is the 6 volt regulated power supply line from the Nut system. During Nut's "Light-sleep" mode, VCC is still at 6 volt, "SYNC" line is high and $\emptyset_1$ & $\emptyset_2$ clock is disabled. During Nut's "Deep-sleep" mode, VCC is at 3.9 volt, "SYNC" line is low and $\emptyset_1$ & $\emptyset_2$ clock is also disabled.
- GND is common to all systems.

PERIPHERAL INTERFACE LINES

needs 10K pull-up resistor

- DDØ is a bidirectional data line interfacing the peripheral and the NPIC.
- DD1 is a strobe line controlled by the peripheral. Data or flag can be transferred through the DDØ line sequentially by the strobing of DD1.
- DD2 is a direction-select line. Data can be transferred from the peripheral to the NPIC when DD2 is low. One or more DD1 strobes, while DD2 is low, followed by a positive edge of DD2 sets "RFF". Two or more DD1 strobes, while DD2 is high, followed by a negative edge of DD2 resets "Busy".

When DD2 goes high, the first bit on DDØ line is the "Print Flip Flop". The second bit on DDØ line is the "RFF". The 56 bits of data from buffer 1 follows after "RFF". "PFF" is the same as "$\overline{BUSY}$". When NPIC is not connected to the

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PERIPHERAL INTERFACE LINES CONT.

peripheral DDØ should stay high indicating "$\overline{\text{Busy}}$".

When DD2 goes low, 56 bits of data from the peripheral can be transferred into buffer 2.

DD3 can be any peripheral flag. Normally it will be used to indicate peripheral on/off status.

$\overline{\text{PON}}$ is a bidirectional power on for both the Nut-CPU and the peripheral. Normally $\overline{\text{PON}}$ stay high. When the peripheral pull down $\overline{\text{PON}}$, while Nut-CPU is in "Light-sleep" mode, it wakes up the Nut-CPU. This is done internal to the NPIC by detecting "Light-sleep" mode and pulling "ISA" line high until "PWO" line goes high.

When "Nut-CPU" sends a "PRTON" peripheral instruction, it pulls down the $\overline{\text{PON}}$ line for exactly one word time. If the peripheral is designed to detect this state, it will be able to execute a wake-up routine.

TIMING REQUIREMENTS

When transferring data from the peripheral to the NPIC, DD2 must be low. Valid data must be held stable on DDØ for at least two Nut-system clock after the positive transition of DD1.

When transferring data from the NPIC to the peripheral, DD2 must be high. "PFF" will be on DDØ, one Nut-system clock after the positive transition of DD2. The rest of the data will be on DDØ, two Nut-system clock after the positive transition of DD1.

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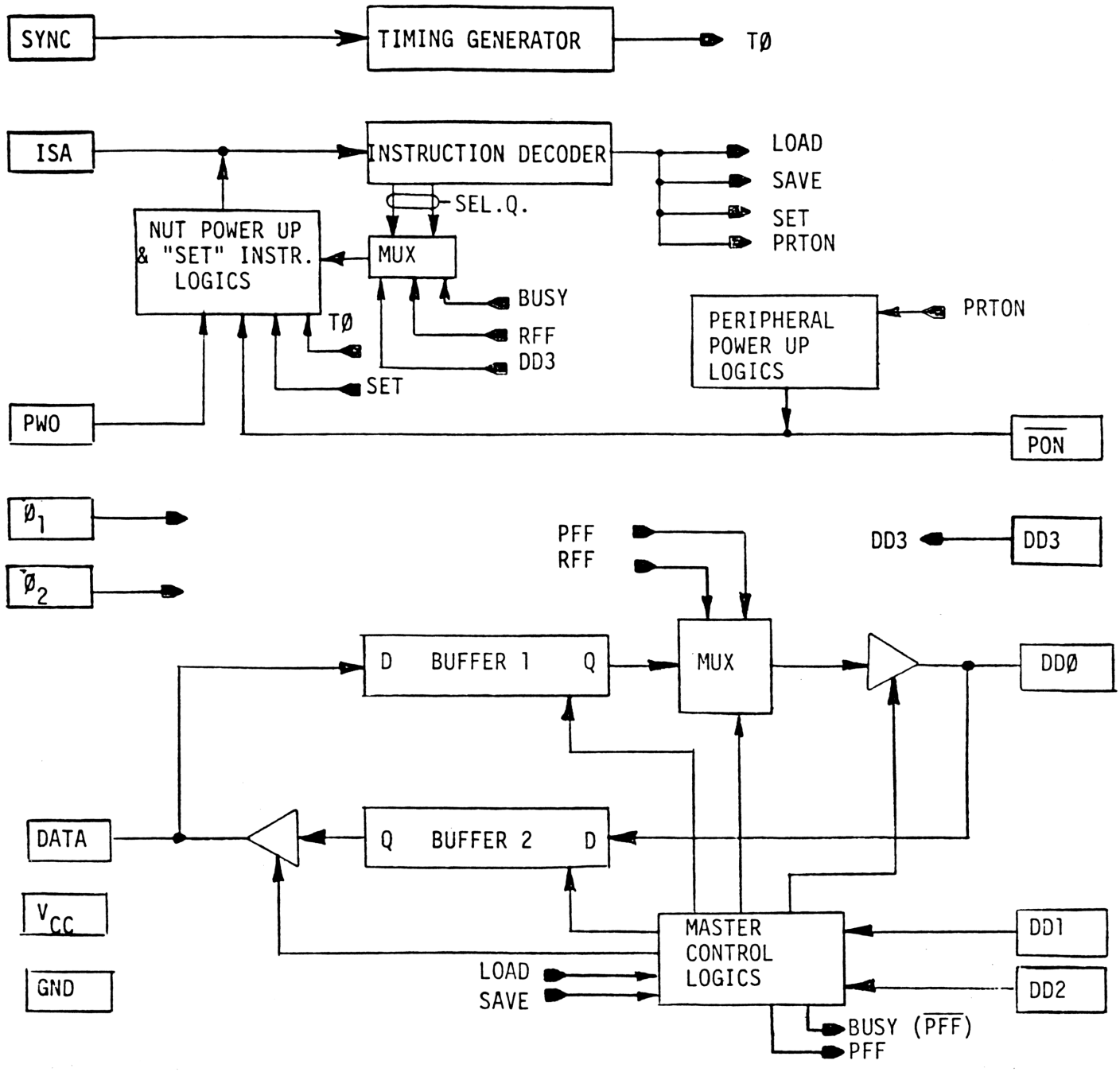

BLOCK DIAGRAM OF NUT PERIPHERAL INTERFACE CHIP

FIGURE 1

LTR	P C NO	APPROVED	DATE
	REVISIONS		

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TITLE PERIPHERAL INTERFACE CHIP	
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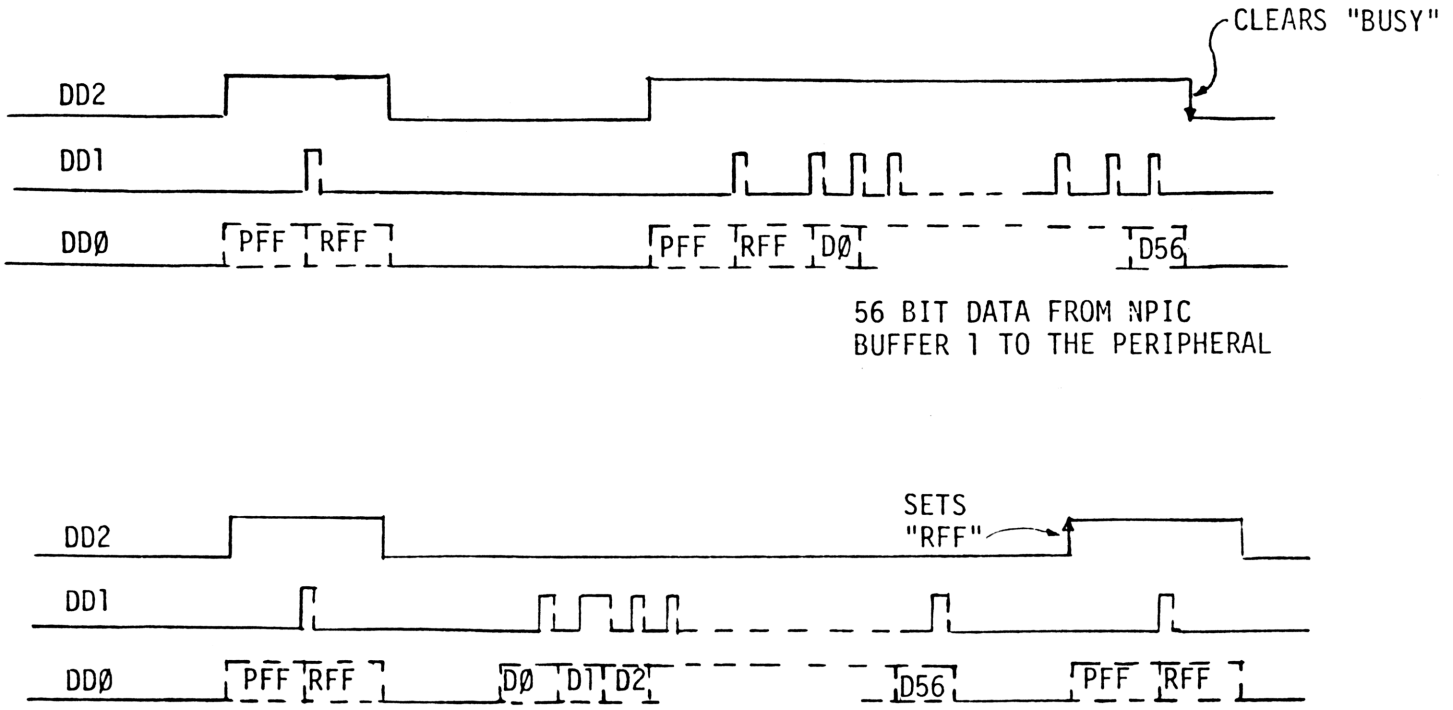

NOTES:

1. VALID DATA MUST BE ON DDØ BEFORE DD1 STROBES.
2. RECOMMENT TO HOLD DATA FOR AT LEAST 2 NUT SYSTEM CLOCK AFTER DD1 STROBES.

TIMING DIAGRAM OF THE NPIC-PERIPHERAL INTERFACE SIGNAL

FIGURE 2

LTR	P.C. NO	APPROVED	DATE
	REVISIONS		

MODEL	STK NO 1LB4-4001
PERIPHERAL INTERFACE CHIP	
BY Charles Tan	DATE March 29, 1978
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NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before-and-after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle, or other attention-getting outline).

Ltr	REVISIONS	DATE	INITIALS
A	As Issued	6-5-79	CT/RG

Model No.	Stock No. 1LB4-4001
Title INTERFACE CHIP	
Description ELECTRICAL SPECIFICATION	Date 8-15-78
By Charles Tan	Sheet No. 1 of 8
Supersedes	Drawing No. A-1LB4-4001-1

I MAXIMUM RATINGS

1.1 Supply Voltage V_{CC} .....+10V

1.2 Storage Temperature.....-50°C to +150°C

1.3 Operating Temperature.....0°C to 65°C

1.4 Humidity.....0 to 90%

1.5 Voltage at any input or output pin.....GND -0.3V to V_{CC} +0.3V

1.6 Input transient protection.....1000 V

II OPERATING CONDITIONS

0°C ≤ TEMP ≤ 45°C

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
V_{CC}	POWER SUPPLY VOLTAGE	6.0	6.25	7	V	
GND	GROUND	0	0	0	V	
I_{CCOP}	SUPPLY CURRENT		1		mA	CLK @ 380 KHz V_{CC} @ 6.5 V
I_{CCST}			1		uA	CLK @ 0 KHz V_{CC} @ 5 V
	INPUT PARAMETERS					
$V_{IN}(H)$	INPUT VOLTAGE LEVEL (HIGH)	V_{CC}-1.25	.8 V_{CC}	V_{CC}	V	
$V_{IN}(L)$	INPUT VOLTAGE LEVEL (LOW)	GND	.2 V_{CC}	GND+1.25	V	
I_{INL}	INPUT LEAKAGE CURRENT			0.1	uA	All INPUT PINS V_{CC} @ 6.5 V
I_{IOL}	TRI-STATE LEAKAGE CURRENT			1.0	uA	All I/O PINS WHEN TRI-STATED

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
C_{IN}	INPUT CAPACITANCE			8	pf	EXCEPT V_{CC}
	OUTPUT PARAMETERS					
$V_{OUT}(H)$	OUTPUT VOLTAGE LEVEL (HIGH)	V_{CC}-1.0			V	
$V_{OUT}(L)$	OUTPUT VOLTAGE LEVEL (LOW)			GND+1.0	V	
C_{OUT}	OUTPUT CAPACITANCE (DRIVE CAPABILITY)					
	ISA, DATA	200			pf	
	DDØ, PON	200			pf	
	TIMING PARAMETERS					
T_P	CLOCK PERIOD	2.63	2.78	2.95	us	SEE FIG. 1
$T_{PW}(Ø1)$	Ø1 PULSE WIDTH	500	(2/8 of T_0)	750	ns	" " "
$T_{PW}(Ø2)$	Ø2 PULSE WIDTH	500	(2/8 of T_0)	750	ns	" " "
TCD	CLOCK DELAY	900	3/8 of T_0	1200	ns	" " "
T_R, T_F	CLOCK RISE, FALL TIME		50		ns	" " "
T_{DV}	OUTPUT DATA VALID (AFTER TRAILING EDGE OF Ø2)		(3/8 of T_0)	800	ns	" " "
T_{SU}	DATA SETUP TIME	300	(1/8 of T_0)		ns	" " "

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MODEL | STK. NO 1LB4-4001

INTERFACE CIRCUIT - ELECTRICAL SPECIFICATIONS

BY CHARLES TAN | DATE 8-15-78

APPD | SHEET NO 3 OF 8

SUPERSEDES | DWG. NO A-1LB4-4001-1

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
	TIMING PARAMETERS FOR PERIPHERAL INTERFACE					
T_{DV2}	TIME FROM DD2↑ TILL VALID "BUSY" ON DDØ	TP+200			ns	SEE FIG.2 NO DD1↑ ALLOWED
T_{PW1}	DD1 PULSE WIDTH	TP+50			ns	SEE FIG.2
T_{DV1}	TIME FROM 1st DD1↑ TILL VALID "REF" ON DDØ	TP+400			ns	SEE FIG. 2
T_R,T_F	RISE, FALL TIME		100		ns	SEE FIG. 2
T_{DV3}	TIME FROM 2nd AND SUCCEEDING DD1↑ TILL VALID DATA ON DDØ	3TP+300			ns	SEE FIG. 2
T_{DV5}	TIME FROM DD2↑ TILL DDØ TRI-STATED BY NPIC	TP+200			ns	SEE FIG. 3
T_{DV4}	TIME FROM DD1↑ TILL DATA ON DDØ READ			TP+100		SEE FIG. 3 DDØ DATA MUST BE VALID BEFORE THIS TIME
T_{DH}	DATA HOLD TIME	TP+100				SEE FIG. 3 DATA ON DDØ MUST BE HELD VALID FOR THIS TIME.

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL | STK NO 1LB4-4001

INTERFACE CHIP - ELECTRICAL SPECIFICATION

BY Dave Shelley | DATE 6-1-79

APPD | SHEET NO 4 OF 8

SUPERSEDES | DWG NO A-1LB4-4001-1

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PARA.	WAFER	PKG	QA	WAFER	PKG	QA
	LOW VOLTAGE (V)			HIGH VOLTAGE (V)		
VCC	5.5	5.5	5.7	7.6	7.5	7.4
VIH	4.25	4.25	4.45	6.0	6.0	6.0
VIL	1.25	1.25	1.25	1.25	1.25	1.25
VOH	4.5	4.5	4.7	6.0	6.0	6.0
VOL	1.0	1.0	1.0	1.0	1.0	1.0
	HIGH FREQUENCY (ns)			LOW FREQUENCY (ns)		
TP	2360	2360	2360	2950	2950	2950
TPW1	500	500	500	750	750	750
TPW2	500	500	500	750	750	750
TCD	900	900	900	1200	1200	1200
TDV	1000 (1)	1000 (1)	1000 (1)	1000 (1)	1000 (1)	1000 (1)
TSU	550	550	550	550 (2)	550 (2)	550 (2)

	DC PARAMETRIC			TEST CONDITIONS
ICCOP	.8ICCOP	.9ICCOP	ICCOP	VCC = 6.5V, FREQ = MAX
ICCST	.8ICCST	.9ICCST	ICCST	VCC = 5.0V, STATIC
I_{INL}	$.9I_{INL}$	I_{INL}	- - -	@10V TO GND AND VCC
I_{INL}	- - -	- - -	I_{INL}	@6.5V TO GND AND VCC
I_{IOL}	$.8I_{IOL}$	$.9I_{IOL}$	I_{IOL}	@5.6V TO GND AND VCC

	STRESS TEST			COMMENTS
VSTRESS	10V	- - -	- - -	OPERATE PART AT MAX FREQ WITH VCC= VSTRESS FOR 1 LMLOAD, IGNORE FAILURES.

NOTE:

1. DATA and ISA (Ø) on 1LA5, and ISA on 1LA3 - - TDV at 800 ns.
2. DATA and ISA inputs on 1AL4 and 1LA7 - - TSU at 800 ns before trailing edge Ø1.

LTR	P C NO	APPROVED	DATE
	REVISIONS		

MODEL	STK NO 1LB4-4001
INTERFACE CIRCUIT - ELECTRICAL SPECIFICATIONS	
BY CHARLES TAN	DATE 8-15-78
APPD	SHEET NO 5 OF 8
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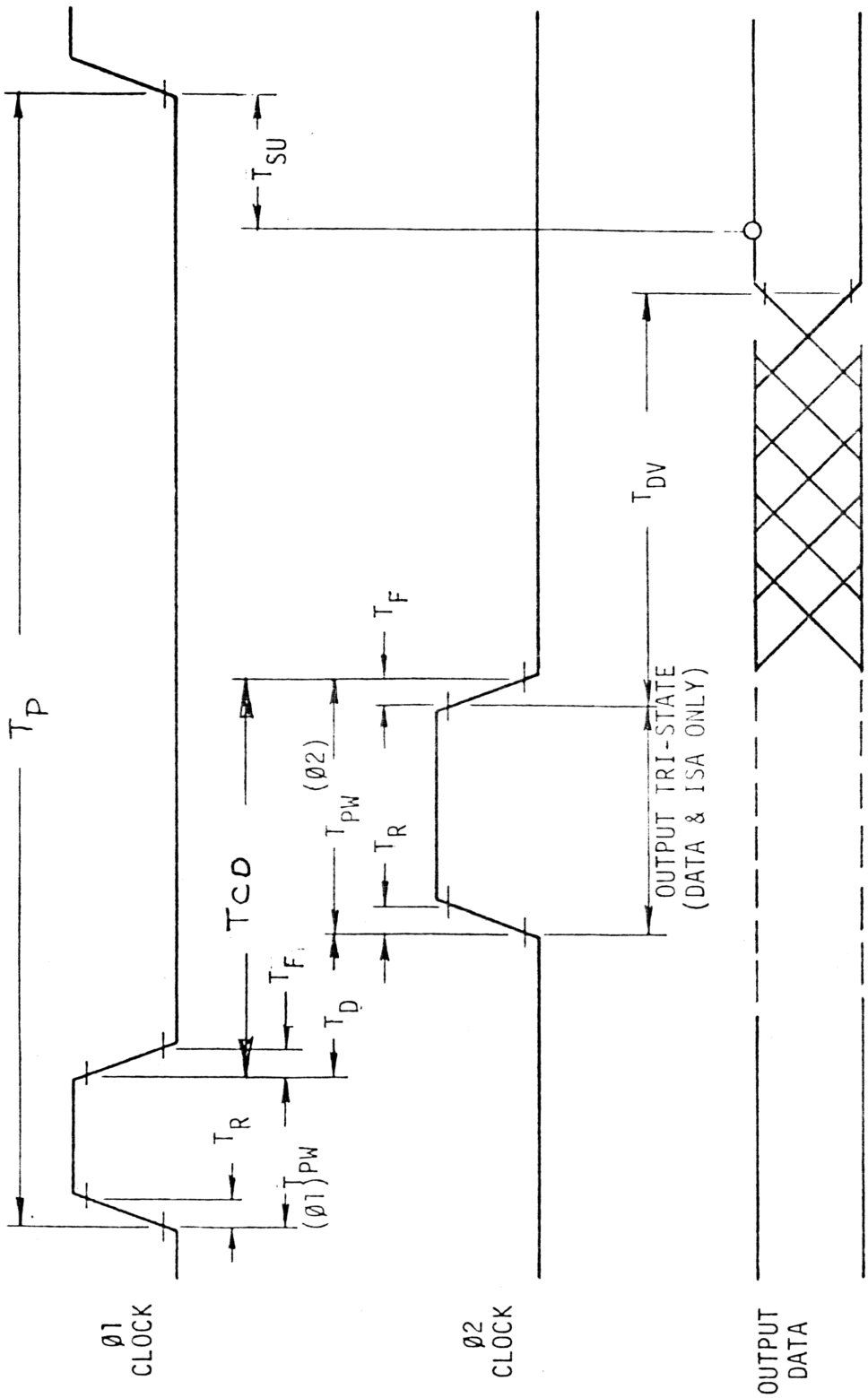

SYSTEM CLOCK WAVEFORMS

FIGURE 1

				MODEL	STK NO 1LB4-4001
				INTERFACE CHIP - ELECTRICAL SPECIFICATIONS	
				BY Charles Tan	DATE 8-15-78
LTR	P.C NO	APPROVED	DA	APPD	SHEET NO 6 OF 8
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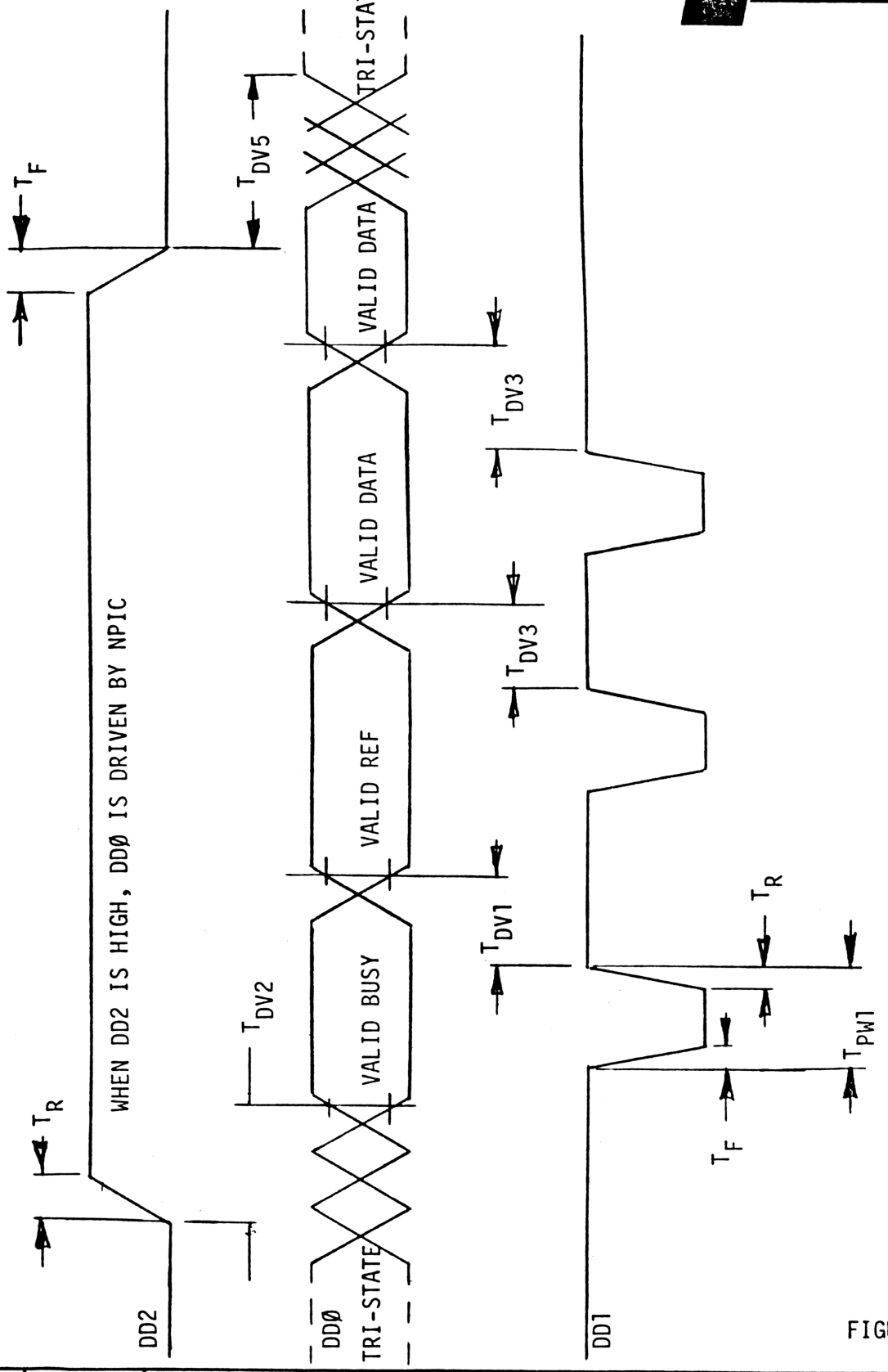
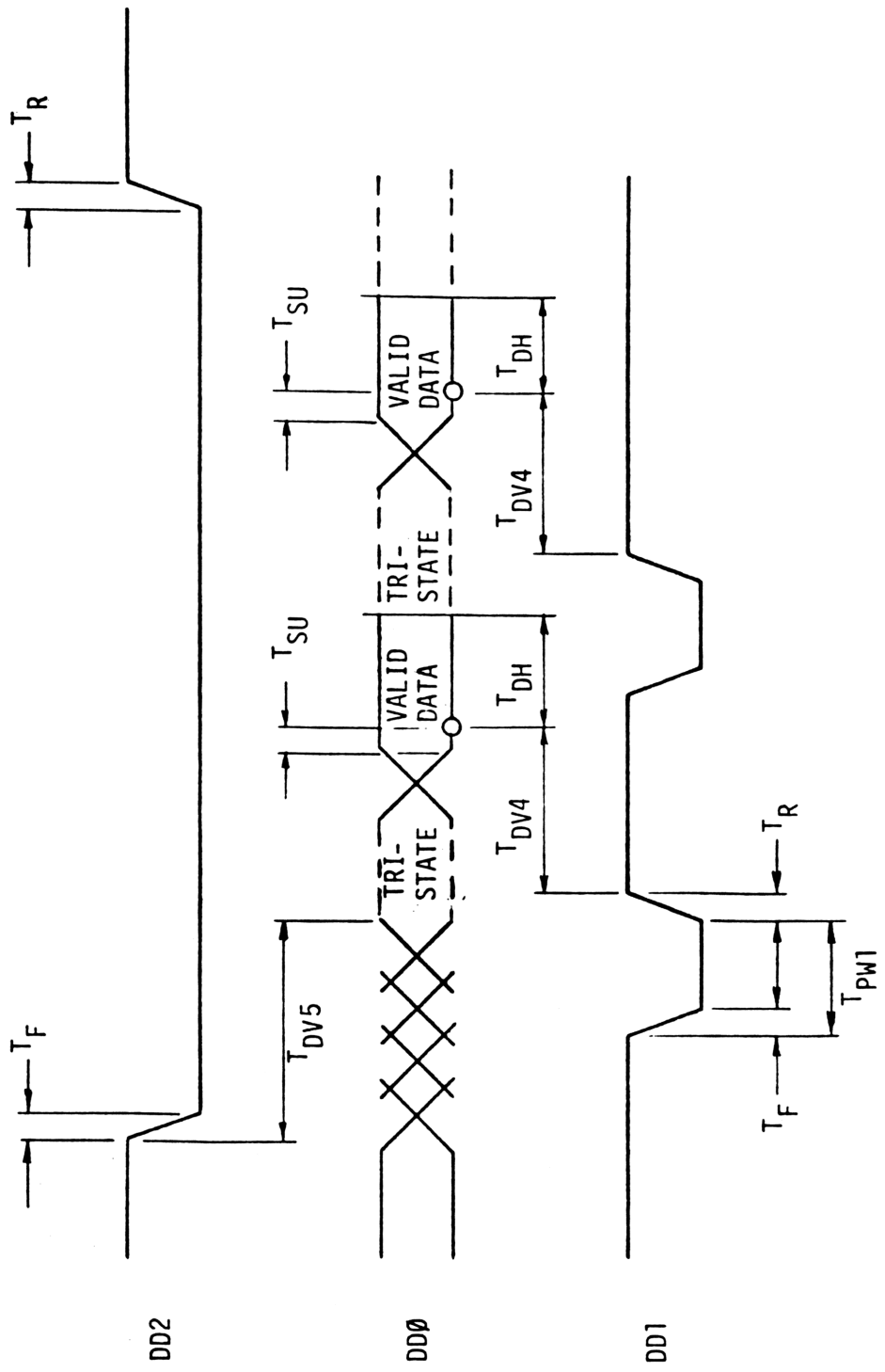


FIGURE II

				MODEL	STK NO 1LB4-4001
				INTERFACE CHIP - ELECTRICAL SPECIFICATIONS	
				BY Dave Shelley	DATE 6-1-79
LTR	P.C NO	APPROVED	DA	APPD	SHEET NO 7 OF 8
		REVISIONS		SUPERSEDES	DWG NO A-1LB4-4001-1



DATA TRANSFER FROM PERIPHERAL TO NPIC

FIGURE 3

				MODEL	STK NO 1LB4-4001
				INTERFACE CHIP - ELECTRICAL SPECIFICATIONS	
				BY Charles Tan	DATE 8-15-78
LTR	P.C. NO	APPROVED	DATE	APPD	SHEET NO 8 OF 8
	REVISIONS			SUPERSEDES	DWG NO A-1LB4-4001-1