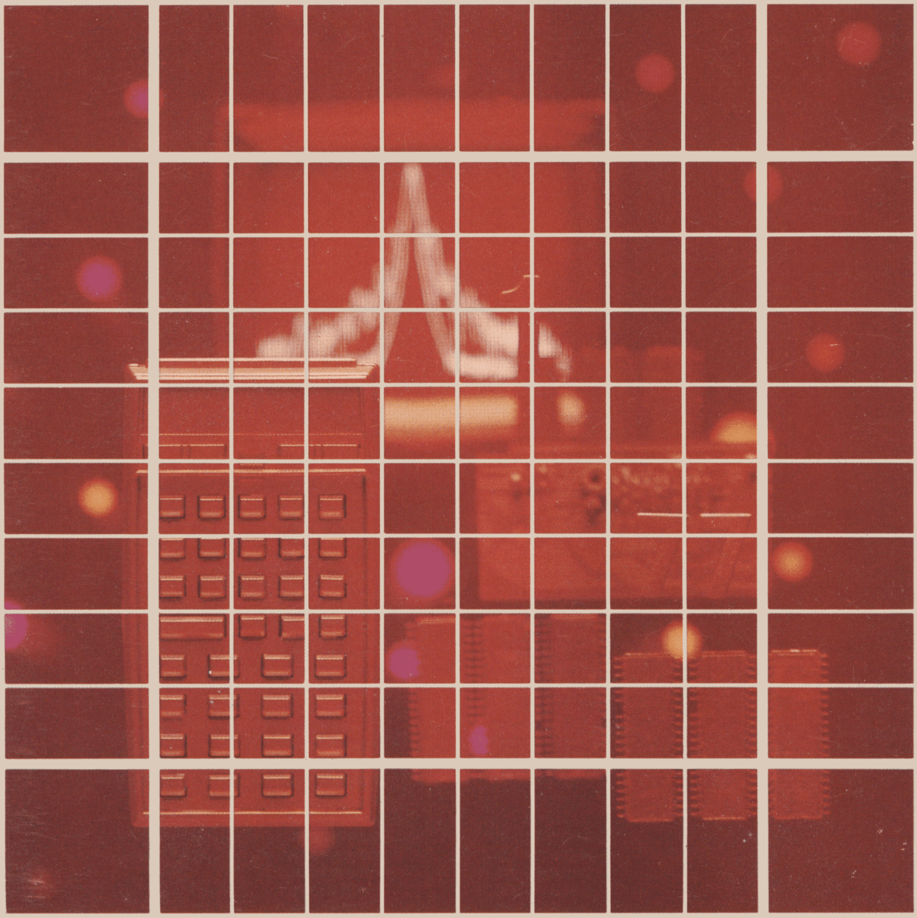
HEWLETT-PACKARD

HP-41C

CIRCUIT ANALYSIS PAC



NOTICE

HEWLETT PACKARD

HEWLETT-PACKARD LISTENS

To provide better calculator support for you, the Application Engineering group needs your help. Your timely inputs enable us to provide higher quality software and improve the existing application pacs for your calculator. Your reply will be extremely helpful in this effort.

1. Pac name ______________________________

2. How important was the availability of this pac in making your decision to buy a Hewlett-Packard calculator?

   ☐ Would not buy without it. ☐ Important ☐ Not important

3. What is the major application area for which you purchased the pac?

____

4. In the list below, please rate the usefulness of the programs in this pac.

PROGRAM NUMBER	ESSENTIAL	IMPORTANT BUT NOT REQUIRED	INFREQUENTLY USED	NEVER USED
1				
2				
3				
4				
5				
6				
7				
8				

PROGRAM NUMBER	ESSENTIAL	IMPORTANT BUT NOT REQUIRED	INFREQUENTLY USED	NEVER USED
9				
10				
11				
12				
13				
14				
15				
16				

5. Did you purchase a printer? ☐ YES ☐ NO

   If you did, is the printing format in this pac useful? ☐ YES ☐ NO

6. What programs would you add to this pac?

____

7. What additional application pacs would you like to see developed?

____

THANK YOU FOR YOUR TIME AND COOPERATION.

____
Name Position

____
Company

____
Address

____
City State

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Additional Comments:

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INTRODUCTION

The Circuit Analysis Pac consists of a general network analysis program, GNAP, and a ladder network analysis program, LNAP. This manual provides a description of each program, relevant equations, a set of instructions for using the programs, and several example problems, each of which includes a list of keystrokes required for its solution.

Before plugging in your Application Module, turn the calculator off, and be sure you understand the section ''Inserting and Removing Application Modules.'' Before using a particular program, take a few minutes to read ''Format of User Instructions'' and ''A Word About Program Usage.''

You should first familiarize yourself with a program by running it once or twice following the user instructions in the manual. Thereafter, the program's prompting or the mnemonics on the overlays should provide the necessary instructions, including which variables are to be input, which keys are to be pressed, and which values will be output.

We hope that the Circuit Analysis Pac will assist you in the solution of numerous problems. We would appreciate knowing your reactions to the programs in this pac, and to this end we have provided a questionnaire inside the front cover of this manual. Would you please take a few minutes to give us your comments on these programs? It is from your comments that we learn how to increase the usefulness of our programs.

CONTENTS

INSERTING AND REMOVING APPLICATION MODULES

Before you insert an Application Module for the first time, familiarize yourself with the following information.

Up to four Application Modules can be plugged into the ports on the HP-41C. While plugged in, the names of all programs contained in the Module can be displayed by pressing ■ CATALOG 2.

CAUTION

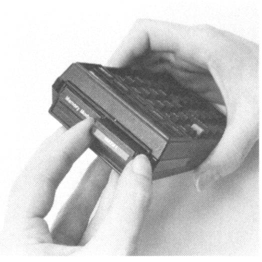
Always turn the HP-41C off before inserting or removing any plug-in extension or accessories. Failure to turn the HP-41C off could damage both the calculator and the accessory.

To insert Application Modules:

1. Turn the HP-41C off! Failure to turn the calculator off could damage both the Module and the calculator.

2. Remove the port covers. Remember to save the port covers; they should be inserted into the empty ports when no extensions are inserted.

3. Insert the Application Module with the label facing downward as shown, into any port **after** the last Memory Module. For example, if you have a Memory Module inserted in port 1, you can insert an Application Module in any of ports 2, 3, or 4. (The port numbers are shown on the back of the calculator.) **Never insert an Application Module into a lower numbered port than a Memory Module.**



4. If you have additional Application Modules to insert, plug them into any port after the last Memory Module. Be sure to place port covers over unused ports.

5. Turn the calculator on and follow the instructions given in this book for the desired application functions.

To remove Application Modules:

1. Turn the HP-41C off! Failure to do so could damage both the calculator and the Module.
2. Grasp the desired Module handle and pull it out as shown.

3. Place a port cap into the empty ports.

Mixing Memory Modules and Application Modules

Any optional accessories (such as the HP-82104A Card Reader, or the HP-82143A Printer) should be treated in the same manner as Application Modules. That is, they can be plugged into any port after the last Memory Module. Also, the HP-41C should be turned off prior to insertion or removal of these extensions.

The HP-41C allows you to leave gaps in the port sequence when mixing Memory and Application Modules. For example, you can plug a Memory Module into port 1 and an Application Module into port 4, leaving ports 2 and 3 empty.

FORMAT OF USER INSTRUCTIONS

The completed User Instruction Form– which accompanies each program is your guide to operating the programs in this Pac.

The form is composed of five labeled columns. Reading from left to right, the first column, labeled STEP, gives the instruction step number.

The INSTRUCTIONS column gives instructions and comments concerning the operations to be performed.

The INPUT column specifies the input data, the units of data if applicable, or the appropriate alpha response to a prompted question. Data input keys consist of 0 to 9 and the decimal point (the numeric keys), [EEX] (enter exponent), and [CHS] (change sign).

The FUNCTION column specifies the keys to be pressed after keying in the corresponding input data.

The DISPLAY column specifies prompts, intermediate and final answers, and their units, where applicable.

Above the DISPLAY column is a box which specifies the minimum number of data storage registers necessary to execute the program. Refer to the Owner's Handbook for information on how the SIZE function affects storage configuration.

The following illustrates the User Instruction Form for the GNAP program.

				SIZE>40
STEP	**INSTRUCTIONS**	**INPUT**	**FUNCTION**	**DISPLAY**
1	Initialize the GNAP program		[XEQ] GNAP [R/S] 2	GNAP NODES=?
2	Key in: number of nodes number of branches	 N B	 [R/S] [R/S] [R/S] 2	 BRANCHES=? N=(N)B=(B)1 BRANCH 1
3	Key in each branch element: a) Resistance (Ohms) or b) Capacitance (Farads) or c) Inductance (Henrys) and enter branch nodes or d) Transconductance (Siemens)	 R C L FR. TO gm	 [A] [B] [C] [R/S] [D]	 NODES: FR. TO=? NODES: FR. TO=? NODES: FR. TO=? BRANCH(n+1) INPUT: V+.V−=?

A WORD ABOUT PROGRAM USAGE

Catalog

When an Application Module is plugged into a port of the HP-41C, the contents of the Module can be reviewed by pressing [shift] [CATALOG] 2 (the Extension Catalog). Executing the [CATALOG] function lists the name of each program or function in the Module, as well as functions of any other extensions which might be plugged in.

Overlays

Overlays have been included for some of the programs in this Pac. To run the program, choose the appropriate overlay, and place it on the calculator. The mnemonics on the overlay are provided to help you run the program. The program's name is given vertically on the left side. When the calculator is in USER mode, a blue mnemonic identifies the key directly above it. Gold mnemonics are similar to blue mnemonics, except that they are above the appropriate key and the shift (gold) key must be pressed before the re-defined key. Once again, USER mode must be set.

ALPHA and USER Mode Notation

This manual uses a special notation to signify ALPHA mode. Whenever a statement on the User Instruction Form is printed in gold, the [ALPHA] key must be pressed before the statement can be keyed in. After the statement is input, press [ALPHA] again to return the calculator to its normal operating mode, or to begin program execution. For example, [XEQ] GNAP means press the following keys: [XEQ] [ALPHA] GNAP [ALPHA].

When the calculator is in USER mode, this manual will use the symbols [A] – [J] and [shift] [A] – [shift] [E] to refer to the reassigned keys in the top two rows. These key designations will appear on the User Instruction Form and in the keystroke solutions to sample problems.

Optional HP-82143A Printer

When the optional printer is plugged into the HP-41C along with the Circuit Analysis Application Module, all results will be printed automatically. You may also want to keep a permanent record of the values input to a certain program. A convenient way to do this is to set the Print Mode switch to NORMAL before running the program. In this mode, all input values and the corresponding keystrokes will be listed on the printer, thus providing a record of the entire operation of the program.

Using Programs as Subroutines

The programs in this Pac may be called as subroutines for user programs in the HP-41C's program memory. Refer to Appendix B for information on special subroutine calling points.

Downloading Module Programs

If you wish to trace execution, to modify, or to record on magnetic cards a program in this Application Module, it must first be copied into the HP-41C's program memory. For information concerning the HP-41C's COPY function, see the Owner's Handbook. It is not necessary to copy a program in order to run it.

Program Interruption

These programs have been designed to operate properly when run from beginning to end, without turning the calculator off (remember, the calculator may turn itself off). If the HP-41C is turned off, it may be necessary to set flag 21 (SF 21) to continue proper execution.

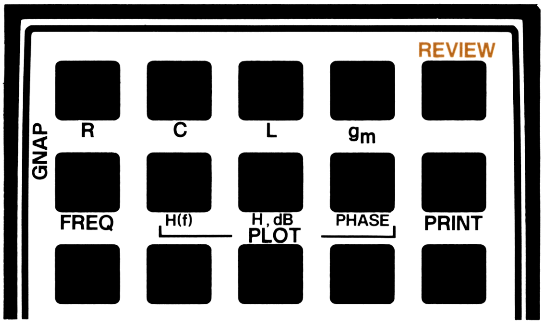
Use of Labels

You should generally avoid writing programs into the calculator memory that use program labels identical to those in your Application Module. In case of a label conflict, the label within program memory has priority over the label within the Application Pac program.

Assigning Program Names

Key assignments to keys [A] – [J] and [■] [A] – [■] [E] take priority over the automatic assignments of local labels in the Application Module. Be sure to clear previously assigned functions before executing a Module program.

GENERAL NETWORK ANALYSIS PROGRAM



This program analyzes electrical networks, computing amplitude and phase of the transfer function $V_2(s)/V_1(s)$. If the optional HP-82143A printer is used, the results may be either printed or plotted. The network elements allowed are resistors, capacitors, inductors, and voltage-controlled current sources. The size of the circuit that can be handled by the program depends on the number of memory registers available. The following table indicates the number of nodes, N, and branches, B, that can be analyzed with three memory modules. The number of registers needed for a circuit is $2N^2 + 3B + 29$.

POSSIBLE CIRCUIT CONFIGURATIONS

Number of Memory Modules

0		1		2		3	
N	B	N	B	N	B	N	B
2	8	2	30	2	51	2	72
3	5	3	26	3	48	3	69
		4	22	4	43	4	64
		5	16	5	37	5	58
		6	8	6	30	6	51
				7	21	7	42
				8	11	8	32
						9	21

Assuming you have set the minimum size of 28, the GNAP program begins by asking you for the size of your circuit and then tests to determine if there is enough storage before it begins. If there is insufficient storage, the message "SET SIZE NNN" warns you that the number of data registers must be increased. When numbering the nodes in your circuit, be sure that node 0 is ground, node 1 is the input node, and node 2 is the node whose voltage you wish to determine.

Analysis Algorithm

For any network, a matrix called the "nodal admittance matrix" can be written.* This matrix gives the relationship between the node voltages and the branch currents:

$$\mathbf{Y}_n \mathbf{V}_n = \mathbf{A}\,\mathbf{I} \tag{1}$$

where:

- $\mathbf{A}$ is the incidence matrix
- $\mathbf{V}_n$ is the node-voltage vector
- $\mathbf{I}$ is the source-current vector
- $\mathbf{Y}_n$ is the nodal admittance matrix

The algorithm assumes that our network is driven only by a current source of 1 ampere flowing from the ground node, node 0, into the input node, node 1. Equation (1) can then be written as

$$\mathbf{Y}_n \mathbf{V}_n = \begin{bmatrix} 1 \\ 0 \\ 0 \\ \cdot \\ \cdot \\ \cdot \end{bmatrix} \tag{2}$$

This equation could be solved explicitly for each node voltage by multiplying both sides on the left by $\mathbf{Y}_n^{-1}$.

$$\mathbf{V}_n = \mathbf{Y}_n^{-1} \begin{bmatrix} 1 \\ 0 \\ 0 \\ \cdot \\ \cdot \\ \cdot \end{bmatrix} \tag{3}$$

But since we only need the ratio V_2/V_1, it is not necessary to invert $\mathbf{Y}_n$. Instead, we can use Gaussian elimination to transform $\mathbf{Y}_n$ into a lower triangular matrix.

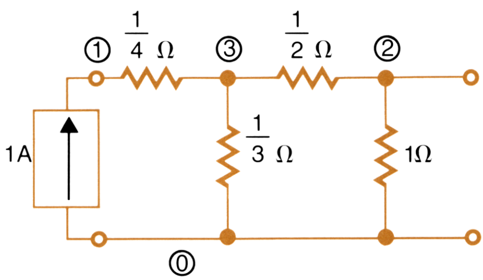
$$\begin{bmatrix} a_{11}\ 0\ 0\ 0 & \cdots\cdots\cdots \\ a_{21}\ a_{22}\ 0\ 0 & \cdots\cdots\cdots \\ a_{31}\ a_{32}\ a_{33}\ 0 & \cdots\cdots\cdots \\ \cdots\cdots\cdots & \cdots\cdots\cdots \\ \cdots\cdots\cdots & \cdots\cdots\cdots \\ \cdots\cdots\cdots & \cdots\cdots\cdots \\ a_{n1}\ a_{n2}\ a_{n3} & \cdots\cdots\ a_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ \cdot \\ \cdot \\ \cdot \\ V_n \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ \cdot \\ \cdot \\ \cdot \\ 0 \end{bmatrix} \tag{4}$$

*See Balabanian & Bickart, *Electrical Network Theory*, Wiley, New York, 1969 or equivalent.

Then we compute the desired ratio by solving the second equation, obtained from (4).

$$\frac{V_2}{V_1} = -\frac{a_{21}}{a_{22}} \tag{5}$$

To illustrate this procedure, consider this circuit:



By using the techniques of Sec. 2.4 of Balabanian, we can write the Y_n matrix

$$Y_n = \begin{bmatrix} 4 & 0 & -4 \\ 0 & 3 & -2 \\ -4 & -2 & 9 \end{bmatrix}$$

Multiplying the third row by $\frac{2}{9}$ and adding it to the second, we get

$$Y_n = \begin{bmatrix} 4 & 0 & -4 \\ -\frac{8}{9} & \frac{23}{9} & 0 \\ -4 & -2 & 9 \end{bmatrix}$$

Since we don't need to triangularize past the second row, we have

$$\frac{V_2}{V_1} = \frac{8}{23} = -9.17 \text{ dB}$$

For circuits containing reactive components, the above procedure is carried out in the same way except that all operations are done with complex numbers. The GNAP program works with a real conductance matrix, G, and an imaginary susceptance matrix, B.

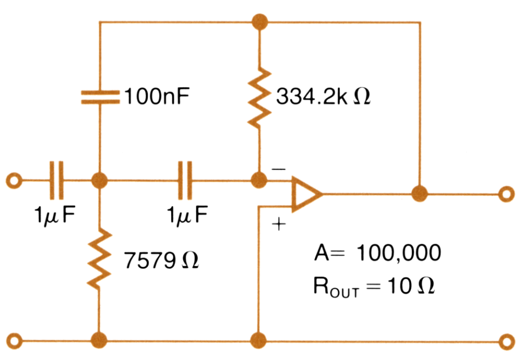
You might get the message DATA ERROR if there is a resonant subnetwork in your circuit and the frequency being used is the exact resonant frequency. If this condition occurs, it will be necessary to alter your input frequency slightly.

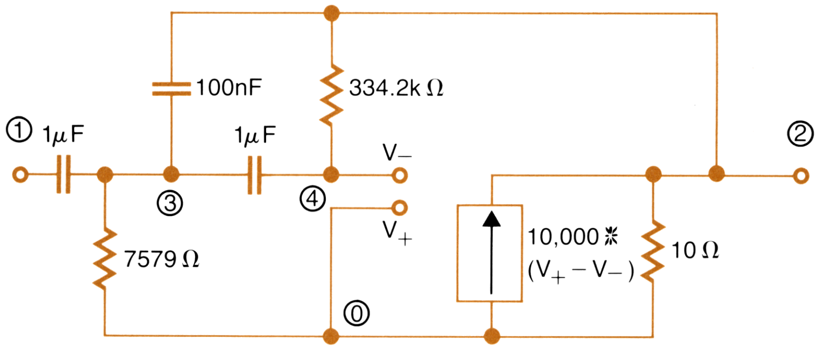
STEP	INSTRUCTIONS	INPUT	FUNCTION	SIZE>40 DISPLAY
1	Initialize the GNAP program		[XEQ] GNAP [R/S] [2]	GNAP NODES=?
2	Key in: number of nodes number of branches	 N B	 [R/S] [R/S] [R/S] [2]	 BRANCHES=? N=(N)B=(B)[1] BRANCH 1
3	Key in each branch element: a) Resistance (Ohms)	 R	 [A]	 NODES: FR. TO=?
	or b) Capacitance (Farads)	C	[B]	NODES: FR. TO=?
	or c) Inductance (Henrys)	L	[C]	NODES: FR. TO=?
	and enter branch nodes[3]	FR. TO	[R/S]	BRANCH(n+1)
	or d) Transconductance (Siemens)	gm	[D]	INPUT: V+.V−=?
	and enter voltage control	V+.V−	[R/S]	OUTPUT: IL.IE=?
	and current nodes (current leaves . current enters)	IL.IE	[R/S]	BRANCH (n+1)
	Repeat step 3 for all branches. When done with all,			DONE
4	(OPTIONAL) To review the circuit:		■ [E] [R/S] [2] :	BRANCH 1 (List of Input) :
5	Specify the frequency sweep: Key in: Lowest Frequency Highest Frequency **frequency increment**[4]	 f_{MIN} f_{MAX} Δf	[F] [R/S] [R/S] [R/S]	FMIN=? FMAX=? F INCR=? READY
6	To compute and list results: Press [R/S] until results have been obtained for all frequencies.		[J] [R/S] [2] [R/S] [2] [R/S] [2] :	frequency magnitude magnitude,dB phase :
	[1] If SET SIZE NNN appears, you need more data registers. Set SIZE as indicated and continue by pressing [R/S]. [2] **If you are using the printer these Run/Stops are not required.** [3] The grounded NODE of a passive branch must be the TO node. [4] **If Δf is entered as a negative value, the program uses Δ as a multiplicative increment.**			

STEP	INSTRUCTIONS	INPUT	FUNCTION	DISPLAY
7	To plot the results (assuming you have an HP-82143A printer attached), select desired plot:			
	a) magnitude		[G]	YMIN=?
	or b) magnitude in dB		[H]	YMIN=?
	or c) Phase		[I]	YMIN=?
8	Specify plot parameters: Key in			
	a) Y_{MIN}	Y_{MIN}	[R/S]	YMAX=?
	b) Y_{MAX}	Y_{MAX}	[R/S]	AXIS=?
	c) x-axis (y-intercept)	x-axis[5]	[R/S]	
	[5] You may suppress printing of the x-axis by placing any alpha character in the alpha display, e.g.; [ALPHA] NO AXIS [R/S] causes "NO AXIS" to be stored as the y-intercept and no axis will be plotted.			

Example 1:

Compute the magnitude and phase response for this active filter. It was designed to be a high-pass filter with a 10-Hz cutoff frequency, passband gain of 20 dB, and α-peaking factor of 1.





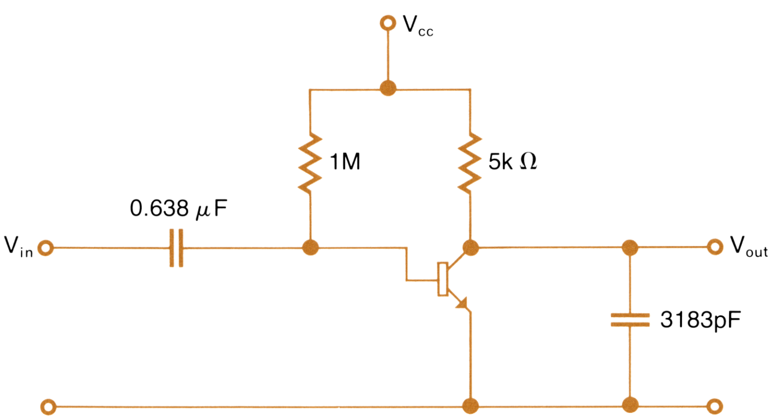
Keystrokes	Display
XEQ ALPHA SIZE ALPHA 082	
XEQ ALPHA GNAP ALPHA	*GNAP*
R/S	*NODES?*
4 R/S	*BRANCHES?*
7 R/S	*N=4 B=7*
R/S	*BRANCH 1*
1 EEX CHS 6 B	*NODES: FR.TO=?*
1.03 R/S	*BRANCH 2*
7579 A	*NODES: FR.TO=?*
3 R/S	*BRANCH 3*
1 EEX CHS 6 B	*NODES: FR.TO=?*
3.04 R/S	*BRANCH 4*
100 EEX CHS 9 B	*NODES: FR.TO=?*
3.02 R/S	*BRANCH 5*
334200 A	*NODES: FR.TO=?*
4.02 R/S	*BRANCH 6*
10000 D	*INPUT: V+.V−=?*
.04 R/S	*OUTPUT: IL.IE=?*
.02 R/S	*BRANCH 7*
10 A	*NODES: FR.TO=?*
2 R/S	*DONE*
F	*FMIN=?*
1 R/S	*FMAX=?*
100 R/S	*F INCR=?*
10 USER √x USER CHS R/S	*READY*

These keystrokes assume the printer is not being used.

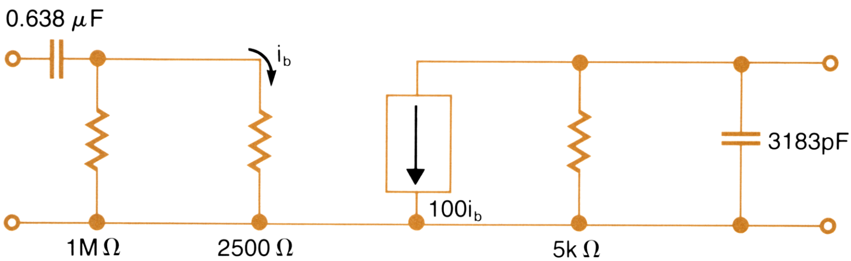
Keystrokes	Display
[J]	*F=1.00*
[R/S]	*H=0.10*
[R/S]	*H=−19.96dB*
[R/S]	*∠=−5.77*
[R/S]	*F=3.16*
[R/S]	*H=1.05*
[R/S]	*H=0.41dB*
[R/S]	*∠=−19.36*
[R/S]	*F=10.00*
[R/S]	*H=10.00*
[R/S]	*H=20.00dB*
[R/S]	*∠=−90.00*
[R/S]	*F=31.62*
[R/S]	*H=10.48*
[R/S]	*H=20.41dB*
[R/S]	*∠=−160.64*
[R/S]	*F=100.00*
[R/S]	*H=10.05*
[R/S]	*H=20.04dB*
[R/S]	*∠=−174.23*

Example 2:

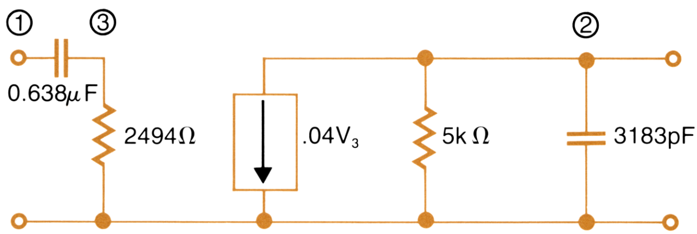
Create a Bode plot for this transistor amplifier.



First transform the circuit using an h-parameter model.

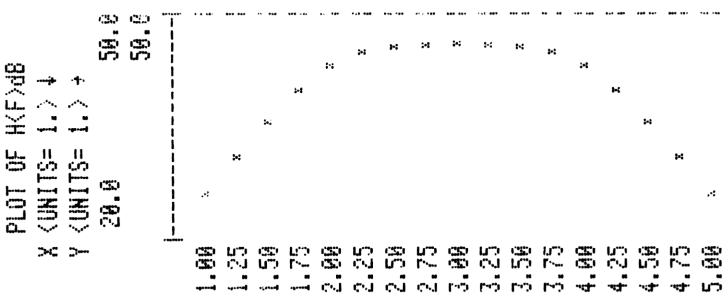


Then replace the current-controlled current source with a voltage-controlled current source.



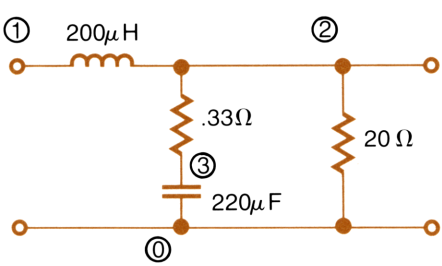
Keystrokes	**Display**	
XEQ ALPHA SIZE ALPHA 062		
XEQ ALPHA GNAP ALPHA	*GNAP*	These keystrokes assume a printer is being used.
	NODES?	
3 R/S	*BRANCHES?*	
5 R/S	*N=3 B=5*	
	BRANCH 1	
.638 EEX CHS 6 B	*NODES: FR.TO=?*	
1.03 R/S	*BRANCH 2*	
2494 A	*NODES: FR.TO=?*	
3 R/S	*BRANCH 3*	
.04 D	*INPUT: V+.V−=?*	
3 R/S	*OUTPUT:IL.IE=?*	
2 R/S	*BRANCH 4*	
5000 A	*NODES: FR.TO=?*	
2 R/S	*BRANCH 5*	
3183 EEX CHS 12 B	*NODES: FR.TO=?*	
2 R/S	*DONE*	
E	*B 1.*	Review the circuit description
	C=638.0E−9	
	NODES: 1.0300	
	B 2.	
	R=2.494E3	
	NODES: 3.0000	

Keystrokes	Display	
	B 3.	
	GM=40.00E−3	
	NODES: 300.0200	(V+ V− .ILIE)
	B 4.	
	R= 5.000E3	
	NODES: 2.0000	
	B 5.	
	C=3.183E−9	
	NODES: 2.0000	
[F]	***FMIN=?***	
10 [R/S]	***FMAX=?***	
1 [EEX] 5 [R/S]	***F INCR =?***	Four steps per decade.
10 [USER] [√x] [√x] [USER] [CHS] [R/S]	***READY***	
[H]	***YMIN=?***	
20 [R/S]	***YMAX=?***	
50 [R/S]	***AXIS=?***	
50 [R/S]		

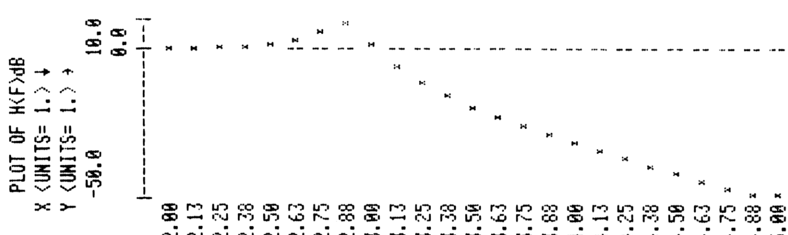


Example 3:

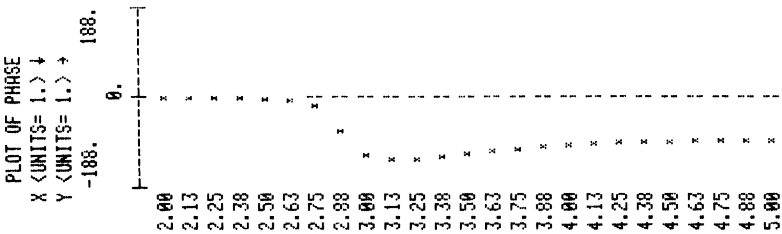
Analyze this circuit from 100 Hz to 100 kHz. Make Bode plots using a multiplicative frequency increment of $10^{1/8}$.



Keystrokes	Display	
[XEQ] [ALPHA] SIZE [ALPHA] 059		If SIZE > 59, ignore this line.
[XEQ] [ALPHA] GNAP [ALPHA]	*GNAP*	These keystrokes
	NODES?	assume a printer
3 [R/S]	*BRANCHES?*	is being used.
4 [R/S]	*N=3 B=4*	
	BRANCH 1	
200 [EEX] [CHS] 6 [C]	*NODES: FR.TO=?*	
1.02 [R/S]	*BRANCH 2*	
.33 [A]	*NODES: FR.TO=?*	
2.03 [R/S]	*BRANCH 3*	
220 [EEX] [CHS] 6 [B]	*NODES: FR.TO=?*	
3 [R/S]	*BRANCH 4*	
20 [A]	*NODES: FR.TO=?*	
2 [R/S]	*DONE*	
[F]	*FMIN=?*	
100 [R/S]	*FMAX=?*	
1 [EEX] 5 [R/S]	*F INCR =?*	
10 [USER] [√x] [√x] [√x] [USER] [CHS]		
[R/S]	*READY*	
[H] ([J] if you have no printer)	*YMIN=?*	
50 [CHS] [R/S]	*YMAX=?*	
10 [R/S]	*AXIS=?*	
0 [R/S]		



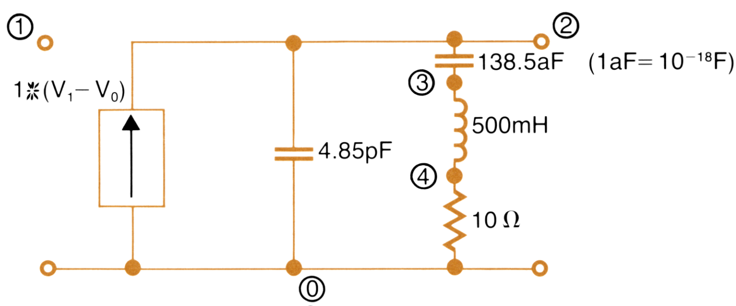
Keystrokes	Display
[I]	*YMIN=?*
188 [CHS] [R/S]	*YMAX=?*
188 [R/S]	*AXIS=?*
0 [R/S]	



Example 4:

You can use programs of your own to put any desired label on a plot. Store Ymin, Ymax, Axis, and the Label. Then execute PRPLOTP.

This example shows how to use a Voltage-Controlled Current Source to determine the input impedance of a circuit and how to plot it with the label "Z IN."



19.125 MHz Crystal Model

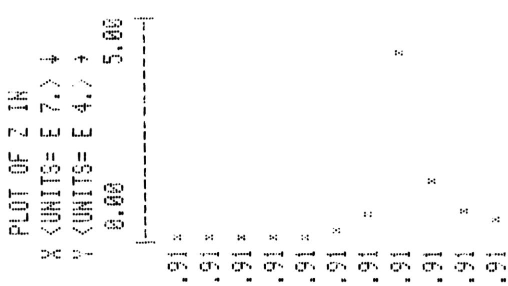
First build the circuit.

Keystrokes	Display	
[XEQ] [ALPHA] SIZE [ALPHA] 076		These keystrokes assume the printer is being used.
[XEQ] [ALPHA] GNAP [ALPHA]	*GNAP*	
	NODES?	
4 [R/S]	*BRANCHES?*	
5 [R/S]	*N=4 B=5*	
	BRANCH 1	
1 [D]	*INPUT: V+.V−=?*	

Keystrokes	Display
1 [R/S]	*OUTPUT:IL.IE=?*
.02 [R/S]	*BRANCH 2*
4.85 [EEX] [CHS] 12 [B]	*NODES: FR.TO=?*
2 [R/S]	*BRANCH 3*
138.5 [EEX] [CHS] 18 [B]	*NODES: FR.TO=?*
2.03 [R/S]	*BRANCH 4*
500 [EEX] [CHS] 3 [C]	*NODES: FR.TO=?*
3.04 [R/S]	*BRANCH 5*
10 [A]	*NODES: FR.TO=?*
4 [R/S]	*DONE*
[F]	*FMIN=?*
19125300 [R/S]	*FMAX=?*
19125800 [R/S]	*F INCR=?*
50 [R/S]	*READY*

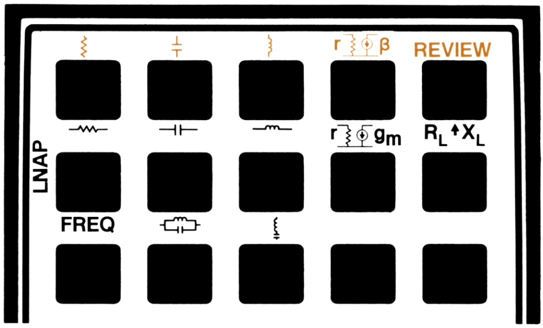
Then write this short program.

Keystrokes	Display	
[■] [GTO] [•] [•]	*PACKING*	
[PRGM]		
[■] [LBL] [ALPHA] Z IN [ALPHA]	*01 LBL Z IN*	
[■] [GTO] [ALPHA] H<F> [ALPHA]	*02 GTO H<F>*	
[PRGM]		
0 [STO] 00		Ymin*
50000 [STO] 01		Ymax
[ALPHA] Z IN [■] [STO] 04		No Axis
[■] [STO] 11 [ALPHA]		Name
[XEQ] [ALPHA] PRPLOTP [ALPHA]		



*For a description of the function PRPLOTP and the registers used to store its plot parameters, see your **Printer Owner's Handbook.**

LADDER NETWORK ANALYSIS PROGRAM



This program analyzes ladder networks of up to 107 branches providing amplitude and phase of various transfer functions, either printed or plotted. Network elements allowed are resistors, capacitors, inductors, series and parallel inductor-capacitor combinations, voltage-controlled current sources, current-controlled current sources, transformers, gyrators, transmission lines, open stub lines, and shorted stub lines. Transfer functions computed are V_2/V_1, I_2/I_1, P_2/P_1 and Z_{in}.

Network size is determined by the number of memory modules present. The maximum number of branches possible is 107.

Memory Modules	Branches (maximum)
0	11
1	43
2	75
3	107

If SIZE is not large enough, the display will show "NONEXISTENT." You may execute SIZE with a larger argument and then press [R/S] to resume execution of the program. You need at least 40 + 2 × (number of elements) data registers to run this program. Some elements require three storage registers.

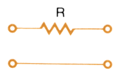
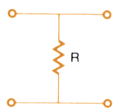
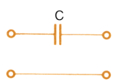
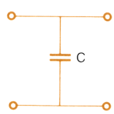
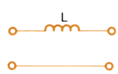
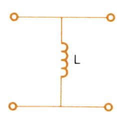
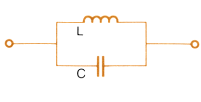
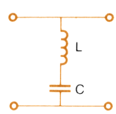
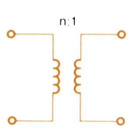
Theoretical Basis of Ladder Network Analysis Program

The operation of this program is based on the fact that the chain-parameter matrix of two cascaded circuits is equal to the product of their individual chain-parameter matrices. Circuit elements are stored as they are input from left to right. Then at each frequency the individual chain-parameter matrices are formed and multiplied to gradually compute the overall matrix. Finally, the desired transfer function is computed.

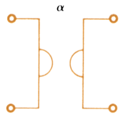
The chain-parameter matrix is defined by the following sketch and matrix equation. ч is the Cyrillic letter "cha".

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \text{ч}_{11} & \text{ч}_{12} \\ \text{ч}_{21} & \text{ч}_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

The circuit elements allowed by this program are shown below with their ч-matrices.

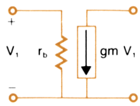
Name	Circuit	Chain-Parameter Matrix
RS Series Resistor		$\text{ч} = \begin{bmatrix} 1\angle 0 & R\angle 0 \\ 0 & 1\angle 0 \end{bmatrix}$
RP Parallel Resistor		$\text{ч} = \begin{bmatrix} 1\angle 0 & 0 \\ \frac{1}{R}\angle 0 & 1\angle 0 \end{bmatrix}$
CS Series Capacitor		$\text{ч} = \begin{bmatrix} 1\angle 0 & \frac{1}{\omega C}\angle -90 \\ 0 & 1\angle 0 \end{bmatrix}$
CP Parallel Capacitor		$\text{ч} = \begin{bmatrix} 1\angle 0 & 0 \\ \omega C\angle 90 & 1\angle 0 \end{bmatrix}$
LS Series Inductor		$\text{ч} = \begin{bmatrix} 1\angle 0 & \omega L\angle 90 \\ 0 & 1\angle 0 \end{bmatrix}$
LP Parallel Inductor		$\text{ч} = \begin{bmatrix} 1\angle 0 & 0 \\ \frac{1}{\omega L}\angle -90 & 1\angle 0 \end{bmatrix}$
LCS Series L-C		$\text{ч} = \begin{bmatrix} 1\angle 0 & \frac{\omega L}{1-\omega^2 LC}\angle 90 \\ 0 & 1\angle 0 \end{bmatrix}$
LCP Parallel L-C		$\text{ч} = \begin{bmatrix} 1\angle 0 & 0 \\ \frac{\omega C}{1-\omega^2 LC}\angle 90 & 1\angle 0 \end{bmatrix}$
TF Transformer		$\text{ч} = \begin{bmatrix} n\angle 0 & 0 \\ 0 & \frac{1}{n}\angle 0 \end{bmatrix}$

GY Gyrator



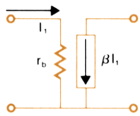
$$\mathcal{A} = \begin{bmatrix} 0 & \alpha\angle 0 \\ \frac{1}{\alpha}\angle 0 & 0 \end{bmatrix}$$

VCIS Voltage-Controlled Current Source



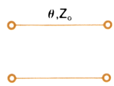
$$\mathcal{A} = \begin{bmatrix} 0 & -\frac{1}{g_m}\angle 0 \\ 0 & -\frac{1}{r_b g_m}\angle 0 \end{bmatrix}$$

ICIS Current-Controlled Current Source



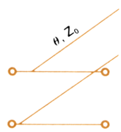
$$\mathcal{A} = \begin{bmatrix} 0 & -\frac{r_b}{\beta}\angle 0 \\ 0 & -\frac{1}{\beta}\angle 0 \end{bmatrix}$$

LINE Transmission Line



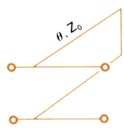
$$\mathcal{A} = \begin{bmatrix} \cos\theta\angle 0 & Z_0 \sin\theta\angle 90 \\ \frac{\sin\theta}{Z_0}\angle 90 & \cos\theta\angle 0 \end{bmatrix}$$

STUBO Open Stub



$$\mathcal{A} = \begin{bmatrix} 1\angle 0 & 0 \\ \frac{\tan\theta}{Z_0}\angle 90 & 1\angle 0 \end{bmatrix}$$

STUBS Shorted Stub



$$\mathcal{A} = \begin{bmatrix} 1\angle 0 & 0 \\ \frac{\cot\theta}{Z_0}\angle -90 & 1\angle 0 \end{bmatrix}$$

Any of the following transfer functions may be computed from the overall chain-parameter matrix.

Input impedance

$$|Z_{in}| = \frac{\mathcal{A}_{11} Z_L + \mathcal{A}_{12}}{\mathcal{A}_{21} Z_L + \mathcal{A}_{22}}$$

Forward transfer admittance

$$\left|\frac{I_2}{V_1}\right| = \frac{-1}{\mathcal{A}_{11} Z_1 + \mathcal{A}_{12}}$$

Power Gain

$$\left|\frac{P_{out}}{P_{in}}\right| = \left|\frac{I_2}{I_1}\right|^2 \frac{\mathrm{Re}\{Z_L\}}{\mathrm{Re}\{Z_{in}\}}$$

Current transfer ratio

$$\left|\frac{I_2}{I_1}\right| = \frac{-1}{\mathcal{A}_{21} Z_L + \mathcal{A}_{22}}$$

Voltage transfer ratio

$$\left|\frac{V_2}{V_1}\right| = \frac{Z_L}{\mathcal{A}_{11} Z_L + \mathcal{A}_{12}}$$

Forward transfer impedance

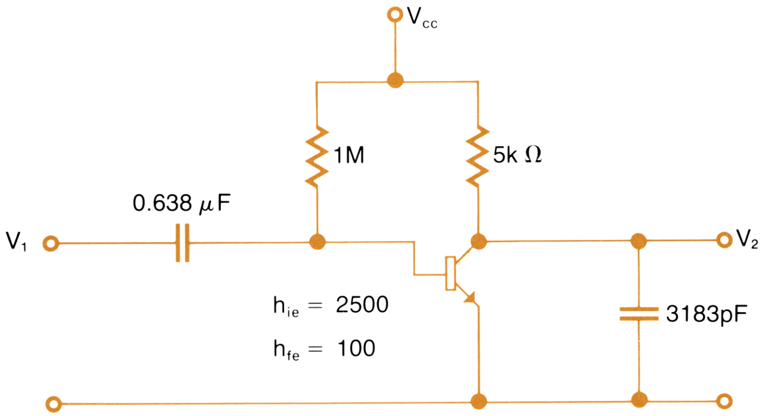
$$\left|\frac{V_2}{I_1}\right| = \frac{Z_L}{\mathcal{A}_{21} Z_L + \mathcal{A}_{22}}$$

				SIZE >50
STEP	INSTRUCTIONS	INPUT	FUNCTION	DISPLAY
1	Initialize the Ladder Network Analysis Program		[XEQ] LNAP [R/S] *	LNAP BEGIN INPUT
2	Input circuit elements one at a time starting at the left.			
	Series Resistor	R	[A]	RS= (R)
	Parallel Resistor	R	[■] [A]	RP= (R)
	Series Capacitor	C	[B]	CS= (C)
	Parallel Capcitor	C	[■] [B]	CP= (C)
	Series Inductor	L	[C]	LS= (L)
	Parallel Inductor	L	[■] [C]	LP= (L)
	Voltage-Controlled Current Source	r g_m	[ENTER↑] [D]	VCIS= (r), (gm)
	Current-Controlled Current Source	r β	[ENTER↑] [■] [D]	ICIS= (r), (β)
	Series L-C	L C	[ENTER↑] [G]	LCS= (L), (C)
	Parallel L-C	L C	[ENTER↑] [H]	LCP= (L), (C)
	Transformer	n	[XEQ] TF	TF= (n)
	Gyrator	α	[XEQ] GY	GY= (α)
	Transmission Line ($\theta = \frac{\text{electrical length}}{f_0}$)	θ Z_o	[ENTER↑] [XEQ] LINE	LINE= (θ), (Z_o)
	Open Stub	θ Z_o	[ENTER↑] [XEQ] STUBO	STUBO= (θ), (Z_o)
	Shorted Stub	θ Z_o	[ENTER↑] [XEQ] STUBS	STUBS= (θ), (Z_o)
3	Input load impedance:	R_L X_L	[ENTER↑] [E]	
4	(Optional) Review the circuit. Press [R/S] to see successive branches. *This [R/S] is not needed if you are using a printer.		[■] [E]	

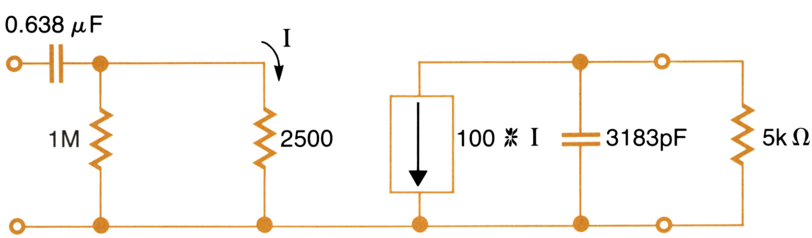
STEP	INSTRUCTIONS	INPUT	FUNCTION	DISPLAY
5	Select frequency sweep		[F]	FMIN=?
	Minimum frequency	f_{MIN}	[R/S]	FMAX=?
	Maximum frequency	f_{MAX}	[R/S]	FINCR=?
	Frequency increment (negative value indicates multiplicative increment)	Δf	[R/S]	FUNCTION?
6	To output results, key in a list-function name. (The calculator is already in ALPHA mode.)			
	Transfer voltage ratio	V2/V1	[R/S]	
	Transfer current ratio	I2/I1	[R/S]	
	Power ratio	P2/P1 *	[R/S]	
	Input Impedance	ZIN	[R/S]	
	All of the above	ALL	[R/S]	
7	To plot results, key in the desired plot-function name. (The calculator is already in ALPHA mode.)			
	Plot Magnitude of V2/V1		PV	YMIN=?
	Plot Magnitude of V2/V1 in dB		PVdB	YMIN=?
	Plot Angle of V2/V1		P∠V	YMIN=?
	Plot Magnitude of I2/I1		PI	YMIN=?
	Plot Magnitude of I2/I1 in dB		PIdB	YMIN=?
	Plot Angle of I2/I1		P∠I	YMIN=?
	Plot Magnitude of ZIN		PZIN	YMIN=?
	Plot Angle of ZIN		P∠ZIN	YMIN=?
8	Specify plotting information	Y_{MIN}	[R/S]	YMAX=?
		Y_{MAX}	[R/S]	AXIS=?
	(Any alpha-data input yields no axis)	axis	[R/S]	
9	When the plot is complete, you may return to step 1, step 3, or step 5. If you wish to return to step 6, press		[J]	FUNCTION?
	*This is the **real** power ratio as only the real portions of Z_L and Z_{in} are considered.			

Example 1:

Make Bode plots (magnitude and phase) of V_2/V_1 for this transistor amplifier.

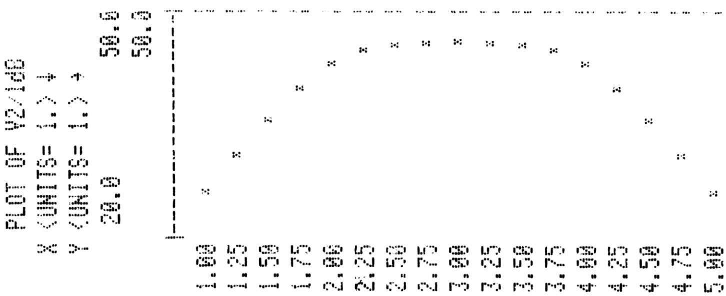


Transform the circuit using an h-parameter model.



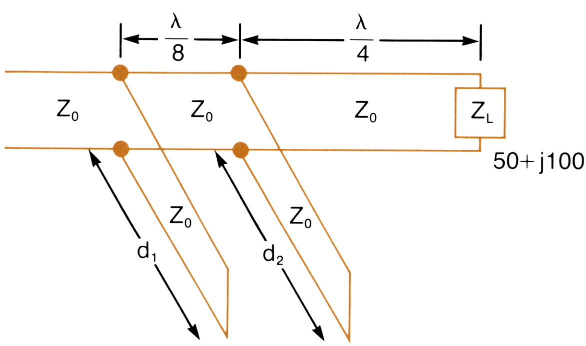
Keystrokes	Display
■ [FIX] 2	
[XEQ] [ALPHA] SIZE [ALPHA] 051	
[XEQ] [ALPHA] LNAP [ALPHA]	***LNAP***
[R/S]	***BEGIN INPUT***
.638 [EEX] [CHS] 6 [B]	***CS=6.38E−7***
1 [EEX] 6 ■ [A]	***RP=1,000,000.00***
2500 [ENTER↑] 100 ■ [D]	***ICIS=2,500.00,100.00***
3183 [EEX] [CHS] 12 ■ [B]	***CP=3.18E−9***
5000 [ENTER↑] 0 [E]	***ZL=5,000.00+J0.00***
[F]	***FMIN = ?***
10 [R/S]	***FMAX = ?***
100000 [R/S]	***FINCR = ?***
10 [USER] [√x] [√x] [USER] [CHS] [R/S]	***FUNCTION?***

PVdB [R/S]	*YMIN = ?*	If you have no printer, V2/V1 [R/S] will cause individual values to be output.
20 [R/S]	*YMAX = ?*	
50 [R/S]	*AXIS = ?*	
50 [R/S]		



Example 2:

If the stub lengths, d1 and d2, are 54° and 49.68° respectively, what is the input impedance of this double-stub tuner? (Z_0 is 100 Ω)

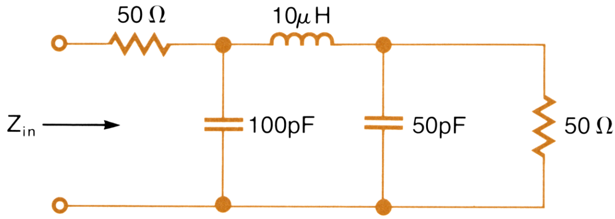


Keystrokes	**Display**	
[ ] [FIX] 2		
[XEQ] [ALPHA] SIZE [ALPHA] 053		
[XEQ] [ALPHA] LNAP [ALPHA]	*LNAP*	
[R/S]	*BEGIN INPUT*	
54 [ENTER↑]		
100 [XEQ] [ALPHA] STUBS [ALPHA]	*STUBS=54.00,100.00*	You might like to assign STUBS to a key, say [ ] [x≷y].
45 [ENTER↑]		
100 [XEQ] [ALPHA] LINE [ALPHA]	*LINE=45.00,100.00*	
49.68 [ENTER↑]		

Keystrokes	Display
100 [XEQ] [ALPHA] STUBS [ALPHA]	*STUBS=49.68,100.00*
90 [ENTER↑]	
100 [XEQ] [ALPHA] LINE [ALPHA]	*LINE=90.00,100.00*
50 [ENTER↑] 100 [E]	*ZL=50.00+J100.00*
[F]	*FMIN = ?*
1 [R/S]	*FMAX = ?*
[R/S]	*FINCR = ?*
[R/S]	*FUNCTION?*
ZIN [R/S]	*F=1.00*
[R/S]	*ZIN=97.00*
[R/S]	*∠−1.27*
[R/S]	*ZIN = 96.97*
[R/S]	*+J − 2.15*

Example 3:

What is the input impedance of the circuit shown at 1 MHz and 10 MHz?



Keystrokes	Display
[■] [FIX] 0	
[XEQ] [ALPHA] SIZE [ALPHA] 048	
[XEQ] [ALPHA] LNAP [ALPHA]	*LNAP*
[R/S]	*BEGIN INPUT*
50 [A]	*RS=50.*
100 [EEX] [CHS] 12 [■] [B]	*CP=1.E−10*
10 [EEX] [CHS] 6 [C]	*LS=1.E−5*
50 [EEX] [CHS] 12 [■] [B]	*CP=5.E−11*
50 [ENTER↑] 0 [E]	*ZL=50.+J0.*

Keystrokes	Display
[F]	*FMIN = ?*
1 [EEX] 6 [R/S]	*FMAX = ?*
10 [EEX] 6 [R/S]	*FINCR = ?*
9 [EEX] 6 [R/S]	*FUNCTION?*
ZIN [R/S]	*F=1,000,000.*
[R/S]	*ZIN=122.*
[R/S]	*∠31.*
[R/S]	*ZIN=104.*
[R/S]	*+J63.*
[R/S]	*F=10,000,000.*
[R/S]	*ZIN=221.*
[R/S]	*∠−75.*
[R/S]	*ZIN=56.*
[R/S]	*+J−213.*

PROGRAM DATA

Program	# Regs. to Copy		Data Registers			Flags	
GNAP	195	00	Ymin			05	S: Δf is multiplicative
		01	Ymax				C: Δf is additive
		02	PRPLOT scratch			06	S: Node is ground
		03	Plotting Character			07	S: Plot dB
		04	Axis			08	S: Plot phase
		05	PRPLOT scratch			09	S: Plot magnitude
		06	f				
		07	scaling multiplier				
		08	fmin				
		09	fmax				
		10	Δf				
		11	Plot Name				
		12					
		13	number of freqs				
		14	J		K		
		15	MJ	V+	JK		
		16	MM	V−	JJ		
		17	IJ	IL	KJ		
		18	IM	IE	KK		
		19	I		J		
		20	M.002				
		21	28+ 3b				
		22	maximum V2/V1				
		23	component-type pointer				
		24	component-value pointer				

Program	# Regs. to Copy	Data Registers		Flags	
LNAP	283	00	Ymin	5	S: Δf is multiplicative
					C: Δf is additive
		01	Ymax		
		02	PRPlot scratch	6	S: Don't print frequency
					C: Print frequency
		03	Plotting character		
		04	Axis	7	S: Plot magnitude in dB
		25			
		26	branches, b		
		27	nodes, n		
		28 to 27+ b	Component types		
		28+ b to 27+ 3b	Component values and nodes		
		28+ 3b to 28+ 3b+ n^2	G matrix (Re{Y})		
		to 27+ 3b+ $2n^2$	B matrix (Im {Y})		

05	PRPlot scratch	8	S: Plot phase
06	f	9	S: Plot magnitude
07	Scaling multiplier	10	S: Don't increment f
08	fmin	20	S: Always execute ※ An
09	fmax		C: Execute ※ An only once
10	f		
11	Plot Name		
12	Re $\{Y_{11}\}$		
13	Im $\{Y_{12}\}$		
14	Re $\{Y_{12}\}$		
15	Im $\{Y_{12}\}$		
16	Re $\{Y_{21}\}$		
17	Im $\{Y_{21}\}$		
18	Re $\{Y_{22}\}$		
19	Im $\{Y_{22}\}$		
20	Re $\{A\}$		
21	Im $\{A\}$		
22	Re $\{B\}$		
23	Im $\{B\}$		
24	Re $\{C\}$		
25	Im $\{C\}$		
26	Re $\{D\}$		
27	Im $\{D\}$		
28	Re $\{$temporary$\}$		

29	Im {temporary}
30	Pointer to next element
31	Number of elements, n
32	RL
33	XL
34	Re $\{Y_{11}Z_L + Y_{12}\}$
35	Im $\{Y_{11}Z_L + Y_{12}\}$
36	Re $\{Y_{21}Z_L + Y_{22}\}$
37	Im $\{Y_{21}Z_L + Y_{22}\}$
38	not used
39	not used
40	List
	of
	network
	elements
	and
45	values
	.
	.
	.

Appendix B

SUBROUTINES

This table provides information necessary to use various portions of the Circuit Analysis Application Module as subroutines.

SUBROUTINE	LABEL	INITIAL REGISTERS	FLAG STATUS	FINAL REGISTERS	REMARKS
Complex Multiply	*C*	$t{:}V_2$ $z{:}U_2$ $y{:}V_1$ $x{:}U_1$		$y{:}\ \mathrm{Im}\{(U_1 + iV_1)*(U_2 + iV_2)\}$ $x{:}\ \mathrm{Re}\{(U_1 + iV_1)*(U_2 + iV_2)\}$	
Complex Add	*C+	$t{:}V_2$ $z{:}U_2$ $y{:}V_1$ $x{:}U_1$		$y{:}\ V_1 + V_2$ $x{:}\ U_1 + U_2$	
GNAP PRINT	*J	See Appendix A for detailed information regarding register contents and flag settings.			This label is provided so that a user-level program can initiate a GNAP analysis after the user has initially set up the circuit.

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