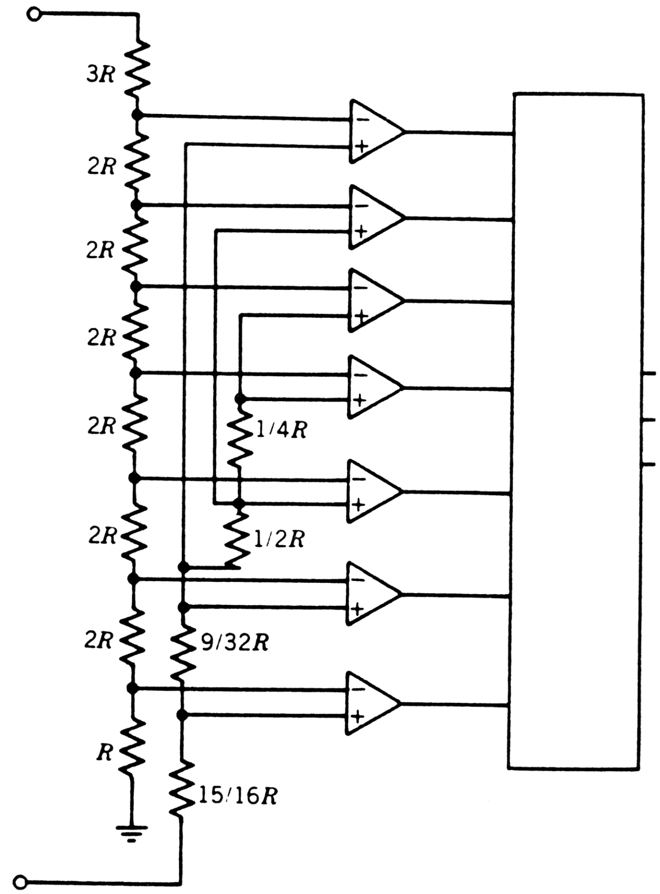
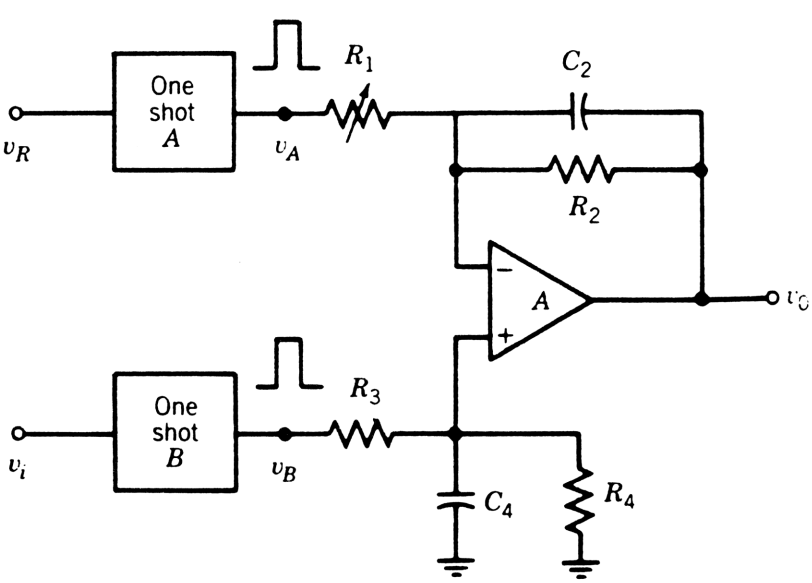
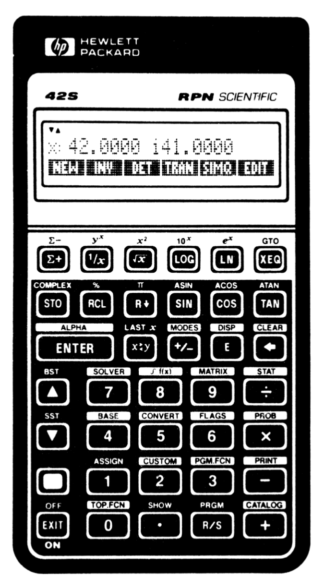
ADVANCED CIRCUIT ANALYSIS with the HP-42S







EduCALC
27953 Cabot Rd.
Laguna Niguel, CA

ADVANCED CIRCUIT ANALYSIS

With the HP-42S

by Robert R. Boyd

INTRODUCTION

The purpose of this work is to present a novel method of of circuit analysis developed by the author several years ago. The method is derived from Kirchoff's current law and results in a dimensionless coefficient matrix in place of the conventional admittance matrix. Using this method, matrix elements can be written by inspection of the circuit, without algebraic manipulation.

Section I presents the method of setting up the circuit matrices. Merely by labeling the voltage nodes to be analyzed, and the branch impedances connected to the nodes, the node equations can be written using the principle of superposition. It is not necessary to identify loops, trees, chords, links, etc., of the topology. One merely has to know how many impedances are connected to the node and which impedance is connected to the driving voltage. This information can be obtained from the cirult diagram. In addition, it is not necessary to convert sources to Norton or Thevenin equivalents.

With linear circuits that contain no dependent sources, the symmetric coefficient matrices using loop or node analysis are very easy to set up. This mnemonic method is presented in just about every undergraduate text on network analysis. However, when dependent sources are introduced, the symmetry disappears along with the mnemonic method. With the technique presented here, the symmetry of the coefficient matrix is of no concern.

Other HP calculators/computers can be used with the material in Section I. Some good choices are the HP-71B/Math Pac, the HP-28S*, or the HP-41CV/X/Advantage module. Of course, any computer that has complex matrix and double precision capabilities can be used as well.

Section II is exclusively for those readers with HP-42S calculators and familiarity with the operation of the calculator is assumed. Most of the circuits given in section I are analyzed with complete descriptions of the main programs. No attempt has been made to minimize the program code. The interested reader will probably see a better way to do it.

* See EduCalc book "Advanced Circuit Analysis with the HP-28S".

A PC AT or XT with P-Spice has some advantages over writing out the node equations and setting up the circuit matrices, no matter how easy and systematic the information herein makes it. There are also analog design workstations appearing on the market that are absolutely fantastic in their capabilities. However, a PC with P-Spice will run about $5,000 while the analog workstations are going for over $50,000. The HP-42S sells for under $100. Comparing capability per dollar, the method presented here using the HP-42S wins hands down.

EduCALC
27953 CABOT ROAD
LAGUNA NIGUEL, CA 92677

To my Wife LINDA: Prov 31:10-12

To my daughter JANA: Prov 31:29

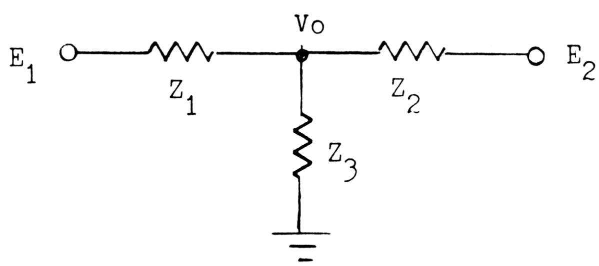
TABLE OF CONTENTS

SECTION I. Setting up The Circuit Matrices.

Notational convention:
- E => Independent voltage source
- V => Dependent voltage source or node voltage
- I => Dependent current source or node current
- Z => real or complex impedance

Two simple star networks will be analyzed to show a method of solving for the voltage at the center node that is easy to remember. This topology is chosen since any circuit can be formed by combining star networks with 2 or more branches. The method is then generalized to an N-branch star network.

<u>Example 1</u> Solve for Vo by superposition:
(N = 3)



a. Set $E_2 = 0$, $Vo \rightarrow Vo'$:

$$Vo' = \frac{E_1 \; Z_2//Z_3}{Z_1 + Z_2//Z_3} = \frac{E_1}{1 + \dfrac{Z_1}{Z_2//Z_3}}$$

Since $Z_2//Z_3 = \dfrac{1}{\dfrac{1}{Z_2} + \dfrac{1}{Z_3}}$,

$$Vo' = \frac{E_1}{1 + Z_1\left(\dfrac{1}{Z_2} + \dfrac{1}{Z_3}\right)}$$

b. Set $E_1 = 0$, $Vo \to Vo''$:

$$Vo'' = \frac{E_2\ Z_1//Z_3}{Z_2 + Z_1//Z_3} = \frac{E_2}{1 + \dfrac{Z_2}{Z_1//Z_3}}$$

$$Vo'' = \frac{E_2}{1 + Z_2\left(\dfrac{1}{Z_1} + \dfrac{1}{Z_3}\right)}$$

Then by the superposition principle,

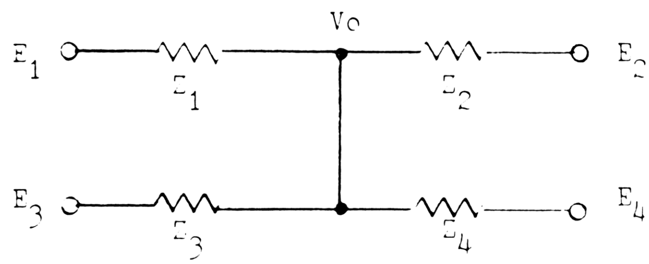
$$Vo = Vo' + Vo'' = \frac{E_1}{1 + Z_1\left(\dfrac{1}{Z_2} + \dfrac{1}{Z_3}\right)} + \frac{E_2}{1 + Z_2\left(\dfrac{1}{Z_1} + \dfrac{1}{Z_3}\right)}$$

$$= E_1K_1 + E_2K_2,$$

where K_1 and K_2 are dimensionless constants determined by Z_1, Z_2, & Z_3, and are always < 1.

We try a second example to see if there is a consistent pattern occurring.

Example 2 Solve for Vo by superposition:
(N = 4)



$$V_o = \frac{E_1\, Z_2//Z_3//Z_4}{Z_1 + Z_2//Z_3//Z_4} + \frac{E_2\, Z_1//Z_3//Z_4}{Z_2 + Z_1//Z_3//Z_4}$$

$$+ \frac{E_3\, Z_1//Z_2//Z_4}{Z_3 + Z_1//Z_2//Z_4} + \frac{E_4\, Z_1//Z_2//Z_3}{Z_4 + Z_1//Z_2//Z_3}$$

$$V_o = \frac{E_1}{1 + \dfrac{Z_1}{Z_2//Z_3//Z_4}} + \frac{E_2}{1 + \dfrac{Z_2}{Z_1//Z_3//Z_4}}$$

$$+ \frac{E_3}{1 + \dfrac{Z_3}{Z_1//Z_2//Z_4}} + \frac{E_4}{1 + \dfrac{Z_4}{Z_1//Z_2//Z_3}}$$

$$V_o = \frac{E_1}{1 + Z_1\left(\dfrac{1}{Z_2} + \dfrac{1}{Z_3} + \dfrac{1}{Z_4}\right)} + \frac{E_2}{1 + Z_2\left(\dfrac{1}{Z_1} + \dfrac{1}{Z_3} + \dfrac{1}{Z_4}\right)}$$

$$+ \frac{E_3}{1 + Z_3\left(\dfrac{1}{Z_1} + \dfrac{1}{Z_2} + \dfrac{1}{Z_4}\right)} + \frac{E_4}{1 + Z_4\left(\dfrac{1}{Z_1} + \dfrac{1}{Z_2} + \dfrac{1}{Z_3}\right)}.$$

$$V_o = E_1K_1 + E_2K_2 + E_3K_3 + E_4K_4.$$

Now the pattern is evident. In general:

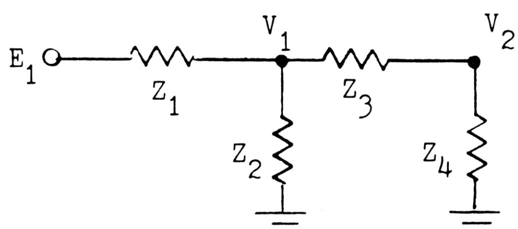
$$V_o = \sum_{i=1}^{N} \frac{E_i}{1 + \text{impedance in series with } E_i \begin{pmatrix}\text{Sum of remaining reciprocal} \\ \text{impedances (admittances)} \\ \text{connected to node Vo}\end{pmatrix}}$$

$$= \sum_{i=1}^{N} E_iK_i.$$

As shown in the next example, the Ei's can be a mix of Ei and Vi.

Now we will use this method to write node equations by inspection.

<u>Example 3</u> Ladder network.



Solve for dependent node voltages V_1 and V_2.

We see that the equation for V_1 will be the superposition sum of E_1 and V_2:

(1) $V_1 = E_1K_1 + V_2K_2$, where $K_1 = \dfrac{1}{1 + Z_1\left(\dfrac{1}{Z_2} + \dfrac{1}{Z_3}\right)}$,

$$K_2 = \frac{1}{1 + Z_3\left(\dfrac{1}{Z_1} + \dfrac{1}{Z_2}\right)}$$

Since there is only one voltage driving node V_2, the equation for V_2 will have only one term:

(2) $V_2 = V_1K_3$, where $$K_3 = \frac{1}{1 + \dfrac{Z_3}{Z_4}}$$

Equations (1) and (2) can be solved for V_1 and V_2 by elimination or by matrix methods. By elimination:

$V_1 = E_1K_1 + (V_1K_3)K_2$, substituting (2) into (1). Then

(3) $$V_1 = \frac{E_1K_1}{1 - K_2K_3}$$

Substituting (3) into (2) gives V_2, or

$$V_2 = V_1K_3 = \frac{E_1K_1K_3}{1 - K_2K_3}$$

Using matrix methods:

Rearranging (1) and (2) so that the independent terms are on the LH side:

$$E_1K_1 = V_1 - V_2K_2$$

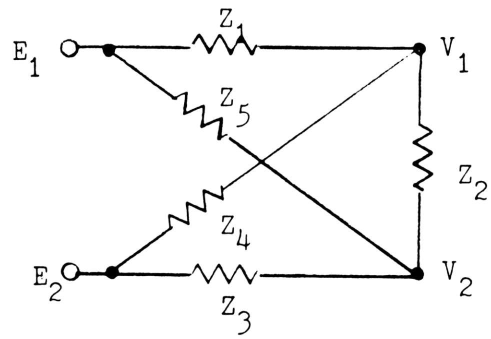
$$0 = V_2 - V_1K_3.$$

From this form it is easy to construct the coefficient matrix and independent column vector:

$$\begin{vmatrix} 1 & -K_2 \\ -K_3 & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \end{vmatrix} = \begin{vmatrix} E_1K_1 \\ 0 \end{vmatrix}$$

From now on, matrices will be used exclusively. As the circuits get larger and more complicated, solving for the unknown node voltages using algebra and the elimination method becomes too lengthy and error prone.

<u>Example 4</u> Lattice network.



Now we can be methodical and consisent.

Step 1. Write dependent node equations using superposition and assigning a unique K factor to each term.

$$V_1 = E_1K_1 + E_2K_2 + V_2K_3$$

$$V_2 = E_1K_4 + E_2K_5 + V_1K_6$$

(We dont care what the K's are until after the matrices are formed.)

Step 2. Put independent terms on LH side:

$$E_1K_1 + E_2K_2 = V_1 - V_2K_3$$

$$E_1K_4 + E_2K_5 = V_2 - V_1K_6$$

Step 3. Put in matrix form:

$$\begin{vmatrix} 1 & -K_3 \\ -K_6 & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \end{vmatrix} = \begin{vmatrix} E_1K_1 + E_2K_2 \\ E_1K_4 + E_2K_5 \end{vmatrix}$$

Step 4. From the circuit diagram and the equations of step 1, write out the K factors.

Before doing this, a functional notation for the K factors will be defined.

$$\text{Let} \quad \frac{1}{1 + \dfrac{A}{B}} = F2(A,B) \ ,$$

$$\frac{1}{1 + A\left(\frac{1}{B} + \frac{1}{C}\right)} = F3(A,B,C),$$

$$\frac{1}{1 + A\left(\frac{1}{B} + \frac{1}{C} + \frac{1}{D}\right)} = F4(A,B,C,D).$$

Note, for example, that $F3(B,C,A) = \frac{1}{1 + B\left(\frac{1}{C} + \frac{1}{A}\right)}$

$= F3(B,A,C)$, i.e., after the first variable, the order is not important since the reciprocals can be summed in any order.

Getting back to Example 4, we can write out the K factors using this functional notation:

$K1 = F3(Z1,Z2,Z4)$, $K2 = F3(Z4,Z1,Z2)$

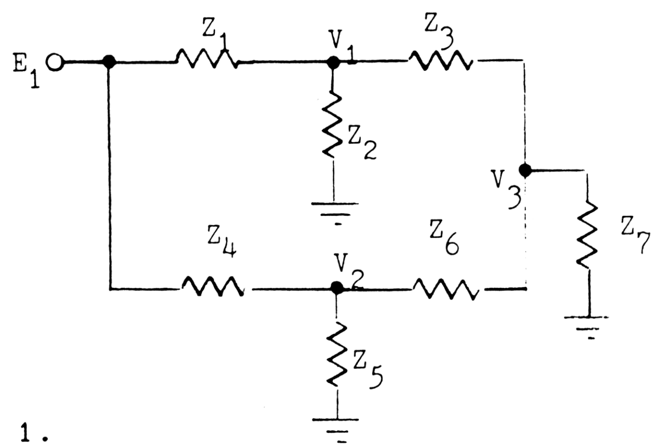
$K3 = F3(Z2,Z1,Z4)$, $K4 = F3(Z5,Z2,Z3)$

$K5 = F3(Z3,Z2,Z5)$, $K6 = F3(Z2,Z3,Z5)$

Remember that the first Z in F3 is in series with the E or V in question. For example, in $V_1 = E_1K_1 + \ldots$, the first Z in K_1 is between V_1 and E_1, or Z_1. Be sure to account for all the remaining Z's connected to node V_1; in this case Z_2 and Z_4.

One last example before going on to transistor and op-amp circuits:

Example 5 Twin-T Network



Step 1.

$$V_1 = E_1K_1 + V_3K_2$$

$$V_2 = E_1K_3 + V_3K_4$$

$$V_3 = V_1K_5 + V_2K_6$$

Step 2.

$$E_1K_1 = V_1 - V_3K_2$$

$$E_1K_3 = V_2 - V_3K_4$$

$$0 = V_3 - V_1K_5 - V_2K_6$$

Step 3.

$$\begin{vmatrix} 1 & 0 & -K_2 \\ 0 & 1 & -K_4 \\ -K_5 & -K_6 & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \\ V_3 \end{vmatrix} = \begin{vmatrix} E_1K_1 \\ E_1K_3 \\ 0 \end{vmatrix}$$

Step 4.

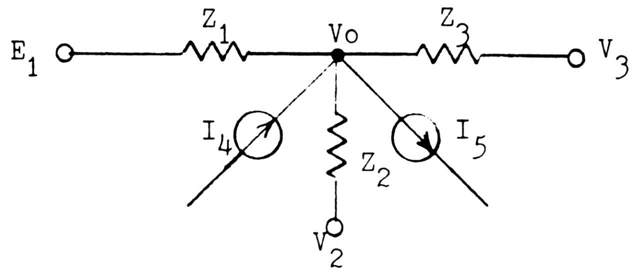
K1 = F3(Z1,Z2,Z3), K2 = F3(Z3,Z1,Z2),

K3 = F3(Z4,Z5,Z6), K4 = F3(Z6,Z4,Z5),

K5 = F3(Z3,Z6,Z7), K6 = F3(Z6,Z3,Z7).

The circuit is now ready for solution by the HP-42S.

At this point, we modify our basic star network by adding current sources:



Again, by superposition:

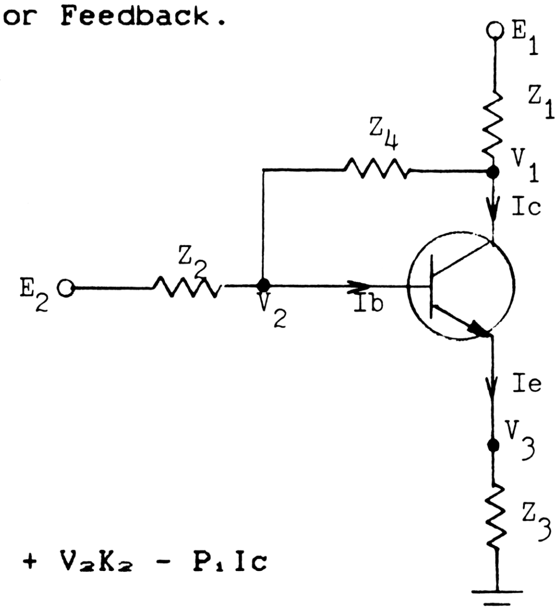
$V_o = E_1K_1 + V_2K_2 + V_3K_3 + P_1I_4 - P_1I_5$,

where K1 = F3(Z1,Z2,Z3), K2 = F3(Z2,Z1,Z3),

K3 = F3(Z3,Z1,Z2), and P1 = Z1//Z2//Z3.

Note direction of current flow and the sign attached; toward node => +, away from node => -.

Example 6   Collector Feedback.



Step 1.

$V_1 = E_1K_1 + V_2K_2 - P_1Ic$

$V_2 = E_2K_3 + V_1K_4 - P_2Ib$

$V_3 = Z_3Ie$

$V_2 - V_3 = Vbe \quad (= 0.6V)$

Step 2. (Express Ic and Ie in terms of Ib.)

$E_1K_1 = V_1 - V_2K_2 + P_1BIb$ (Ic = Beta Ib = BIb)

$E_2K_2 = V_2 - V_1K_4 + P_2Ib$

$0 = V_3 - (1 + B)IbZ_3$ [Ie = (1 + B)Ib]

$Vbe = V_2 - V_3$

Step 3.

$$\begin{vmatrix} 1 & -K_2 & 0 & P_1B \\ -K_4 & 1 & 0 & P_2 \\ 0 & 0 & 1 & -(1+B)Z_3 \\ 0 & 1 & -1 & 0 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \\ V_3 \\ Ib \end{vmatrix} = \begin{vmatrix} E_1K_1 \\ E_2K_2 \\ 0 \\ Vbe \end{vmatrix}$$

Step 4.

K1 = F2(Z1,Z4), K2 = F2(Z4,Z1),

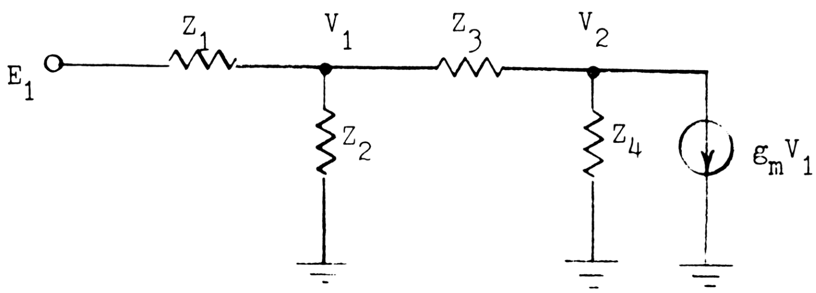
K3 = F2(Z2,Z4), K4 = F2(Z4,Z2)

P1 = Z1//Z4, P2 = Z2//Z4

This circuit is not easily solved by conventional methods. Using the above matrices, the HP-42S will solve for all node voltages and the base current Ib. Collector and emmitter currents are easily obtained from Ic = BIb, and Ie = (1 + B)Ib.

Note that in forming the P's associated with current sources, they are easily remembered as the parallel combination of all impedances connected to the node in question.

Example 7 Common Emitter Hybrid Pi Transistor Model



Note that ($g_M V_1$) is a voltage-controlled-current-source, or VCCS.

Step 1.

$$V_1 = E_1 K_1 + V_2 K_2$$

$$V_2 = V_1 K_3 - g_M V_1 P_1 = V_1 (K_3 - g_M P_1)$$

Step 2.

$$E_1 K_1 = V_1 - V_2 K_2$$

$$0 = V_2 - V_1 (K_3 - g_M P_1)$$

Step 3.

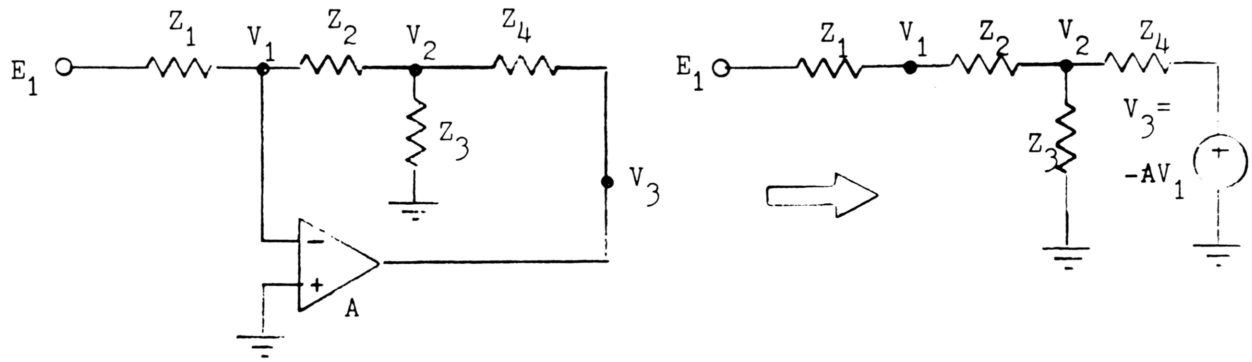
$$\begin{vmatrix} 1 & -K_2 \\ (g_M P_1 - K_3) & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \end{vmatrix} = \begin{vmatrix} E_1 K_1 \\ 0 \end{vmatrix}$$

Step 4.

K1 = F3(Z1,Z2,Z3), K2 = F3(Z3,Z1,Z2)

K3 = F2(Z3,Z4), P1 = Z3//Z4

Example 8 Inverting op-amp



A simplified model of the op-amp is obtained by the dependent voltage source $V_3 = -AV_1$, where A is the open loop gain. (V_3 is a voltage-controlled-voltage-source, or VCVS.)

The variable A can be complex to show the first order rolloff without adding additional reactive components:

$$A = \frac{Aol}{1 + \frac{jw}{w_1}}, \text{ where } Aol = \text{about } 10{,}000 \text{ v/v},$$

and w1 = 2pi(f1) is the frequency breakpoint , and 10 < f1 < 100 in Hz for most op-amps.

Gain A can have zeros as well as poles:

$$\frac{Aol\left(1 + \frac{jw}{w_2}\right)}{\left(1 + \frac{jw}{w_1}\right)\left(1 + \frac{jw}{w_3}\right)}$$

For most op-amp circuits, the single pole rolloff will suffice.

Again, steps 1 thru 4 are no different:

Step 1.

$$V_1 = E_1K_1 + V_2K_2$$

$$V_2 = V_1K_3 + V_3K_4 = V_1K_3 - AV_1K_4$$

$$= V_1(K_3 - AK_4)$$

Step 2.

$$E_1K_1 = V_1 - V_2K_2$$

$$0 = V_2 - V_1(K_3 - AK_4)$$

Step 3.

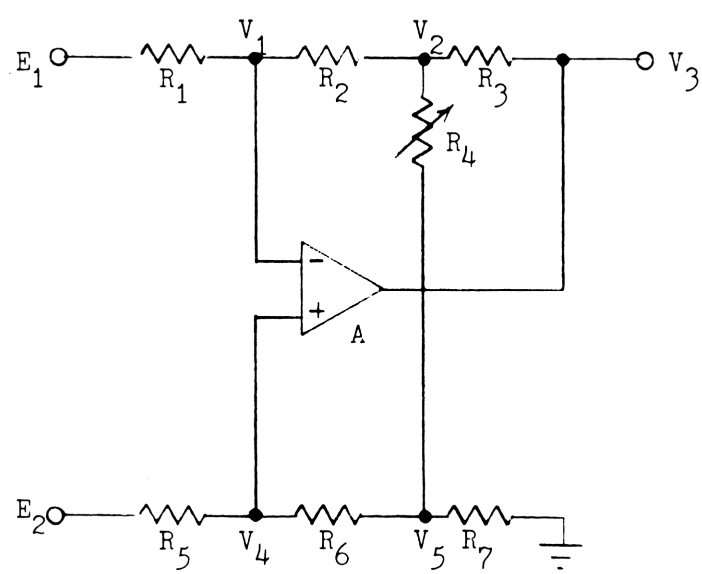
$$\begin{vmatrix} 1 & -K_2 \\ (AK_4-K_3) & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \end{vmatrix} = \begin{vmatrix} E_1K_1 \\ 0 \end{vmatrix}$$

Step 4

K1 = F2(Z1,Z2), K2 = F2(Z2,Z1)

K3 = F3(Z2,Z3,Z4), K4 = F3(Z4,Z2,Z3)

<u>Example 9</u> Adjustable gain differential amplifier.



Step 1.

$$V_1 = E_1K_1 + V_2K_2$$

$$V_2 = V_1K_3 + V_3K_4 + V_5K_5$$

$$V_3 = A(V_4 - V_1)$$

$$V_4 = E_2K_6 + V_5K_7$$

$$V_5 = V_4K_8 + V_2K_9$$

Step 2.

$$E_1K_1 = V_1 - V_2K_2$$

$$0 = V_2 - V_1K_3 - V_3K_4 - V_5K_5$$

$$0 = V_3 - AV_4 + AV_1$$

$$E_2K_6 = V_4 - V_5K_7$$

$$0 = V_5 - V_2K_9 - V_4K_8$$

Step 3.

$$\begin{vmatrix} 1 & -K_2 & 0 & 0 & 0 \\ -K_3 & 1 & -K_4 & 0 & -K_5 \\ A & 0 & 1 & -A & 0 \\ 0 & 0 & 0 & 1 & -K_7 \\ 0 & -K_9 & 0 & -K_8 & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{vmatrix} = \begin{vmatrix} E_1K_1 \\ 0 \\ 0 \\ E_2K_6 \\ 0 \end{vmatrix}$$

Step 4.

K1 = F2(R1,R2), K2 = F2(R2,R1)

K3 = F3(R2,R3,R4), K4 = F3(R3,R2,R4),

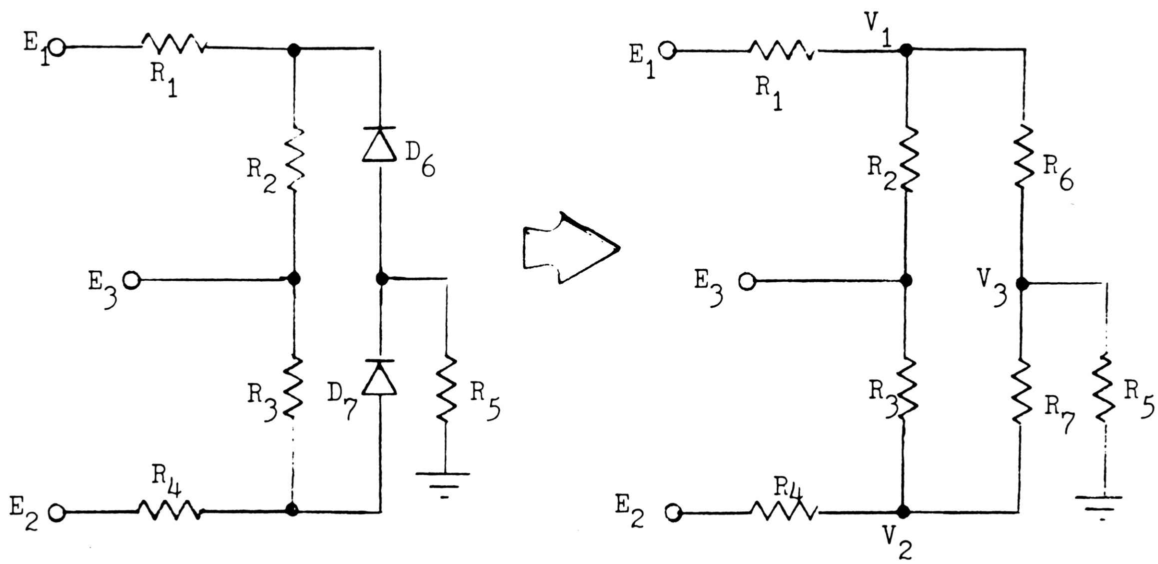
K5 = F3(R4,R2,R3),

K6 = F2(R5,R6), K7 = F2(R6,R5),

K8 = F3(R6,R4,R7), K9 = F3(R4,R6,R7)

Example 10 Non-linear Circuits.

Some non-linear diode circuits can be solved by converting the diodes to resistors (in series with a 0.6V source if need be). The method is to monitor the voltages across the resistor (diode) for polarity. If the "diode" becomes reverse biased, then change its value to 10 Megohms. If it becomes forward biased, change its value to, say, 10 ohms.



Step 1 (For the circuit on the right)

$$V_1 = E_1K_1 + E_3K_2 + V_3K_3$$

$$V_2 = E_2K_4 + E_3K_5 + V_3K_6$$

$$V_3 = V_1K_7 + V_2K_8$$

Step 2.

$$E_1K_1 + E_3K_2 = V_1 - V_3K_3$$

$$E_2K_4 + E_3K_5 = V_2 - V_3K_6$$

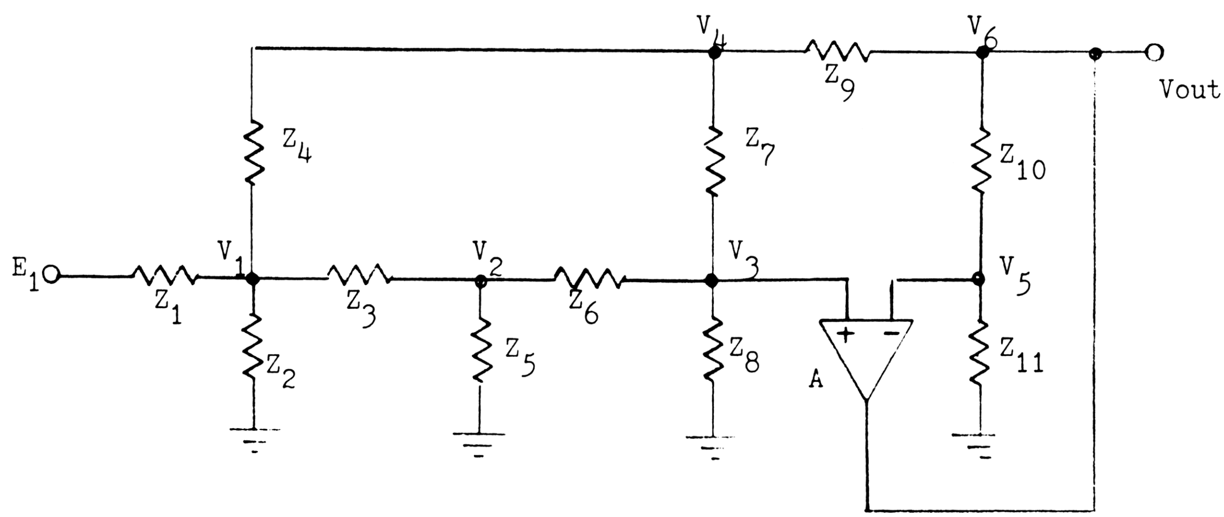
$$0 = V_3 - V_2K_8 - V_1K_7$$

Steps 3 and 4 are, as they say, "left as an excercise for the student".

During the analysis in section II, if $(V_1 - V_3) < 0$, set R_6 = 10 ohms; if > 0 set R_6 = 10 Megohms. Similarly, if $(V_2 - V_3) > 0$, set R_7 = 10 ohms; if < 0 set R_7 = 10 Megohms.

Examples 11 and 12 following illustrate the ease of writing node equations using the K method for relatively large and complicated circuits.

Example 11   Fifth Order Active Filter



Step 1.

$$V_1 = E_1K_1 + V_2K_2 + V_4K_3$$

$$V_2 = V_1K_4 + V_3K_5$$

$$V_3 = V_2K_6 + V_4K_7$$

$$V_4 = V_1K_8 + V_3K_9 + V_6K_{10}$$

$$V_5 = V_6K_{11}$$

$$V_6 = A(V_3 - V_5)$$

Step 2.

$$E_1K_1 = V_1 - V_2K_2 - V_4K_3$$

$$0 = V_2 - V_1K_4 - V_3K_5$$

$$0 = V_3 - V_2K_6 - V_4K_7$$

$$0 = V_4 - V_1K_8 - V_3K_9 - V_6K_{10}$$

$$0 = V_5 - V_6K_{11}$$

$$0 = V_6 - AV_3 + AV_5$$

Step 3.

$$\begin{vmatrix} 1 & -K_2 & 0 & -K_3 & 0 & 0 \\ -K_4 & 1 & -K_5 & 0 & 0 & 0 \\ 0 & -K_6 & 1 & -K_7 & 0 & 0 \\ -K_8 & 0 & -K_9 & 1 & 0 & -K_{10} \\ 0 & 0 & 0 & 0 & 1 & -K_{11} \\ 0 & 0 & -A & 0 & A & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{vmatrix} = \begin{vmatrix} E_1K_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{vmatrix}$$

Step 4.

K1 = F4(Z1,Z2,Z3,Z4), K2 = F4(Z3,Z1,Z2,Z4)

K3 = F4(Z4,Z1,Z2,Z3)

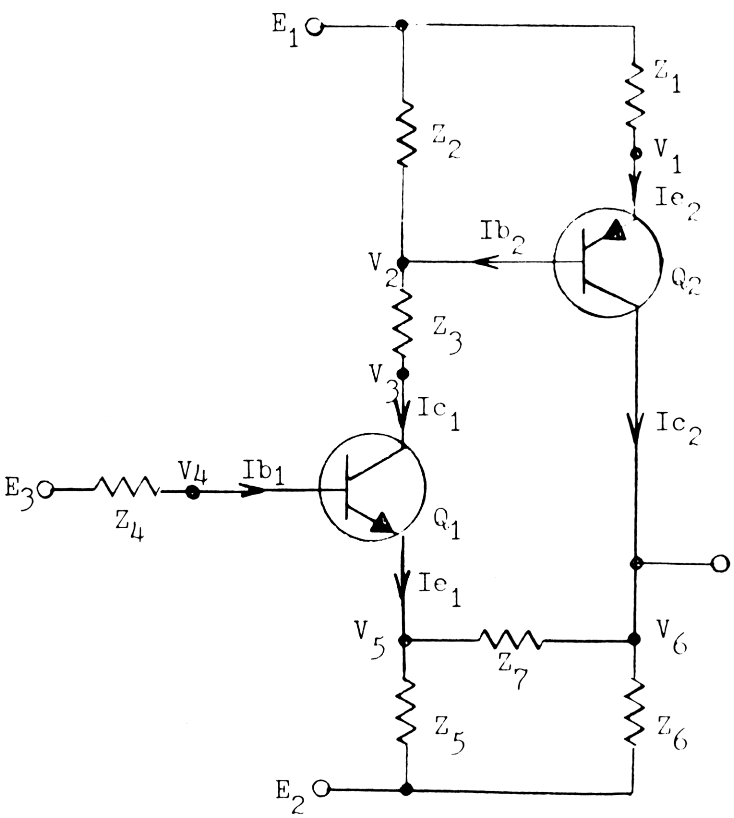
K4 = F3(Z3,Z5,Z6), K5 = F3(Z6,Z3,Z5)

K6 = F3(Z6,Z7,Z8), K7 = F3(Z7,Z6,Z8)

K8 = F3(Z4,Z7,Z9), K9 = F3(Z7,Z4,Z9)

K10 = F3(Z9,Z4,Z7), K11 = F2(Z10,Z11)

<u>Example 12</u> Complementary Feedback Amplifier.



Step 1.

$$V_1 = E_1 - Ie_2Z_1$$

$$V_2 = E_1K_1 + V_3K_2 + Ib_2P_1$$

$$V_3 = V_2 - Ic_1Z_3$$

$$V_4 = E_3 - Ib_1Z_4$$

$$V_5 = E_2K_3 + V_6K_4 + Ie_1P_2$$

$$V_6 = E_2K_5 + V_5K_6 + Ic_2P_3$$

$$Vbe_1 = V_4 - V_5$$

$$Vbe_2 = V_1 - V_2$$

Step 2.

$$E_1 = V_1 + (1 + B_2)Ib_2Z_1$$

$$E_1K_1 = V_2 - V_3K_2 - Ib_2P_1$$

$$0 = V_3 - V_2 + B_1Ib_1Z_3$$

$$E_3 = V_4 + Ib_1Z_4$$

$$E_2K_3 = V_5 - V_6K_4 - (1 + B_1)Ib_1P_2$$

$$E_2K_5 = V_6 - V_5K_6 - B_2Ib_2P_3$$

$$Vbe_1 = V_4 - V_5$$

$$Vbe_2 = V_1 - V_2$$

Step 3.

$$\begin{vmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & (1+B_2)Z_1 \\ 0 & 1 & -K_2 & 0 & 0 & 0 & 0 & -P_1 \\ 0 & -1 & 1 & 0 & 0 & 0 & B_1Z_3 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & Z_4 & 0 \\ 0 & 0 & 0 & 0 & 1 & -K_4 & -(1+B_1)P_2 & 0 \\ 0 & 0 & 0 & 0 & -K_6 & 1 & 0 & -B_2P_3 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ Ib_1 \\ Ib_2 \end{vmatrix}$$

$$= \begin{vmatrix} E_1 & E_1K_1 & 0 & E_3 & E_3K_3 & E_3K_5 & Vbe_1 & Vbe_2 \end{vmatrix}^T$$

(The ^{T} transposes the row vector into a column vector.)

Step 4.

K1 = F2(Z2,Z3), K2 = F2(Z3,Z2)

K3 = F2(Z5,Z7), K4 = F2(Z7,Z5)

K5 = F2(Z6,Z7), K6 = F2(Z7,Z6)

P1 = Z2//Z3, P2 = Z5//Z7, P3 = Z6//Z7

In setting up the coefficient matrix, advantage should be taken of all the zeros in the matrix (a so-called sparse matrix) and that the main diagaonal is nearly all 1's. That is, one should form an identity matrix first, and then store only the non-zero elements.

By now the astute reader has probably seen the similarity of the F3 and F4 K factor functions with the parallel impedance function. There are two alternate formulations of these functions that may result in shorter HP-42S programs.

For example, if

K1 = F4(Z1,Z2,Z3,Z4), K2 = F4(Z2,Z1,Z3,Z4,

K3 = F4(Z3,Z1,Z2,Z4), K4 = F4(Z4,Z1,Z2,Z3),

a shorter way of computing K1 through K4 is

K1 = F4(Z1,Z2,Z3,Z4), K2 = (K1*Z1)/Z2,

K3 = (K1*Z1)/Z3, K4 = (K1*Z1)/Z4.

Note that the denominator of Ki is Zi, i = 2, 3, 4.

Still another way of calculating K1 through K4 is

P1 = Z1//Z2//Z3//Z4, then

K1 = P1/Z1, K2 = P1/Z2, K3 = P1/Z3, and K4 = P1/Z4.

The form here is Ki = P1/Zi

Also note that K1 + K2 + K3 + K4 = 1. Then K4 can also be calculated by K4 = 1 - K1 - K2 - K3. Similary, for N =3

K1 = F3(Z1,Z2,Z3); K2 = F3(Z2,Z1,Z3); K3 = F3(Z3,Z1,Z2);

but it is quicker to compute K3 = 1 - K1 - K2.

SECTION II. HP-42S Programs

Due to word processor character limitations, the following substitutions will be used for the given HP-42S characters: (Substituting j for i is due to electrical engineering preference, and should not cause undue confusion.)

HP-42S Character	Text Character
→	ra (right arrow)
↓	da (down arrow)
R↑	Rup
R↓	Rdn
10↑X	10^X
÷	/
i	j

We will begin from the bottom and work up. That is, the following subprograms with global labels will be used with main programs "SETUP", "DCAP", and "ACAP", to be described later. They should be keyed in now.

Circuit element:	Capacitor	Inductor	Resistor in series with capacitor	Resistor in series with inductor
Complex expression:	0 - j/wC	0 + jwL	R - j/wC	R + jwL
Stack must contain:				
Y-reg:	any	any	R	R
X-reg:	C	L	C	L
Listing:	01 LBL "XC" 02 RCLx"w" 03 1/X 04 +/- 05 0 06 X<>Y 07 COMPLEX 09 END	01 LBL "XL" 02 RCLx"w" 03 0 04 X<>Y 05 COMPLEX 06 END	01 LBL "SRC" 02 RCLx"w" 03 1/X 04 +/- 05 COMPLEX 06 END	01 LBL SRL 02 RCLx"w" 03 COMPLEX 04 END

Circuit element:	Resistor in parallel with capacitor	Resistor in parallel with inductor	Operational amplifier
Complex expression:	1/(1/R + jwC)	1/(1/R - j/wL)	Aol/(1 + jw/w_1) = Aol/(1 + jf/f_1)
Stack must contain:			
Y-reg:	R	R	any
X-reg:	C	L	any
Listing:	01 LBL "PRC" 02 RCLx"w" 03 X<>Y 04 1/X 05 X<>Y 06 COMPLEX 07 1/X 08 END	01 LBL "PRL" 02 RCLx"w" 03 1/X 04 +/- 05 X<>Y 06 1/X 07 X<>Y 08 COMPLEX 09 1/X 10 END	01 LBL "OPAMP" 02 1 03 ENTER 04 RCL "F" 05 10^X 06 10 (f_1) 07 / 08 COMPLEX 09 1E4 (Aol) 10 X<>Y 11 / 12 STO "A" 13 END

Function:	F2(Z1,Z2)	Z1//Z2
Complex expression:	$\dfrac{1}{1 + Z1/Z2}$	$\dfrac{1}{1/Z1 + 1/Z2}$
Stack must contain:		
Y-reg:	Z_1	Z_1 or Z_2
X-reg:	Z_2	Z_2 or Z_1
Listing:	01 LBL "F2" 02 1/X 03 x 04 1 05 + 06 1/X 07 END	01 LBL "PZ2" 02 1/X 03 X<>Y 04 1/X 05 + 06 1/X 07 END

Function:	$Z_1//Z_2//Z_3$	$Z_1//Z_2//Z_3//Z_4$
Complex expression:	$\dfrac{1}{1/Z_1 + 1/Z_2 + 1/Z_3}$	$\dfrac{1}{1/Z_1 + 1/Z_2 + 1/Z_3 + 1/Z_4}$
Stack must contain:		
T-reg:	any	Z_1
Z-reg:	Z_1	Z_2
Y-reg:	Z_2	Z_3
X-reg:	Z_3	Z_4
Listing:	01 LBL "PZ3" 02 XEQ "PZ2" 03 XEQ "PZ2" 04 END	01 LBL "PZ4" 02 XEQ "PZ3" 03 XEQ "PZ2" 04 END

For "PZ3" and "PZ4", the Z's can be in any order in the stack.

The following program is an initializing routine that must be run before analyzing any new circuit. It need not be executed more than once for the same circuit.

After a menu choice of AC or DC analysis, the required input is the order n of the n x n coefficient matrix.

Listing	Comments
LBL "SETUP"	
WRAP	
CF 01	Clear AC/DC selection flag
CLV "MATK"	Clear old circuit matrices
CLV "MATE"	
CLV "MATV"	
"AC"	Begin menu setup
KEY 1 GTO 01	
"DC"	
KEY 4 GTO 02	
MENU	
STOP	
LBL 02	
SF 01	Set flag 01 for DC analysis
LBL 01	
EXITALL	
"Order?"	
PROMPT	
ENTER	
DIM "MATK"	Dimension K (coefficient) matrix
1	
DIM "MATE"	Dimension E (independent) column vector
DIM "MATV"	Dimension V (node voltage) column vector
RECT	
0	
ENTER	
COMPLEX	
FS? 01	DC analysis?
GTO 01	Then do not create complex matrices
STOx "MATK"	Create complex matrices for AC analysis
STOx "MATE"	
STOx "MATV"	
LBL 01	Begin creating MATK = I (Identity matrix)
INDEX "MATK"	
Rup	Place n in X-reg.
ENTER	
ENTER	Start in lower rh corner (element n,n)
LBL 00	
STOIJ	
1	
STOEL	Store 1 in element i, j = i
Rdn	
DSE ST Y	Decrement i and j pointers
DEG	
DSE ST X	
GTO 00	If i,j not 0 then repeat
FC? 01	
GTO "ACAP"	Go to AC Analysis Program
GTO "DCAP"	Go to DC Analysis Program
END	

As an introduction, a DC analysis example will be given first. The ladder network on page 4 will be analyzed with resistors for the impedances Z_1 thru Z_4.

Generally speaking, a circuit under analysis has component designations such as R_1, C_2, L_3, R_4, etc. Thus we can store R_1 in numbered register 01, C_2 in reg. 02, etc. This keeps alot of clutter out of the variable catalog and provides easy association of registers vs. components.

Circuits analyzed here will have less than 15 components, so the numbered registers can be SIZEd to 15. This will leave room for some scratch storage if needed.

<u>Example 1</u> (DC) Ladder Network

First, the main program "DCAP" will be listed so that the program flow can be demonstrated.

Listing	Comments
01 LBL "DCAP"	
02 XEQ "SKF"	Store K Factors subprogram. Creates and stores all the required K factors. For the DC ladder network, this will be K_1, K_2, and K_3 (see page 4).
03 XEQ "MAT"	Form the n x n K-matrix, the n x 1 E-vector, and solve for the n x 1 V-vector containing the node voltages.
04 LBL 01	
05 INPUT "Vn"	Choose which node voltage to display
06 XEQ "GETV"	This subprogram recalls and displays the node voltage selected in line 05.
07 STOP	Display node voltage
08 GTO 01	Select another node if desired
09 END	

Before going any further, the following resistor values for the ladder network should be stored in the corresponding numbered registers:

```
1000 STO 01  (R1)
2000 STO 02  (R2)
3000 STO 03  (R3)
4000 STO 04  (R4)
```

Also store 10 in "E1", so that the input voltage is 10 V.

The first subprogram encountered is "SKF", which is given below:

Listing	Comments
01 LBL "SKF"	
02 RCL 01	
03 RCL 02	
04 RCL 03	Create K_1
05 XEQ "PZ3"	Get $P = R_1//R_2//R_3$
06 ENTER	
07 RCL/ 01	$K_1 = P/R_1$
08 STO "K1"	
09 Rdn	
10 RCL/ 03	$K_2 = P/R_3$
11 STO "K2"	
12 RCL 03	
13 RCL 04	
14 XEQ "F2"	Get K_3
15 STO "K3"	
16 END	

Now the HP-42S has created all three K factors and we are ready to fill the 2 x 2 K-matrix, and the 2 x 1 E-vector shown on page 5, with the subprogram "MAT":

Listing	Comments
01 LBL "MAT"	
02 INDEX "MATK"	Pointers at $i = j = 1$.
03 J+	Skip to element 1:2, since "SETUP" already has put 1's on the main diagonal.
04 RCL "K2"	
05 +/-	
06 ra	Put $-K_2$ at 1:2
07 RCL "K3"	
08 +/-	
09 ra	Put $-K_3$ at 2:1
10 INDEX "MATE"	
11 RCL "E1"	Input voltage = 10 V
12 RCLx "K1"	
13 da	Put E_1K_1 at 1:1
14 RCL "MATE"	
15 RCL/ "MATK"	Get node voltage vector
16 STO "MATV"	
17 END	

Note that lines 01, 02, 10, and 14 thru 17 must be included for every circuit to be analyzed. Thus the general format for every "MAT" subprogram is:

```
01 LBL "MAT"
02 INDEX "MATK"
     .
     .
  (fill K matrix)
     .
     .
   INDEX "MATE"
     .
     .
  (fill E vector)
     .
     .
   RCL "MATE"
   RCL/ "MATK"
   STO "MATV"
   END
```

The last subprogram run by the main program "DCAP" is "GETV", which is given below:

```
  Listing                        Comments

01 LBL "GETV"
02 INDEX "MATV"
03 RCL "Vn"           Vn = the selected node voltage, which is the
                      numbered column element of the node voltage
                      vector "MATV"
04 1
05 STOIJ              Store Vn:1 pointer
06 RCLEL              Get Vn
07 END
```

Now the DCAP program is ready to run; but we must first execute "SETUP" before analyzing any circuit:

XEQ "SETUP".

Choose DC (the LOG key) when the menu appears. In response to Order?, key in the order of the K matrix, which is 2 for this example:

2, R/S. The display should then be:

Y: [2x1 Matrix]
Vn? (any)

For Vn?, key in 2 to get the voltage at node 2:

2, R/S. V_2 should = 3.478 (volts) as displayed in the X-reg.

Repeat for node 1: R/S, 1, R/S. V_1 should = 6.087 (volts).

As a check, K_1 = 0.545; K_2 = 0.182; K_3 = 0.571.

<u>Example 1</u> (AC) Ladder Network

AC analysis is performed by the main program "ACAP", which is listed below:

Listing	Comments
01 LBL "ACAP"	
02 "Log F1"	Log_{10} beginning frequency in Hz
03 PROMPT	
04 STO "F"	
05 INPUT "PD"	PD = points per decade of frequency
06 INPUT "ND"	ND = number of decades
07 RCL+ "F"	Add beginning frequency to get
08 STO "FL"	ending or last frequency point
09 INPUT "Vn"	Node to be analyzed
10 RCL "F"	To convert F1 to radians/sec ("w")
11 LBL 00	
12 10^X	Get F from Log F
13 2	
14 PI	
15 x	
16 x	
17 STO "w"	Store radians/sec
18 XEQ "SKF"	Store K Factors subprogram (same as "DCAP")
19 XEQ "MAT"	Create & solve matrices (same as "DCAP")
20 XEQ "GETV"	Get node voltage selected by "Vn" input
21 -> POL	Convert to polar form
22 COMPLEX	complex -> real
23 X<>Y	Put magnitude in X-reg
24 LOG	Convert to dBV. Lines 24 thru 26 can be deleted
25 20	if volts are desired.
26 x	
27 FIX 02	Begin display setup
28 CLA	
29 ARCL "F"	
30 ⊢ " "	Append space
31 FIX 03	Display format for dBV
32 ARCL ST X	
33 Rdn	
34 FIX 00	For phase angle is deg
35 RND	
36 ⊢ " "	
37 ARCL ST X	
38 AVIEW	Set flag 21 to stop
39 RCL "PD"	
40 1/X	
41 STO+ "F"	Increment frequency
42 RCL "FL"	
43 RCL "F"	
44 X≤Y?	
45 GTO 00	Repeat if not done
46 FIX 03	
47 END	

As an introduction to an AC analysis, the ladder network analyzed in the DC analysis will have the components changed as follows:

Element	Reference Designator	New AC value	Stored in Register
Z1	R1	10 K ohms	01
Z2	C2	0.01 uF	02
Z3	R3	10 K ohms	03
Z4	C4	0.01 uF	04
E1	E1	1	"E1"

These values should now be stored in the registers shown above.

Since the matrix on page 5 has the same form whether real or complex (DC or AC), subprogram "MAT" does not have to be modified from the DC analysis. Only "SKF" must be modified as shown below:

Listing	Comments
01 LBL "SKF"	
02 RCL 02	
03 XEQ "XC"	Get $Z_2 = 0 - j/wC_2$
04 STO "Z2"	
05 RCL 04	Do the same for C_4
06 XEQ "XC"	
07 STO "Z4"	
08 RCL 01	$Z_1 = R_1$
09 RCL "Z2"	
10 RCL 03	$Z_3 = R_3$
11 XEQ "PZ3"	Get $P = R_1//Z_2//R_3$
12 ENTER	
13 RCL/ 01	$K_1 = P/R_1$
14 STO "K1"	
15 Rdn	
16 RCL/ 03	$K_2 = P/R_3$
17 STO "K2"	
18 RCL 03	
19 RCL "Z4"	
20 XEQ "F2"	
21 STO "K3"	The K factors are now all complex
22 END	

After keying in "SKF" above, we are ready to start the AC analysis of the ladder network, which has now become a 2-pole low-pass passive filter. Again, always execute "SETUP" prior to analyzing any new circuit:

XEQ "SETUP"; choose AC from the menu, and the order is still 2.

We will select a frequency sweep of from 100 Hz to 100 KHz at 10 points per the 3 decades: In response to the "Log F1" prompt, key in 2 (log 100 = 2).

In response to PD?, key in 10 (points per decade); and in response to ND?, enter 3 (decades); for Vn?, we still want to look at node 2, so key in 2, R/S.

A sample of the outputs you should have obtained is shown below:

Log F	dBV	Deg	
2.00	-0.118	-11	
2.10	-0.186	-13	
2.20	-0.292	-17	
	.		
	.		
	.		
2.80	-3.273	-55	(Approximate 3 dB breakpoint)
	.		
	.		
	.		
4.00	-32.638	-154	(Approximate 3 dB breakpoint)
	.		
	.		
	.		
4.90	-67.939	-177	
5.00	-71.935	-177	(End of frequency sweep)

The slope of the Bode magnitude at log F = 5 is the dB value at log F = 4.9 minus the dB value at log F = 5 divided by the frequency increment of 1/ND or

$$\text{slope} = (-71.935 - (-67.939))10 = -39.96 \text{ dB/decade}$$

or approximately -40 dB/decade. This is what would be expected for a two pole low-pass filter well beyond the second pole frequency.

Example 4, the lattice network is omitted.

Example 5. Twin-T Network

Step 1. Store the following values in the registers indicated:

Element	Reference Designator	New AC value	Stored in Register
Z1	C1	0.01 uF	01
Z2	R2	133 K	02
Z3	C3	0.01 uF	03
Z4	R4	267 K	04
Z5	C5	0.02 uF	05
Z6	R6	267 K	06
Z7	R7	10 Meg	07
E1	E1	1	"E1"

Step 2. Clear the previous "SKF" and "MAT" programs, and key in the following new ones given without comments: (see page 8)

```
01 LBL "SKF"
02 RCL 01
03 XEQ "XC"
04 STO "Z1"
05 RCL 03
06 XEQ "XC"
07 STO "Z3"
08 RCL 05
09 XEQ "XC"
10 STO "Z5"
11 RCL "Z1"
12 RCL 02
13 RCL "Z3"
14 XEQ "PZ3"
15 ENTER

16 RCL/ "Z1"
17 STO "K1"
18 Rdn
19 RCL/ "Z3"
20 STO "K2"
21 RCL 04
22 RCL "Z5"
23 RCL 06
24 XEQ "PZ3"
25 ENTER

26 RCL/ 04
27 STO "K3"
28 Rdn
29 RCL/ 06
```

```
01 LBL "MAT"
02 INDEX "MATK"
03 J+
04 J+
05 RCL "K2"
06 +/-
07 ra
08 J+
09 J+
10 RCL "K4"
11 +/-
12 ra
13 RCL "K5"
14 +/-
15 ra
16 RCL "K6"
17 +/-
18 ra
19 INDEX "MATE"
20 RCL "E1"
21 RCLx "K1"
22 da
23 RCL "K3"
24 da
25 RCL "MATE"
26 RCL/ MATK"
27 STO "MATV"
28 END
```

```
30 STO "K4"
31 RCL "Z3"
32 RCL 06
33 RCL 07
34 XEQ "PZ3"
35 ENTER
36 RCL/ "Z3"
37 STO "K5"
38 Rdn
39 RCL/ 06
40 STO "K6"
41 END
```

The given component values are for a 60 Hz notch filter. Hence we want to look at one decade between 10 and 100 Hz. Twenty points should be enough, therefore execute the following:

XEQ "SETUP"; choose AC; Order? 3, R/S, Log F1?, 1, (log 10 = 1), R/S, PD?, 20, R/S, ND?, 1, Vn?, 3, R/S. Output samples are:

```
Log F   dBV     Deg

1.00 -2.046 -34
      .
      .
      .
1.80 -31.184 90  (the notch)
      .
      .
2.00 -11.777 76
```

To see what the output is at exactly 60 Hz: XEQ "ACAP", Log F1?, 60, LOG, (see 1.778), R/S, PD?, 1, R/S, ND?, 0, Vn?, 3, will give just one output at log 60 Hz = 1.778:

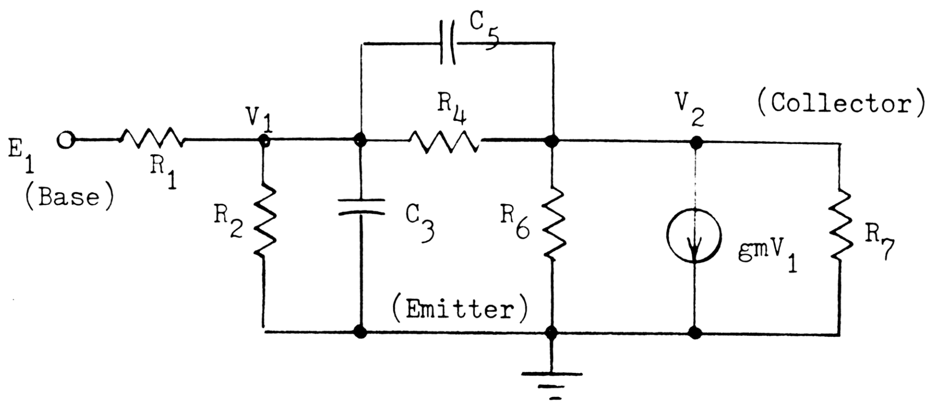
```
1.78 -51.048 100
```

which verifies the notch filter design.

For the remaining circuits, just component values, listings for "SKF" and "MAT", output sample points to verify the analysis, and a schematic if necessary will be provided. Be sure to execute "SETUP" prior to analyzing each new circuit. The "Order?" can be obtained by inspection of the corresponding K-matrix in section I.

Example 7. Common Emitter Hybrid Pi Transistor Model

The circuit used for the analysis is shown below:



Note that Z1 ---> R1; Z2 ---> R2//C3; Z3 ---> R4//C5; and Z4 ---> R6//R7. (See page 11.)

Component storage:

Element	Reference Designator	Value	Stored in Register
Gm	GM	0.025	00
Z1	R1	100	01
Z2	R2	1 K	02
Z2	C3	100 pF	03
Z3	R4	4 Meg	04
Z3	C5	3 pF	05
Z4	R6	80 K	06
Z4	R7	10 K	07
E1	E1	1	Not stored

Listing for "SKF" and "MAT":

```
01 LBL "SKF"
02 RCL 02
03 RCL 03
04 XEQ "PRC"
05 STO "Z2"
06 RCL 04
07 RCL 05
08 XEQ "PRC"
09 STO "Z3"
10 RCL 06
```

```
01 LBL "MAT"
02 INDEX "MATK"
03 J+
04 RCL "K2"
05 +/-
06 ra
07 RCL "P1"
08 RCLx 00
09 RCL- "K3"
10 ra
```

```
11 RCL 07
12 XEQ "PZ2"
13 STO "Z4"
14 RCL 01
15 RCL "Z2"
16 RCL "Z3"
17 XEQ "PZ3"
18 ENTER
19 RCL/ 01
20 STO "K1"
21 Rdn
22 RCL/ "Z3"
23 STO "K2"
24 RCL "Z3"
25 RCL "Z4"
26 XEQ "PZ2"
27 STO "P1"
28 RCL/ "Z3"
29 STO "K3"
30 END
```

```
11 INDEX "MATE"
12 RCL "K1"
13 da
14 RCL "MATE"
15 RCL/ "MATK"
16 STO "MATV"
17 END
```

Output samples for node 2:

Log F	dBV	Deg	
3.00	46.045	180	
6.20	43.336	136	(3 dB rolloff point)
8.15	-0.222	18	(Gain-bandwidth-product ≅ 1, or f_T = 10^8.15 = 141.3 MHz.)

<u>Example 8.</u> Inverting op-amp

Element	Reference Designator	Value	Stored in Register
Z1	R1	10 K	R01
Z2	R2	15 K	R02
Z3	R3	1 K	R03
Z3	C4	0.015 uF	R04
Z4	R5	15 K	R05
E1	E1	1	Not stored

To illustrate the affects of op-amp rolloff, change line 06 in program "OPAMP" to: 06 10E6.

Since we desire the output V_2, the matrix given on page 13 is recreated without the substitution $V_2 = -AV_1$:

$$\begin{vmatrix} 1 & -K_2 & 0 \\ -K_3 & 1 & -K_4 \\ A & 0 & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \\ V_3 \end{vmatrix} = \begin{vmatrix} E_1 K_1 \\ 0 \\ 0 \end{vmatrix}$$

(An alternative method is to solve the original matrix for V_1 and modify "GETV" to multiply V_1 by -A.)

Listing for "SKF" and "MAT":

```
01 LBL "SKF"
02 RCL 03
03 RCL 04
04 XEQ "SRC"
05 STO "Z3"
06 1
07 RCL 01
08 RCL 02
09 XEQ "F2"
10 STO "K1"
11 -
12 STO "K2"
13 RCL 02
14 RCL "Z3"
15 RCL 05
16 XEQ "PZ3"
17 ENTER
18 RCL/ 02
19 STO "K3"
20 Rdn
21 RCL/ 05
22 STO "K4"
23 XEQ "OPAMP"
24 END
```

```
01 LBL "MAT"
02 INDEX "MATK"
03 J+
04 RCL "K2"
05 +/-
06 ra
07 J+
08 RCL "K3"
09 +/-
10 ra
11 J+
12 RCL "K4"
13 +/-
14 ra
15 RCL "A"
16 ra
17 INDEX "MATE"
18 RCL "K1"
19 da
20 RCL "MATE"
21 RCL/ "MATK"
22 STO "MATV"
23 END
```

As can be seen from the above 3 x 3 K-matrix, the order is 3 when executing "SETUP".

Some output points for node 3 are:

Log F	dBV	Deg	
1.00	9.539	-180	(DC gain of 30K/10K in dBV. -180 since this is an inverting opamp circuit.
6.00	28.094	-179	(Gain increase due to feedback T network.)

Now change line 06 of "OPAMP" to: 06 100

This gives an opamp pole of 100 Hz, which is more realistic. The output at node 3 is now:

Log F	dBV	Deg	
1.00	9.539	-180	(No change.)
6.00	-4.231	91	(The opamp is not capable of high gain at F = 10^6 = 1 MHz.)

<u>Example 9</u> Adjustable Gain Differential Amplifier
(Reference 2.)

Element	Reference Designator	Value	Stored in Register
Z1	R1	20 K	R01
Z2	R2	2 K	R02
Z3	R3	2 K	R03
Z4	R4	1 K	R04
Z5	R5	20 K	R05
Z6	R6	2 K	R06
Z7	R7	2 K	R07
E1	E1	10	"E1"
E2	E2	-10	"E2"

Listing for "SKF" and "MAT":

```
01 LBL "SKF"
02 1
03 RCL 01
04 RCL 02
05 XEQ "F2"
06 STO "K1"
07 -
08 STO "K2"
09 RCL 02
10 RCL 03
11 RCL 04
12 XEQ "PZ3"
13 ENTER
14 RCL/ 02
15 STO "K3"
16 Rdn
17 RCL/ 03
18 STO "K4"
19 Rup
20 1          Using
21 X<>Y       K3+K4+K5=1
22 -
23 X<>Y
24 -
25 STO "K5"
```

```
01 LBL "MAT"
02 INDEX "MATK"
03 J+
04 RCL "K2"
05 +/-
06 ra
07 J+
08 J+
09 J+
10 RCL "K3"
11 +/-
12 ra
13 J+
14 RCL "K4"
15 +/-
16 ra
17 J+
18 RCL "K5"
19 +/-
20 ra
21 RCL "A"
22 ra
23 J+
24 J+
25 RCL "A"
```

```
26 1
27 RCL 05
28 RCL 06
29 XEQ "F2"
30 STO "K6"
31 -
32 STO "K7"
33 RCL 06
34 RCL 04
35 RCL 07
36 XEQ "PZ3"
37 ENTER
38 RCL/ 06
39 STO "K8"
40 Rdn
41 RCL/ 04
42 STO "K9"
43 XEQ "OPAMP"
44 END
```

```
26 +/-
27 ra
28 J+
29 J+
30 J+
31 J+
32 J+
33 RCL "K7"
34 +/-
35 ra
36 J+
37 RCL "K9"
38 +/-
39 ra
40 J+
41 RCL "K8"
42 +/-
43 ra
44 INDEX "MATE"
45 RCL "E1"
46 RCLx "K1"
47 da
48 I+
49 I+
50 RCL "E2"
51 RCLx "K6"
52 da
53 RCL "MATE"
54 RCL/ MATK"
55 STO "MATV"
56 END
```

Though all components are real (resistive), the opamp has an AC rolloff component, so when executing "SETUP", choose AC. From page 14, the order is 5.

We will examine the affects of gain setting resistor R4 at 10 Hz: (Node 3)

Log F	dBV	Deg	R4 value
1	21.579	-180	1 K
1	16.476	180	3 K
1	20.001	180	1.332 K

The last setting of R4 gives an output of -10 V.

(Example 10, Non-linear circuit, will be covered after example 12.)

<u>Example 11.</u> Fifth Order Active Filter

Element	Reference Designator	Value	Stored in Register
Z1	C1	0.03 uF	R01
Z2	R2	2.0 K	R02
Z3	R3	70 K	R03
Z4	C4	0.02 uF	R04
Z5	C5	1.9 nF	R05
Z6	R6	140 K	R06
Z7	C7	0.01 uF	R07
Z8	R8	12 K	R08
Z8	C9	0.4 nF	R09
Z9	R10	2.7 K	R10
Z10	R11	3.2 K	R11
Z11	R12	10 K	R12
E1	E1	1	Not stored

Listing for "SKF" and "MAT":

```
01 LBL "SKF"
02 RCL 01
03 XEQ "XC"
04 STO "Z1"
05 RCL 04
06 XEQ "XC"
07 STO "Z4"
08 RCL 05
09 XEQ "XC"
10 STO "Z5"
11 RCL 07
12 XEQ "XC"
13 STO "Z7"
14 RCL 08
15 RCL 09
16 XEQ "PRC"
17 STO "Z8"
18 RCL "Z1"
19 RCL 02
20 RCL 03
21 RCL "Z4"
22 XEQ "PZ4"
23 ENTER
24 ENTER
25 RCL/ "Z1"
26 STO "K1"
27 Rdn
```

```
01 LBL "MAT"
02 INDEX "MATK"
03 J+
04 RCL "K2"
05 +/-
06 ra
07 J+
08 RCL "K3"
09 +/-
10 ra
11 J+
12 J+
13 RCL "K4"
14 +/-
15 ra
16 J+
17 RCL "K5"
18 +/-
19 ra
20 J+
21 J+
22 J+
23 J+
24 RCL "K6"
25 +/-
26 ra
27 J+
```

```
28 RCL/ 03
29 STO "K2"
30 Rdn
31 RCL/ "Z4"
32 STO "K3"
33 RCL 03
34 RCL 06
35 RCL "Z5"
36 XEQ "PZ3"
37 ENTER
38 RCL/ 03
39 STO "K4"
40 Rdn
41 RCL/ 06
42 STO "K5"
43 RCL 06
44 RCL "Z7"
45 RCL "Z8"
46 XEQ "PZ3"
47 ENTER
48 RCL/ 06
49 STO "K6"
50 Rdn
51 RCL/ "Z7"
52 STO "K7"
53 RCL "Z4"
54 RCL "Z7"
55 RCL 10
56 XEQ "PZ3"
57 ENTER
58 ENTER
59 RCL/ "Z4"
60 STO "K8"
61 Rdn
62 RCL/ "Z7"
63 STO "K9"
64 Rdn
65 RCL/ 10
66 STO "K10"
67 RCL 11
68 RCL 12
69 XEQ "F2"
70 STO "K11"
71 XEQ "OPAMP"
72 END
```

```
28 RCL "K7"
29 +/-
30 ra
31 J+
32 J+
33 RCL "K8"
34 +/-
35 ra
36 J+
37 RCL "K9"
38 +/-
39 ra
40 J+
41 J+
42 RCL "K10"
43 +/-
44 ra
45 5
46 6
47 STOIJ
48 RCL "K11"
49  +/-
50 ra
51 J+
52 J+
53 RCL "A"
54 +/-
55 ra
56 J+
57 RCL "A"
58 ra
59 INDEX "MATE"
60 RCL "K1"
61 da
62 RCL "MATE"
63 RCL/ "MATK"
64 STO "MATV"
65 END
```

In "OPAMP", be sure that line 06 is: 06 100; and line 09 is: 09 1E4.

From page 17, the order is 6, and from page 16 we want to look at node 6. Some outputs at node 6 are:

Log F	dBV	Deg
2.00	-51.890	84
2.70	-55.156	-107
2.80	-37.701	-122
3.60	2.553	64
6.00	-2.610	-52

The area between log F = 2.0 and log F = 3.6 should show an elliptical response with a very steep climb to the peak value at log F = 3.6. The slope between log F = 2.7 and log F = 2.8 is:

$$\frac{-37.701 - (-55.156)}{2.8 - 2.7} = \frac{17.455}{0.1} = 174.55 \text{ dB/decade.}$$

which indicates a very sharp high pass response.

<u>Example 12</u> Complementary Feedback Amplifier

Element	Reference Designator	Value	Stored in Register
Z1	R1	200	R01
Z2	R2	1 K	R02
Z3	R3	0.1	R03
Z4	R4	10 K	R04
Z5	R5	1.5 K	R05
Z6	R6	300	R06
Z7	R7	5.1 K	R07
E1	E1	+ 15 V	"E1"
E2	E2	- 15 V	"E2"
E3	E3	+ 5 V	"E3"
B1	B1	100	"B1"
B2	B2	100	"B2"

Listing for "SKF" and "MAT":

```
01 LBL "SKF"
02 RCL 02
03 RCL 03
04 XEQ "PZ2"
05 STO "P1"
06 ENTER
07 RCL/ 02
08 STO "K1"
09 Rdn
10 RCL/ 03
11 STO "K2"
12 RCL 05
13 RCL 07
14 XEQ "PZ2"
15 STO "P2"
16 ENTER
17 RCL/ 05
18 STO "K3"
19 Rdn
20 RCL/ 07
21 STO "K4"
22 RCL 06
23 RCL 07
24 XEQ "PZ2"
25 STO "P3"
26 ENTER
27 RCL/ 06
28 STO "K5"
29 Rdn
30 RCL/ 07
31 STO "K6"
32 END
```

```
01 LBL "MAT"
02 INDEX "MATK"
03 1
04 8
05 STOIJ
06 1
07 RCL+ "B2"
08 RCLx 01
09 STOEL
10 I+
11 RCL "P1"
12 +/-
13 STOEL
14 2
15 3
16 STOIJ
17 RCL "K2"
18 +/-
19 STOEL
20 I+
21 J-
22 -1
23 STOEL
24 3
25 7
26 STOIJ
27 RCL "B1"
28 RCLx 03
29 STOEL
30 I+
31 RCL 04
32 STOEL
33 I+
34 1
35 RCL+ "B1"
36 RCLx "P2"
37 +/-
38 STOEL
39 J-
40 RCL "K4"
41 +/-
42 STOEL
43 I+
44 J-
45 RCL "K6"
46 +/-
47 STOEL
48 J+
```

```
49 J+
50 J+
51 RCL "B2"
52 RCLx "P3"
53 +/-
54 STOEL
55 7
56 4
57 STOIJ
58 1
59 STOEL
60 J+
61 +/-
62 STOEL
63 J+
64 J+
65 0
66 STOEL
67 J-
68 J-
69 J-
70 1
71 STOEL
72 J+
73 +/-
74 STOEL
75 8
76 1
77 STOIJ
78 STOEL
79 J+
80 +/-
81 STOEL
82 8
83 ENTER
84 STOIJ
85 0
86 STOEL
87 INDEX "MATE"
88 RCL "E1"
89 da
90 RCL "E1"
91 RCLx "K1"
92 da
93 I+
94 RCL "E3"
95 da
96 RCL "E2"
```

Listing for "MAT" Cont':

```
97 RCLx "K3"
98 da
99 RCL "E2"
100 RCLx "K5"
101 da
102 0.6
103 da
104 0.6
105 da
106 RCL "MATE"
107 RCL/ "MATK"
108 STO "MATV"
109 END
```

Using STOIJ and STOEL function names for large, sparse matrices will result in a shorter listing for "MAT".

Execute "SETUP", DC, Order? = 8. The node voltages and currents are given below in FIX 03 format:

V1 = 3.860	V5 = 3.171
V2 = 3.260	V6 = 1.636
V3 = 3.258	Ib1 = 1.229E-4 (7:1)
V4 = 3.771	Ib2 = 0.001 (8:1)

For an AC analysis of this circuit, it is suggested that the CE hybrid pi high frequency model be substituted for the simple linear DC model used here. A more accurate non-linear model can be created by using the diode equations in reference 5 and the Ebers-Moll models in reference 6.

<u>Example 10</u> Non-linear Circuit.
(See reference 3.)

Element	Reference Designator	Value	Stored in Register
Z1	R1	3 K	01
Z2	R2	2 K	02
Z3	R3	2 K	03
Z4	R4	3 K	04
Z5	R5	10 K	05
Z6	R6	10 Meg	06 (Initial value)
Z7	R7	10 Meg	07 " "
E1	E1	+5	"E1"
E2	E2	-5	"E2"

Listing for SKF" and "MAT":

```
01 LBL "SKF"
02 RCL 01
03 RCL 02
04 RCL 06
05 XEQ "PZ3"
06 ENTER
07 ENTER
08 RCL/ 01
09 STO "K1"
10 Rdn
11 RCL/ 02
12 STO "K2"
13 Rdn
14 RCL/ 06
15 STO "K3"
16 RCL 04
17 RCL 03
18 RCL 07
19 XEQ "PZ3"
20 ENTER
21 ENTER
22 RCL/ 04
23 STO "K4"
24 Rdn
25 RCL/ 03
26 STO "K5"
27 Rdn
28 RCL/ 07
29 STO "K6"
30 RCL 06
31 RCL 07
32 RCL 05
33 XEQ "PZ3"
34 ENTER
35 RCL/ 06
36 STO "K7"
37 Rdn
38 RCL/ 07
39 STO "K8"
40 END
```

```
01 LBL "MAT"
02 INDEX "MATK"
03 J+
04 J+
05 RCL "K3"
06 +/-
07 ra
08 J+
09 J+
10 RCL "K6"
11 +/-
12 ra
13 RCL "K7"
14 +/-
15 ra
16 RCL "K8"
17 +/-
18 ra
19 INDEX "MATE"
20 RCL "E1"
21 RCLx "K1"
22 RCL "E3"
23 RCLx "K2"
24 +
25 da
26 RCL "E2"
27 RCLx "K4"
28 RCL "E3"
29 RCLx "K5"
30 +
31 da
32 RCL "MATE"
33 RCL/ "MATK"
34 STO "MATV"
35 END
```

In order to see the affect of a varying input voltage E3 and to change the "diode" resistor values if forward or reverse biased, a different main program is required which will be labled "VSWP" for "voltage sweep". This main program is similar in structure to "ACAP" and is given below with comments:

```
01 LBL "VSWP"
02 CF 01                    (Diode ON/OFF flag)
03 10E6
04 STO 06                   (Initial values)
05 STO 07                       "       "
06 -16                      (Sweep starts from -16 V)
07 STO "EL"                 (Left voltage)
08 LBL 00
09 STO "E3"                 (Varying input voltage)
10 XEQ "SKF"
11 XEQ "MAT"
12 1
13 STO "Vn"
14 XEQ "GETV"               (Get V1)
15 STO 11
16 3
17 STO "Vn"
18 XEQ "GETV"               (Get V3)
19 STO 13
20 CLA                      (Display setup)
21 FIX 00
22 ARCL "E3"
23 |-" "                    (Append space)
24 FIX 03
25 ARCL 13
26 AVIEW                    (E3 V3)
27 RCL 11
28 X<>Y
29 -
30 X≤0?                   (V3 - V1 < 0 => D6 is ON)
31 SF 01
32 10                       (ON resistance)
33 10E6                     (OFF resistance)
34 FS?C 01
35 X<>Y
36 STO 06
37 2
38 STO "Vn"
39 XEQ "GETV"               (Get V2)
40 RCL- 13
41 X≤0?                   (V2 - V3) < 0 => D7 is OFF
42 SF 01
43 10E6
44 10
45 FS?C 01
46 X<>Y
47 STO 07
48 1
49 STO+ "EL"                (Increment input voltage)
50 16
```

```
51 RCL "EL"
52 X≠Y?                      (Stop at +15 V)
53 GTO 00                    (Repeat)
54 END
```

In "SETUP", temporarily change line from 48 GTO "DCAP" to 48 GTO "VSWP". Execute "SETUP", choose DC, and from page 15 the order must be 3, since we are analyzing three nodes, V_1, V_2, and V_3.

The output from -15 V to +15 V is shown below: (Ignore the first output at E3 = -16 V, since this step determines which diode should be turned on.)

E3	V3	
-15	-6.245	
-14	-5.710	
-13	-5.174	
-12	-4.639	
-11	-4.104	
-10	-3.569	
-9	-3.033	
-8	-2.498	
-7	-1.963	
-6	-1.428	
-5	-0.893	
-4	-0.357	Begin dead zone
-3	0.178	i.e., both diodes OFF
-2	-0.002	
-1	-0.001	
0	0.000	
1	0.001	
2	0.002	
3	0.004	
4	0.005	End dead zone
5	0.893	
6	1.428	
7	1.963	
8	2.498	
9	3.033	
10	3.569	
11	4.104	
12	4.639	
13	5.174	
14	5.710	
15	6.245	

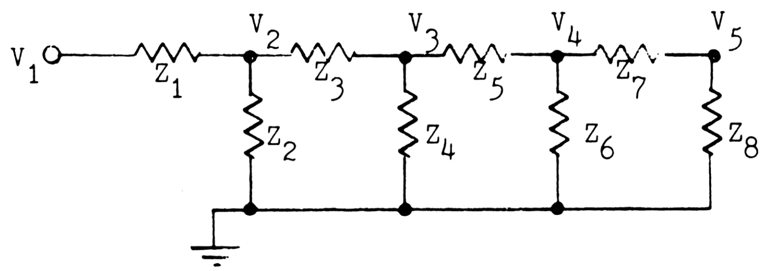
The "glitch" at E3 = -3 V, is due to the discrete 1 V steps in E3. Ideally, the program should be structured so that smaller steps such as 0.1 V, are applied to the circuit and the output displayed only at 1 V or 2 V intervals. The "glitch" would then disappear since the program would more closely simulate the actual circuit where E3 is continuous. However, this is not necessary since the actual circuit operation can be understood using 1 V increments.

APPENDIX

I. Ladder Network Analysis

All circuits analyzed so far have used matrices for the solution form. Ladder networks lend themselves to a more efficient solution form which will run faster.

Given the 4 L-section ladder network shown below:



Let $B_8 = 1/Z_8$

$B_6 = 1/Z_6 + 1/(Z_7 + 1/B_8)$

$B_4 = 1/Z_4 + 1/(Z_5 + 1/B_6)$

$B_2 = 1/Z_2 + 1/(Z_3 + 1/B_4)$

Then

$V_1/V_2 = 1 + Z_1B_2$

$V_2/V_3 = 1 + Z_3B_4$

$V_3/V_4 = 1 + Z_5B_6$

$V_4/V_5 = 1 + Z_7B_8$

Finally $V_1/V_5 =$

$(1 + Z_1B_2)(1 + Z_3B_4)(1 + Z_5B_6)(1 + Z_7B_8)$

Taking the inverse will give the transfer function V_5/V_1.

For output impedance Zo:

$Zo = Z_8//(Z_7 + Z_6//(Z_5 + Z_4//(Z_3 + Z_1//Z_2)))$

Or by chained fractions:

Let $A_2 = 1/Z_2 + 1/Z_1$

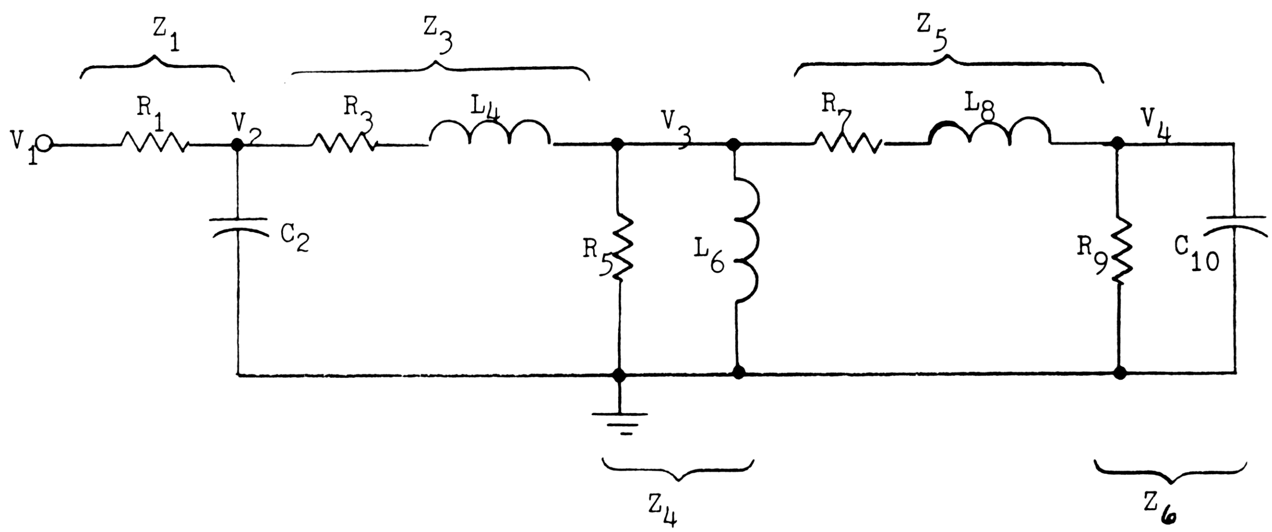
$A_4 = 1/Z_4 + 1/(Z_3 + 1/A_2)$

$A_6 = 1/Z_6 + 1/(Z_5 + 1/A_4)$

$A_8 = 1/Z_8 + 1/(Z_7 + 1/A_6)$

$Zo = 1/A_8$, and similarly for the input impedance Zin.

The ladder network shown below will be analyzed using the above expressions for the output voltage. The circuit is a model of a high frequency transformer. (Ref. 4) The topology is a 3 L-section ladder network.



Although "SKF" and "MAT" may now be inappropriately named, they are retained for the sake of consistency. The high frequency transformer model can be analyzed faster with the following routines than the matrix format used previously.

Store the following values in the registers indicated:

Element	Reference Designator	New AC value	Stored in Register
Z1	R1	10	01
Z2	C2	20 pF	02
Z3	R3	1.5	03
Z3	L4	1 uH	04
Z4	R5	20 K	05
Z4	L6	2 mH	06
Z5	R7	1.5	07
Z5	L8	1 uH	08
Z6	R9	1 K	09
Z6	C10	20 pF	10

Listing for "SKF" and "MAT":

```
01 LBL "SKF"
02 RCL 02
03 XEQ "XC"
04 STO "Z2"
05 RCL 03
06 RCL 04
07 XEQ "SRL"
08 STO "Z3"
09 RCL 05
10 RCL 06
11 XEQ "PRL"
12 STO "Z4"
13 RCL 07
14 RCL 08
15 XEQ "SRL"
16 STO "Z5"
17 RCL 09
18 RCL 10
19 XEQ "PRC"
20 STO "Z6"
21 END
```

```
01 LBL "MAT"
02 RCL "Z6"
03 RCL+ "Z5"
04 1/X
05 RCL "Z4"
06 1/X
07 +
08 STO "B4"
09 1/X
10 RCL+ "Z3"
11 1/X
12 RCL "Z2"
13 1/X
14 +
15 STO "B2"
16 RCL "Z5"
17 RCL/ "Z6"
18 1
19 +
20 RCL "B4"
21 RCLx "Z3"
22 1
23 +
24 x
25 RCL "B2"
26 RCLx 01
27 1
28 +
```

```
29 x
30 1/X
31 END
```

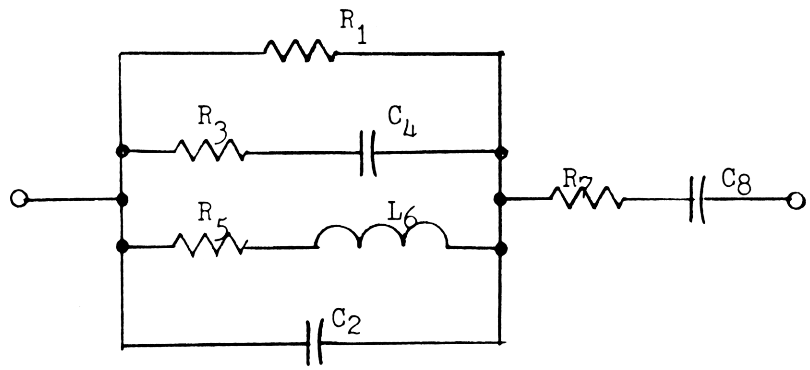
The program "ACAP" must be modified slightly since we are not looking for an element of the "MATV" vector. Delete or flag around line 20 XEQ "GETV", and ignore the Vn? prompt. Some outputs of the transformer model are given below:

Log F	dBV	Deg	
2.00	-19.296	84	(Low frequency response)
5.00	-0.122	0	(Mid-band response)
7.40	8.849	-89	(Resonance peak)
8.00	-23.496	177	(High frequency rolloff)

Note that the resonance peak is followed by a sharp rolloff.

II. Building Branch Impedances with the HP-42S

Branch impedances other tha the simple series and parallel RC or RL given by the subprograms on page 22 are easy to construct. For example, for the branch impedance Z1 shown below



the HP-42S sequence is:

RCL 01 RCL 02 XEQ "PRC" RCL 03 RCL 04 XEQ "SRC" XEQ "PZ2"

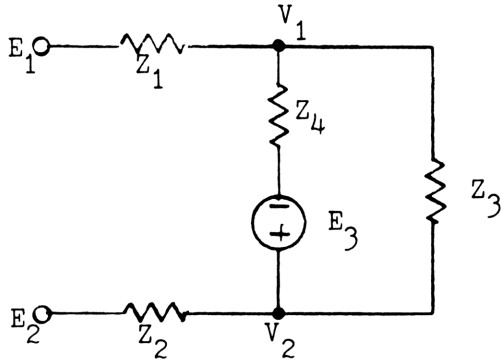
RCL 05 RCL 06 XEQ "SRL" XEQ "PZ2" RCL 07 RCL 08 XEQ "SRC"

\+ STO "Z1"

(Insure that the stack does not fill up and an impedance lost into the T-register.)

III. Floating Voltage Sources

Floating voltage sources are sometimes required for diode and transistor models where the value of the voltage source in series with a resistor is about 0.6V. Whatever the purpose, they are analyzed as shown in the example below:



Step 1.

$$V_1 = E_1K_1 + V_2K_2 + (V_2 - E_3)K_3 \quad \text{or}$$

$$V_1 = E_1K_1 + V_2(K_2 + K_3) - E_3K_3$$

$$V_2 = E_2K_4 + V_1K_5 + (V_1 + E_3)K_6 \quad \text{or}$$

$$V_2 = E_2K_4 + V_1(K_5 + K_6) + E_3K_6$$

Step 3.

$$\begin{vmatrix} 1 & -(K_2 + K_3) \\ -(K_5 + K_6) & 1 \end{vmatrix} \begin{vmatrix} V_1 \\ V_2 \end{vmatrix} = \begin{vmatrix} E_1K_1 - E_3K_3 \\ E_2K_4 + E_3K_6 \end{vmatrix}$$

where the intermediate step 2. is skipped. Note that node V_1 "sees" a voltage of $V_2 - E_3$ when "looking at" node V_2 via impedance Z_4. Conversely, node V_2 "sees" a voltage of $V_1 + E_3$ when "looking at" node V_1 via Z_4. Hence the polarity of the floating source must be observed with care when writing the node equations.

IV. Designing with K Factors

The following is an example of how K factors can be used in circuit design:

Given the N = 4 star network shown on page 3 where the Z's will be assumed all R's, determine the required resistor values such that:

$$Vo = E_1K_1 + E_2K_2 + E_3K_3 + E_4K_4$$

$$= E_1(0.1) + E_2(0.2) + E_3(0.3) + E_4(0.4)$$

for any values of E_1 thru E_4. Note that

$$K_1 + K_2 + ,,, + K_N = 1 \qquad (1)$$

for a star network of N branches.

One solution method would be to generate a set of four simultaneous equations from Kirchoff's Current Law or Kirchoff's Voltage Law, for the four unknown resistor values. However, using K factors allows the simultaneous equations to be avoided:

Let R_1 = 1K (or any convenient value), then:

$R_2 = R_1K_1/K_2 = 1000(0.1)/0.2 = 500$ ohms.

$R_3 = R_1K_1/K_3 = 100/0.3 = 333$ ohms.

$R_4 = R_1K_1/K_4 = 100/0.4 = 250$ ohms.

For an N = 3 branch, assume the design requirements are:

$K_1 = 0.2$, $K_2 = 0.25$, & $K_3 = 0.15$.

In this case, $K_1 + K_2 + K_3 = 0.6$, and to satisfy (1) above, we must provide a fourth branch with V4 = 0 and

$K_4 = 1 - 0.6 = 0.4$.

Again letting R_1 be 1K:

$R_2 = 1000(0.2)/.25 = 800$ ohms,

$R_3 = 200/0.15 = 1333$ ohms,

$R_4 = 200/0.4 = 500$ ohms.

The star or summing network is useful where the output Vo is connected to a high impedance such as non-inverting op amp or comparator inputs.

References:

1. Pulse, Digital, and Switching Waveforms, Millman & Taub, 1965, p. 7.

2. Operational Amplifiers, Design and Applications, Graeme, Tobey, & Huelsman, 1971, p. 202.

3. Introduction to Operational Amplifier Theory and Applications, Wait, Huelsman, & Korn, 1975, p. 147.

4. Reference Data for Radio Engineers, 5th Ed., ITT/Sams, p. 12-1.

5. Algorithms for RPN Calculators, Ball, 1978, p. 272.

6. Modeling The Bipolar Transistor, Getreu, 1976, Tektronix.