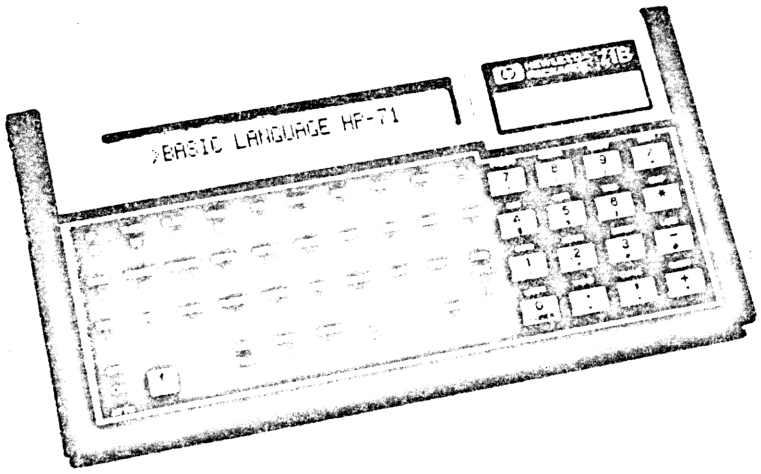
HP-71

HANDHELD COMPUTER

OWNER'S MANUAL



HEWLETT-PACKARD

HEWLETT PACKARD

HP-71

Hand-Held Computer

SERVICE MANUAL

Reorder Number
00071-90055

Portable Computer Division
1000 N.E. Circle Blvd.
Corvallis, OR 97330 U.S.A.

Printed December 1983

Contents

Contents (Continued)

Illustrations

Tables

SECTION
I

General Information

1-1. INTRODUCTION

1-2. This service manual contains information you will require to troubleshoot and repair the HP-71 hand-held computer (HHC).

1-3. This manual is divided into seven sections:

- A general description of the HP-71 (section I).
- A functional description of how the HP-71 works (section II).
- Assembly/disassembly procedures (section III).
- Troubleshooting and test procedures (section IV).
- A description of available accessories (section V).
- A list of replaceable parts (section VI).
- Reference diagrams (section VII).

1-4. Before using this manual in actual repair, read sections I and II to become familiar with the HP-71 and its operation. Then read sections III, IV and appendix A to become familiar with the repair procedures.

1-5. You can find the following additional information, which may be helpful, in the HP-71 Owner's Manual and in the peripheral owner's manuals:

- Battery.
- AC Power Adapter.
- Card Reader Operation.
- Plug-in Modules, ROM/RAM.

1-6. PRODUCT DESCRIPTION

1-7. The HP-71 HHC is an integrated system which features:

- ANSI standard minimal BASIC with extensions.
- Two operating modes:
  - calculator mode.
  - BASIC immediate mode.
- 17.5K bytes of multi-file RAM.
- A 64K byte operating system.
- An 8 by 132 dot matrix single line, 22 character LCD display.
- A 39-key typewriter keyboard with a 16-key numeric keypad.
- All CMOS ICs for low power consumption and continuous memory.
- HP-IL module and hand-pulled card reader plug-in ports.
- Plug-in ports for additional RAM and ROM modules.

1-8. Specifications for the HP-71 are listed in table 1-1.

Table 1-1. Specifications

Physical Properties

- Width: 19.3 cm (7.60 inches).
- Depth: 9.8 cm (3.85 inches).
- Height: 2.7 cm (1.05 inches).
- Weight: 260 grams (9.16 oz).

Environmental Limits

- Operating Temperature: 0° to 45° C (32° to 113° F).
- Storage Temperature: -40° to 55° C (-40° to 131° F).
- Operating and Storage Humidity: 0 to 95% relative humidity.

Power

- Primary: 4 AAA size alkaline batteries.
- Secondary: AC adapter.

Table 1-1. Specifications (Continued)

Display

- Type: Liquid crystal display (LCD).
- Number of characters: 22.
- 8 X 132 dot matrix.
- 16 annunciators.

Keyboard

- 39-key typewriter style.
- 16-key numeric keypad.

Interface

- Type: Hewlett-Packard Interface Loop (HP-IL) module.
- Default at turn on: system controller.

Card Reader

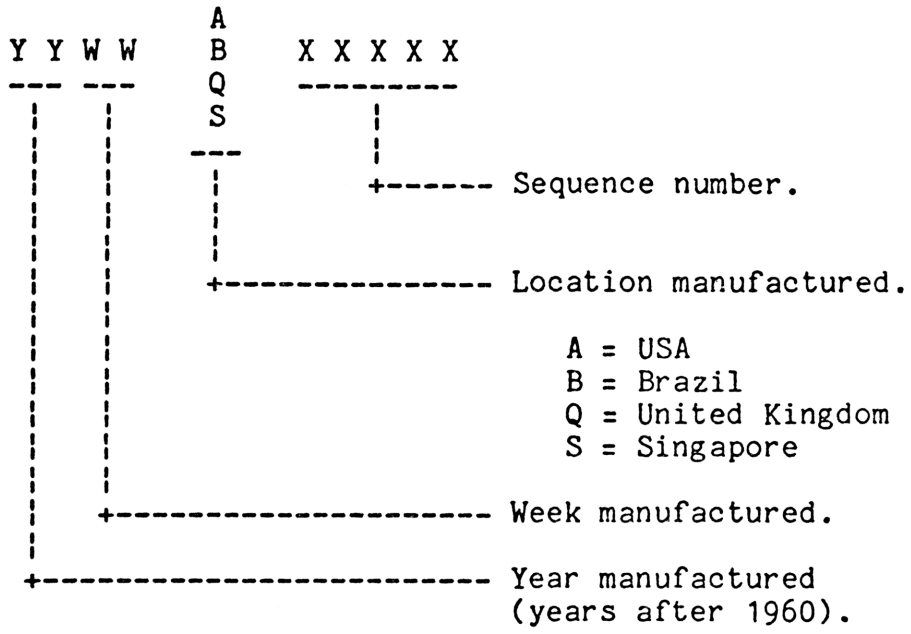
- Maximum read/write speed: 76.2 cm (30 inches) per second.
- Minimum read/write speed: 12.7 cm (5 inches) per second.
- Number of tracks: 2 data and 2 timing.
- Density: 315 bits per centimeter (800 flux reversals per inch).
- Formatted capacity: 650 data bytes per track.
- Encoding method: MFM (modified frequency modulation).

Magnetic Card

- Length: 25.4 cm (10 inches).
- Width: 1.0 cm (0.38 inches).
- Thickness: 0.2 mm (0.009 inches).
- Temperature Limits: 4° to 32° C (40° to 90° F).

1-9. IDENTIFICATION

1-10. The serial number of the computer is used for identification and determination of the warranty status. It is located along the back edge of the bottom case between the four plug-in ports. Its format is shown below:



Note: Date code 2629 or later on HP-71's are machines with a redesign. The flex cable is eliminated, the battery compartment uses "sponge" springs, etc.

SECTION
II

Theory of Operation

2-1. INTRODUCTION

2-2. This section contains a functional description of the six primary logic circuits contained in the HP-71 HHC. They are the:

- CPU (central processing unit).
- RAM (random access memory).
- ROM (read only memory).
- LCD drivers, RAM and LCD
- Power Supply.
- Keyboard.

2-3. INPUT/OUTPUT DEVICES

2-4. Standard input entry to the HP-71 is through the block qwerty typewriter keyboard. Standard output is to the 22-character LCD display.

2-5. Additional devices for providing input and/or output capabilities are:

- 16, 32, 48, 64K-byte plug-in ROM modules.
- 4K byte plug-in RAM modules.
- A programmable 1 Hz. to 4900 Hz. piezoelectric beeper.
- A hand-pulled card reader.
- HP-IL modules.

2-6. The card reader and the HP-IL modules are described elsewhere in this manual. For information about the other I/O devices, refer to the user's documentation.

2-7. ASSEMBLIES

2-8. The CPU integrated circuit (IC) U4, the display RAM ICs (U1, U2, and U3), the LCD, and the keyboard are contained on the keyboard printed-circuit assembly (PCA) mounted in the top case.

2-9. The system ROM IC (U5), the system RAM ICs (U6, U7, U8, and U9), the power supply, and the piezoelectric beeper are contained on the input/output

(I/O) PCA mounted in the bottom case.

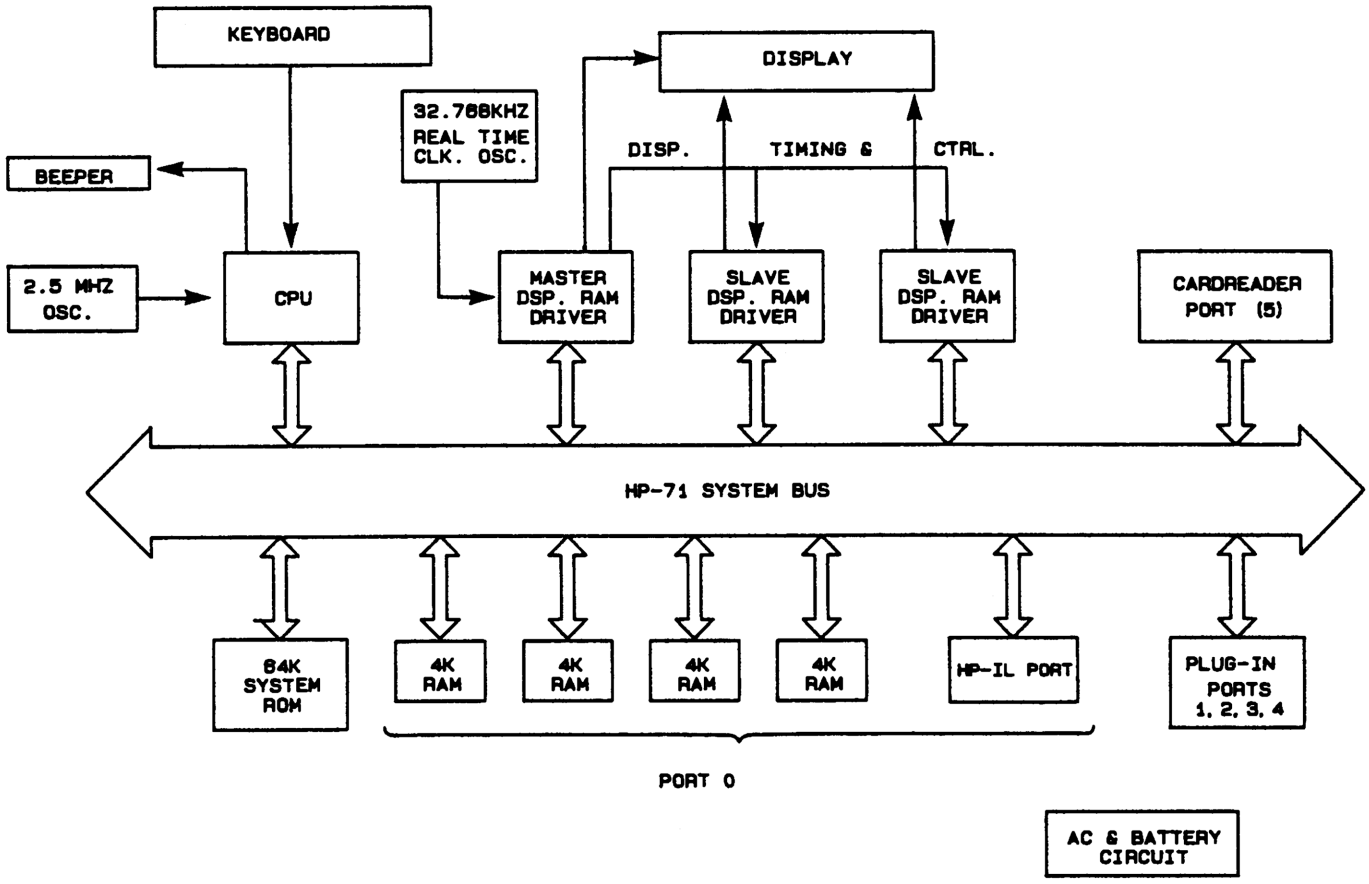


Figure 2-1. HP-71 System Block Diagram

2-10. CPU

2-11. The CPU is designed to execute instructions quickly. The on-chip oscillator, which uses the external components inductor L1, capacitor C3, and capacitor C4, provides a clock frequency of approximately 640 kHz.

2-12. The CPU communicates with other parts of the system via a bus. This bus transmits four bits of data in parallel plus two control signals. Using five four-bit groups or "nibbles" of data, the CPU can address over 1 million nibbles or a half million bytes of data and instructions. The internal logic permits the CPU to operate with words up to 16 nibbles long.

2-13. The two control lines, $\overline{STR}$ (strobe), and $\overline{CD}$ (control/data), control the operation of the bus. The strobe clocks the bus, indicating that there is valid information on the $\overline{CD}$ and bus lines. The state of the $\overline{CD}$ line indicates whether the bus is transmitting data or a command.

2-14. To indicate a data transfer, the CPU pulls the $\overline{CD}$ line low and places the command that indicates the type of data transfer that is to take place after the falling edge of $\overline{STR}$. Command data will be latched by all devices on the rising edge of $\overline{STR}$. When data is being transferred, the $\overline{CD}$ line is held high.

2-15. The CPU can be interrupted by pulling the module interrupt line, $\overline{INT}$, low, by pulling IR15 high by pressing the [ON] key that is connected directly to IR15, or by pulling any of the input register lines, IR0 through IR14, high.

2-16. The signals on each pin of the CPU are listed in table 2-1.

Table 2-1. CPU Signals

PIN	SIGNAL	DESCRIPTION
18	GND	System ground.
26,28-30	BUS0 - BUS3	Four-bit multiplexed address, data, and command bus.
31,67	VDD	Power supply - 4 to 6.5 volts.
34,35	OSC1, OSC2	Oscillator inputs to regulate the CPU's internal oscillator frequency.
37	$\overline{STR}$	System clock - active low.

Table 2-1. CPU Signals (Continued)

PIN	SIGNAL	DESCRIPTION
42	$\overline{CD}$	Control/Data - informs all ICs to load either a command or data. Low - command on the bus.
47	$\overline{INT}$	Interrupt - this line is active when pulled low. When it is pulled low, the CPU completes the current instruction, pushes the program counter (PC) onto the top of the subroutine stack, and initiates the interrupt routine starting at address 0000F (hexadecimal).
48	HALT	When driven high, halts the CPU. The CPU completes the current instruction, and then puts the bus, $\overline{STR}$, and $\overline{CD}$ in a high impedance state.
69,68,66-60 56-50	IR0 - IR15	Input register - used for keyboard and general input to the the CPU (except IR14 for General Input only).
70-72,1-2 6-12	OR0 - OR11	Output register - used to strobe the keyboard, to configure the four module ports, and to drive the beeper.

2-17. The system CPU does not have to be unsoldered in order to permit an external controller to assume control of the system. When HALT is brought high, the system CPU places its bus and control lines in a high-impedance state, effectively isolating the CPU from the system. An external CPU can then be connected to the system by inserting it into port one. (The external CPU is not able to access the keyboard, the internal daisy chain, or the beeper.)

2-18. RAM

2-19. The RAM will retain its memory when it is in light or deep sleep.

2-20. Each RAM chip is organized into a 2K by 4 bit memory. Four RAM chips are incorporated into a hybrid module. Each hybrid module has the capacity

to store 8K by 4 bits of memory (or 4K-bytes). The HP-71 contains four hybrid modules.

2-21. Each RAM or ROM chip has two address registers, a local program counter (PC), and a local data pointer (DP). The local PC is used to access program code stored in the chip, while the local DP is used to access data stored in the chip. This makes it possible for faster CPU access to both the program code and data stored in the same RAM or ROM IC.

2-22. In order to access RAM, the CPU sends a command onto the bus to load the PC or DP followed by five nibbles of address. These five nibbles are loaded into the local PC or DP of each chip. If this address matches the address of the RAM, the next read or write operation will cause the RAM to accept or source data from that address. After the data is transferred, the pointer is incremented. If no other command is sent before another cycle of $\overline{STR}$, the data nibble currently selected by the pointer will be put on the bus, and the pointer incremented. Thus, multiple nibble transfers take place without the need to send an address for each nibble desired.

2-23. Each RAM chip must be configured into the system memory map before it can be used by the system (refer to table 2-5). In this manner, all RAM ICs are mapped uniquely into the address space.

2-24. ROM

2-25. The ROM IC (U5) contains the operating system of the HP-71. It is organized into a hybrid package containing four 32K by 4-bit ROM chips for a total of 64K bytes of read-only memory. It is located in the system memory map starting at address 00000 to 1FFFF (hexadecimal). The system ROM is permanently programmed into this location. It can not be configured to any other address. (Refer to table 2-2 for the common RAM/ROM signals.)

Table 2-2. RAM/ROM Signals

PIN	SIGNAL	DESCRIPTION
1	GND	System ground.
3	OD	Places the bus lines to the RAM/ROMs in a high impedance state.
5 6	DAISY OUT DAISY IN	Lines used by ID, CONFIGURE, UNCONFIGURE, and RESET to configure the RAM in system memory.
7	$\overline{CD}$	Control line that indicates that the bus contains data (CD high), or control information ($\overline{CD}$ low).

Table 2-2. RAM/ROM Signals (Continued)

PIN	SIGNAL	DESCRIPTION
8	$\overline{\text{STR}}$	System clock for system.
9-12	BUS0-BUS3	Four multiplexed data, address, and control bus lines.
13	VDD	Power supply 4 to 6.5 Vdc.

2-26. The system ROM can be either expanded or taken over by plug-in ROM modules; plug-in modules that expand the HP-71's capability are configurable. Application pack modules can be used in any or all of the four ports while plug-in ROMs that take over the system ROM may only be plugged into port 1. Take-over ROMs are used to give the HP-71 totally different capabilities, such as enabling it to be programmed in different languages. When the take-over ROM is plugged into the HP-71, the system ROM is disabled. Plug-in ROMs can range in size from 16K to 64K bytes in size.

2-27. LCD DISPLAY.

2-28. The HP-71 uses an 8 by 132 dot matrix, single line, liquid crystal display. Included in the LCD are 17 annunciators. They inform the user of a low battery (BAT), whether a program is running (PRGM), if a program is suspended (SUSP), if the HP-71 is in calculator mode (CALC), if the HP-71 is set to interpret in radians (RAD), if the 'f' or 'g' keys have been pressed (f, g), where the rest of the line in the display is (←, →), five user display flags (0,1,2,3,4), and if the user definable keyboard is enabled (USER). The annunciators (AC) and [((●))] are not used.

2-29. Three display/RAM ICs (U1, U2, U3) are used to drive and control the display. IC U1 is the master display/RAM while U2 and U3 are slaves. IC U1 provides the timing signal ($\overline{\text{CLK}}$), control signal ($\overline{\text{DON}}$), and the voltage reference (VREF) for the slave ICs. The timing signal is generated by a separate crystal oscillator (Y1) connected to the OSCA and OSCB inputs and divided down to 512 Hz to supply the display clock. IC U1 also drives the 8 rows of the LCD and 40 of the columns. ICs U2 and U3 each drive 48 columns.

2-30. Each dot of the LCD has a corresponding bit in the display RAM. If the bit is a one, the dot will be on. If the bit is a zero, the dot will be off. Eight bytes of the master display RAM (U1) are used to control the row drivers, and 38 bytes plus two bytes for the annunciators at the right of the display are used to control the columns 95 through 132. The slave display ROM U2 uses 48 bytes to control columns 47 through 94. The slave display ROM U3 uses 46 bytes to control columns 1 through 46 plus two bytes for annunciators at the left of the display. All of the display RAM is addressable by the CPU through the system bus. Each display chip also has

512 bytes of user RAM for a total of 1.5K bytes.

2-31. The display/RAM (U1) has the capability to control the contrast (view angle) of the display. The contrast control nibble controls the LCD drive voltages, which control the darkness of the display. The higher the value of the contrast nibble, the darker is the display.

2-32. The display/timer control nibble is located in the master and slave display ICs except for the timer enable bit (written to bit 3) that is functional only on the master chip. Bit 0 turns the display on and off. Setting both bit 0 and bit 1 at the same time will blink the display. Bits 2 and 3 give low-battery information. If bit 2 is set, the battery voltage is below the very-low-battery indicator (VLBI) trip point. If bit 3 is set, the battery voltage is below the low-battery indicator (LBI) trip point. (The VLBI trip point is between 0.8 and 1.2 Vdc below the LBI trip point. The LBI trip point is between 4.3 and 4.5 Vdc.) When written, bit 2 defines the state of the display test bit (accessible only for factory testing). Bit 3, when written, defines the state of the timer enable bit.

2-33. Each of the display/RAM ICs also has a six-nibble timer. This binary counter is decremented each 1/512 second. When the most-significant-bit (MSB) of the timer and the timer-enable bit are set, the display/RAM will respond to a bus service request and will wake up the CPU during shutdown by pulling $\overline{CD}$ low. The timer in the master display driver is used by software to implement a real-time clock.

2-34. Display driver signals are listed in table 2-3.

Table 2-3. Display Driver Signals

PIN	SIGNAL	DESCRIPTION
2,4	OSC A, OSC B	Quartz crystal oscillator connections (32768 Hz).
31-67	VDD	Power supply - 4 to 6.5 Vdc
32-48,50-52 30-14,12-10	C1-C39(odd) C2-C40(even)	Column driver outputs.
53,56 9-6	C41-C47(odd) C42-C48(even)	Column driver outputs (slave drivers only).
56-53,9-6	R1-R8	Row drivers (master driver only).
57	OD	Output disable.
60-63	BUS0-3	System bus.

Table 2-3. Display Driver Signals (Continued)

PIN	SIGNAL	DESCRIPTION
64	$\overline{STR}$	Strobe
65	$\overline{CD}$	Control/data
66	GND	System ground
68,69	CB0,CB1	Used for address configuration and to identify master/slave ICs.
70	$\overline{CLK}$	Display timer clock (driven by master display IC).
71	$\overline{DON}$	Display on (driven by master display IC).
72	VREF	LCD voltage reference (driven by display IC).

2-35. KEYBOARD

2-36. The primary input device to the HP-71 is the 55-key keyboard. Each key is located above a dome shaped snap-disc that is mounted between the top case and the keyboard printed circuit board. The keyboard is divided into a block qwerty-style keyboard and a numeric keypad. The top three rows of keys allow the user to access many commonly used typing aids. The numeric key lets the user access mathematical functions. The keyboard can also be completely redefined by the user except for the [f] and [g] keys.

2-37. When a key is pressed, the snap-disc shorts the corresponding row and column lines. The column lines are connected to the input register of the CPU. As soon as any input register line goes high, an interrupt is issued and the CPU enters the interrupt routine. The operating system waits until the input register hasn't changed for 16 milliseconds (maximum key bounce time), and then scans the keyboard to determine which key(s) are depressed. After the key(s) are known, their corresponding key codes are stored in the key buffer. The system program then looks for input from the keyboard. When a command, such as "INPUT", is executed, the program uses the key codes in the key buffer. (Up to 15 key codes can be stored in the buffer. Any more than 15 are ignored.) The system program then tells the CPU to leave the interrupt routine and resume current program execution.

2-38. The [ON] key differs from the other keys in that it is connected to

the CPU through pin IR15. When the [ON] key is pressed, it interrupts the CPU, which then enters the interrupt routine and services the [ON] key. Pressing the [ON] key interrupts anything the CPU is doing with one exception; it cannot interrupt an interrupt routine. If the CPU is already servicing an interrupt (INT, keyboard, etc.), all other interrupts are disabled.

2-39. CARD READER

2-40. A hand-pulled card reader can be added to the HP-71. It plugs into the rear port on the opposite end from the HP-IL port. It consists of a three-coil magnetic head and its associated electronic circuitry; one coil is for reading timing signals on the card; the second coil is for reading data from the card, and the third coil is for writing data to the card.

2-41. The card reader has its own bus interface and control registers. The bus interface transfers data to and from the HP-71 bus, and from and to a data buffer, depending upon the status of a control register. The bus provides direct access to the control register. The control register locations hold the current status and any error conditions. Since the HP-71 bus is 4-bit parallel and information is stored on the card sequentially, the card reader contains a bidirectional serial-to-parallel converter. The data encoder/decoder converts the information to and from the modified frequency modulation (MFM) encoding format. The timing circuit ensures that the data is read and written correctly. (See figure 2-3 for the card reader block diagram.)

2-42. Each magnetic card has two tracks available for data and two corresponding prerecorded tracks for timing. Each card can store up to 650 bytes on each data track for a total of 1300 bytes of data per card. The card also contains write-protect and file information features. (See figure 2-4 for the magnetic card layout.) The cards must be pulled through the reader at a speed of 5 to 30 inches per second in order to work properly.

2-43. HP-IL MODULE.

2-44. The HP-IL module permits the HP-71 to communicate with up to 30 devices connected to it in an HP-IL using primary addressing and 930 devices using extended addressing. It plugs into the port on the back edge of HP-71 on the opposite end from the card reader port. The module allows the HP-71 to act as either a controller (default), a listener, or talker, and contains the analog circuitry required to transmit and receive on the loop. (See figure 2-5 for the HP-IL block diagram.) It also contains a ROM and a microprocessor and is unique to the HP-71.

2-45. AC POWER ADAPTER AND BATTERY OPERATION

2-46. The HP-71 can be powered by either four AAA alkaline batteries or by the AC power adapter. When the adapter is plugged in, the batteries are electrically isolated by diode CR2. The power from the full wave rectifier, CR3, turns on transistor Q1. The current flow through Q1 is at a higher potential than the batteries which reverse biases CR2. With CR2 reverse biased, current cannot flow from the batteries to the rest of the circuit.

The HP-71 can be powered by the ac adapter with the batteries removed. The HP-71 can not recharge the batteries. When the adapter is not plugged in, CR2 allows the current from the batteries to flow, but the batteries are isolated from the ac connector by transistor Q1. Capacitors C1, C2, and C8 are used to provide power supply noise isolation for the rest of the system. A fresh set of alkaline batteries can maintain memory for 60 hours with the computer running and for at least two years with the computer turned off. A capacitor in the power supply circuit allows the user 30 seconds to change batteries without losing the contents of the RAM provided the computer was first turned off.

2-47. BUS COMMUNICATION

2-48. All addresses, data, and commands are transferred on the four bit bus. Four control signals are used; $\overline{CD}$, $\overline{STR}$, $\overline{INT}$, and HALT. $\overline{CD}$ (Control/Data) line tells whether the information on the bus is a command or data. If $\overline{CD}$ is high, the information is data; if low, the information is a command. STR is the system bus clock and runs at approximately 640 kHz. $\overline{INT}$ is the interrupt line used by the four plug-in ports and the HP-IL module; it is active when low . $\overline{INT}$ is activated when modules are plugged in or pulled out. When HALT is held high, the CPU completes its current instruction and then places the clock ($\overline{STR}$), $\overline{CD}$, and the bus in a high impedance state. Refer to figure 2-2.

2-49. When data is read to or written from memory, only the first address of a block of data needs to be sent. After the starting address is loaded into the appropriate local pointer in memory, the nibble at that address is loaded onto the bus on the next $\overline{STR}$. Consecutive nibbles are then loaded into the bus on consecutive pulses of the $\overline{STR}$. The number of addresses sent out onto the bus is greatly reduced because an address is not sent out for each location in memory being addressed. Up to 16 nibbles of data may be read or written before another address is sent.

Table 2-4. Command, Read, and Write Cycles

REFERENCE	SIGNAL	MINIMUM	MAXIMUM	UNITS
Tacc	Strobe low to chip data high		200	nsec
Tc1	$\overline{CD}$ low to strobe low	30		nsec
Tc2	Strobe high to $\overline{CD}$ high	50		nsec
Tc3	$\overline{CD}$ high to strobe low	100		nsec
Tdm	Strobe high to CPU data invalid	100		nsec
Tdwc	$\overline{CD}$ data valid to strobe high	200		nsec
Tdwd	Data valid to strobe high	100		nsec
To	Strobe cycle time	1.0		usec

Table 2-4. Command, Read, and Write Cycles (Continued)

REFERENCE	SIGNAL*	MINIMUM	MAXIMUM	UNITS
Toh	Strobe high to chip data invalid	20	100	nsec
Tpw1	Strobe low	0.5To		
Tpwh	Strobe high	0.5To		
* - Bus precharge time: 50 nsec minimum.				

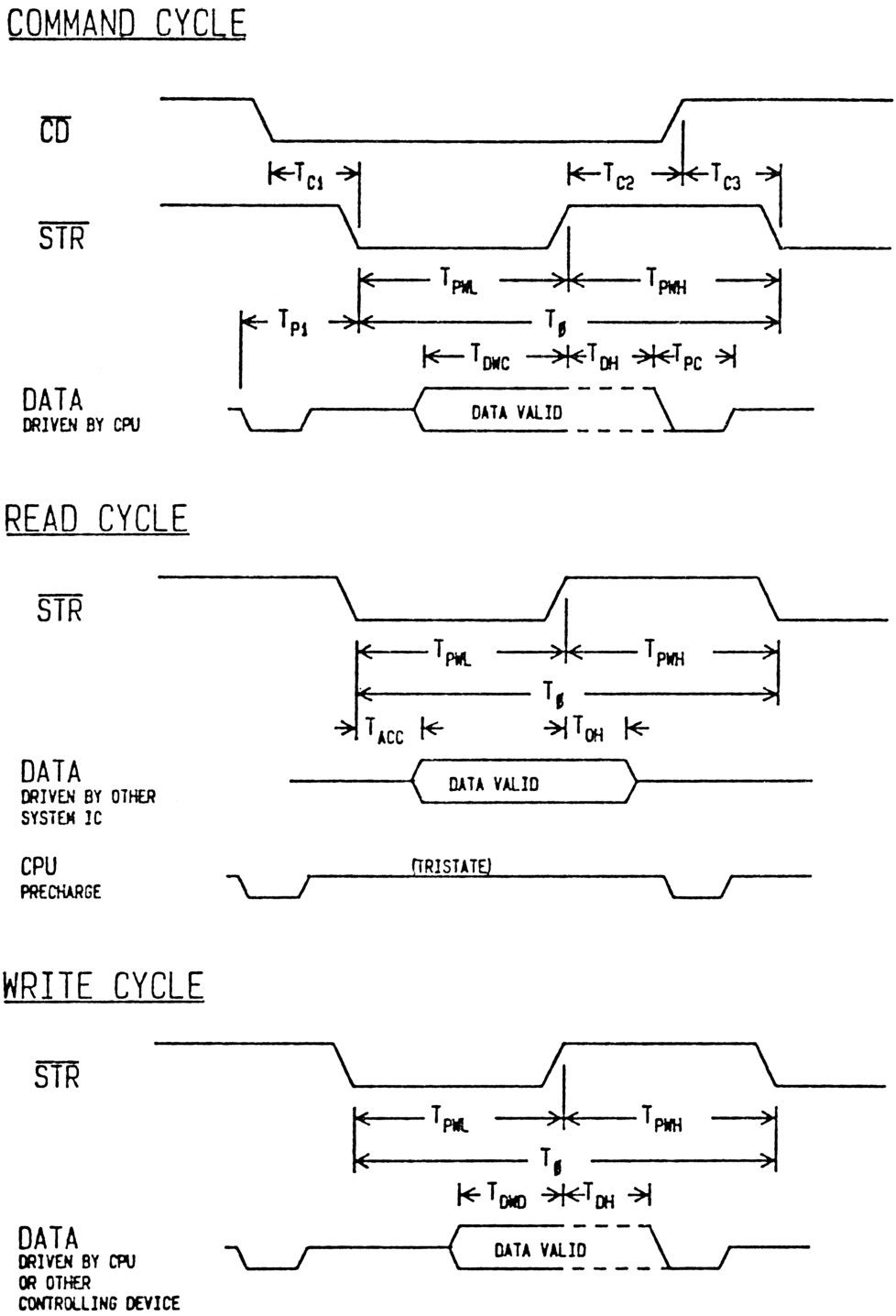


Figure 2-2. Bus Timing Relationships

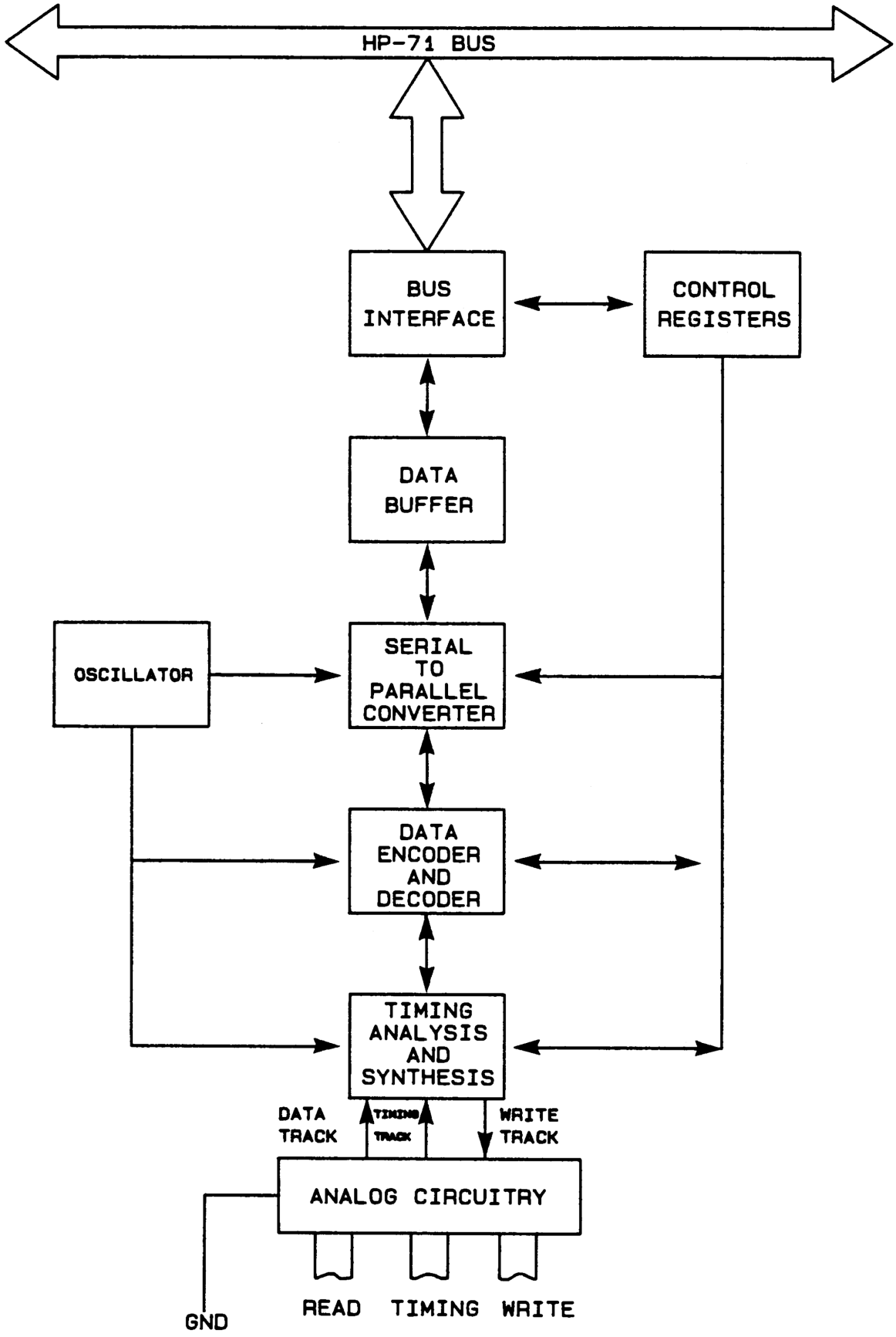


Figure 2-3. Card Reader Block Diagram

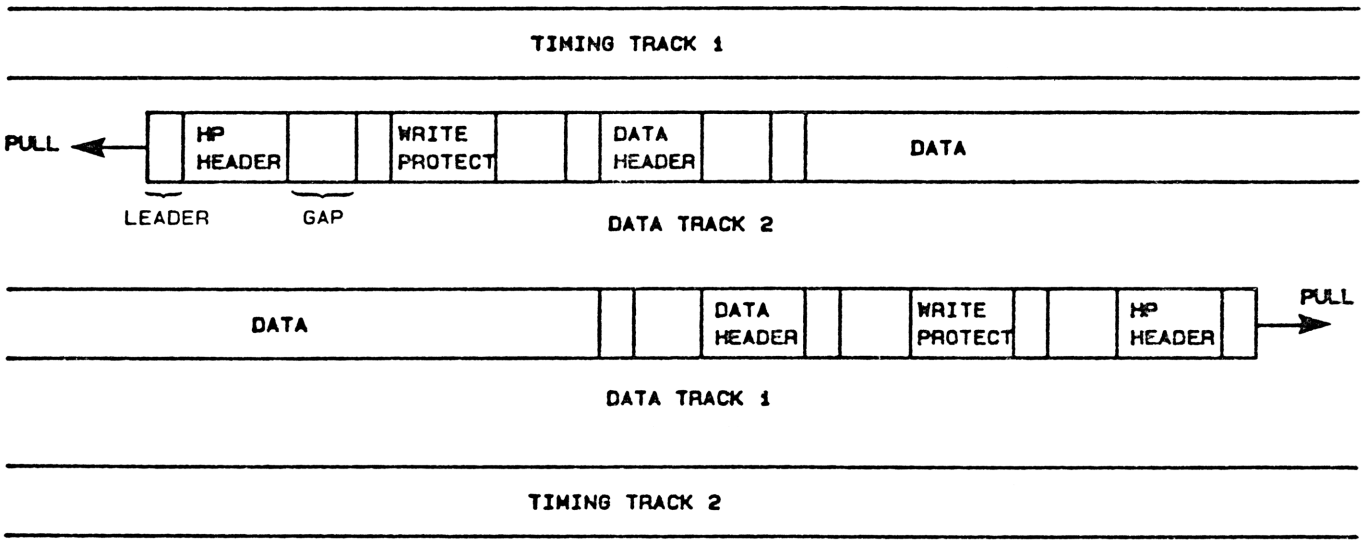


Figure 2-4. Magnetic Card Layout

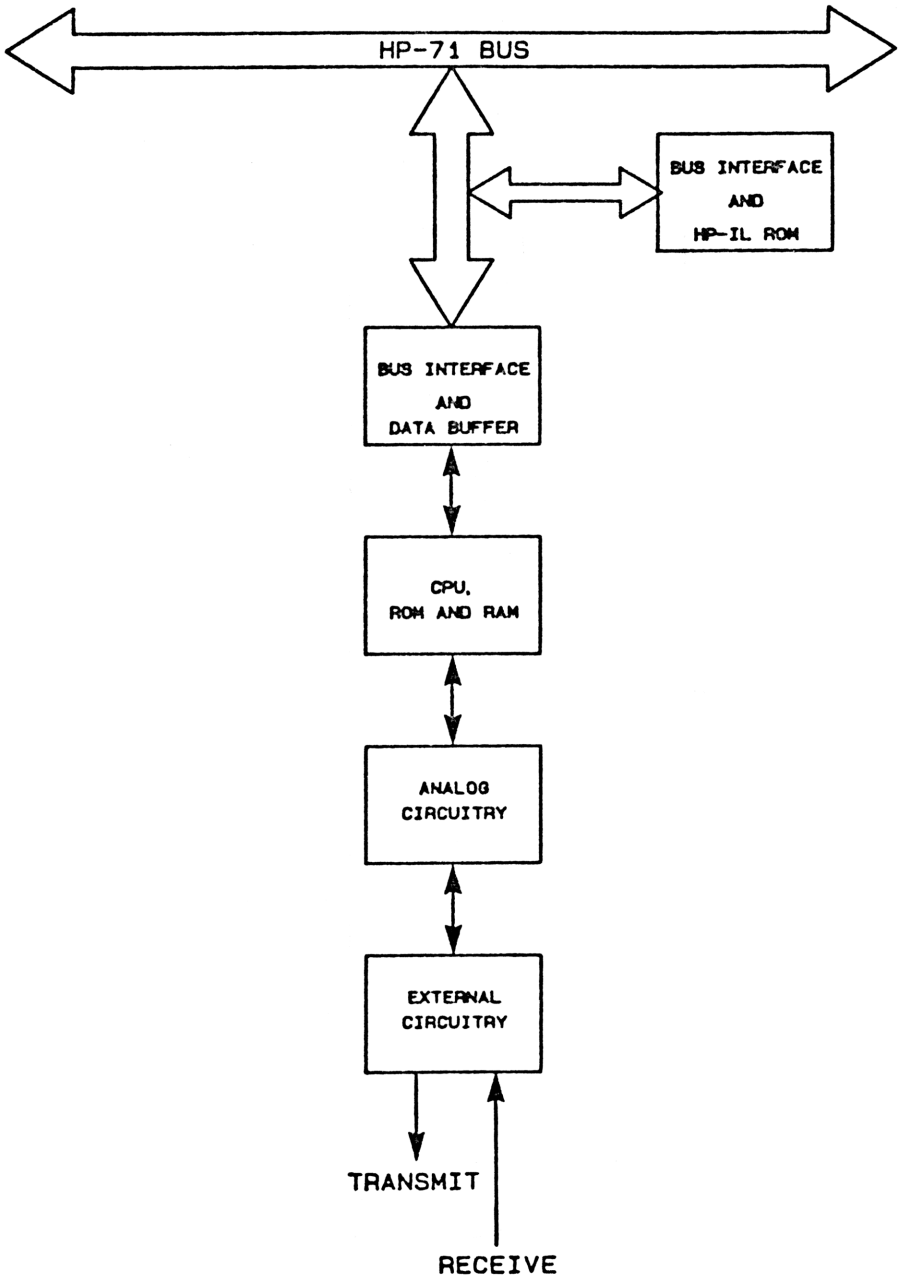


Figure 2-5. HP-IL Block Diagram

2-50. CONFIGURATION OF RAM, ROM, AND I/O

2-51. All memory must be assigned a location in the HP-71's memory map, with the exception of the system ROM (U5) and the Display/RAM ICs (U1-3). This is called configuration. All system RAM (U6-9), plug-in RAM and ROM, and HP-IL plug-in modules must be assigned a specific starting address. Configuration is performed at initial turn-on, after a system reset, or when any plug-in modules except the card reader (which is hard-configured) are inserted or removed.

2-52. RAM, ROM, and I/O are either hard-configured or soft-configured. A device that is hard-configured has a predetermined, unique, location in the memory map. It cannot be moved from its predetermined location. A soft-configured device is assigned a starting address by the configuration routines in system software. The system address map contains areas for RAM, ROM, and I/O devices. Within these areas the specific device may be assigned a starting address.

2-53. Table 2-5 contains the system address map. Only the card reader, system ROM, and Display Driver/Rams are hard-configured.

Table 2-5. System Address Map

DEVICE	LOCATION (hexadecimal)
Operating system ROMs (U5)	00000 - 1FFFF
Memory-mapped I/O devices*	20000 - 2BFFF
Card reader	2C000 - 2C01F
Display RAM (U1-3)	2E100 - 2E3FF
Display-driver RAM (U1-3)	2F400 - 2FFFF
Soft-configured RAM/ROM	30000 - E0000
If nothing is hard-configured at E0000, the address is	- FFC00
Hard-configured ROM	E0000 - FFFFF
* - for example, the HP-IL module.	

2-54. After reset, after power loss, or after a RAM, a ROM, or an HP-IL module is inserted or removed, it is desirable to reconfigure the HP-71 system. The software first must build a list of devices connected to the daisy chain (DI/DO). This list is generated by successively executing an identification instruction (ID) followed by a configure instruction. The ID instruction returns the identification code of the next unconfigured device on the daisy chain. The identification code is returned to the CPU by the device on the daisy chain which has its DAISY-IN (DI) line high. This code contains information as to the device size and type (RAM, ROM, or memory-mapped I/O). Note that hard-configured devices do not respond to the configure command and do not have any identification code. They occupy their preassigned, fixed, addresses.

2-55. The configuration routine temporarily configures the device to 40000_{16}. The temporary configuration is done in order to get the ID of the next device, since a device once configured will raise its DAISY-OUT (DO) LINE (which becomes the DI line for the next device on the chain). Using this procedure, the the table of devices is compiled. The table is then sorted according to size and type. The RAMs are sorted and addressed starting at 30000_{16}, with the larger RAMs occupying the lower addresses. Then the ROMs are assigned addresses with the larger ROMs occupying the higher addresses in the space above RAM. The smaller ROMs fill in any address space available above that (refer to table 2-5). The memory-mapped I/O device(s), such as the HP-IL, are addressed in port order starting at address 20000_{16}. The devices are then unconfigured using a RESET instruction, and the above configuration process is repeated using the correct addresses as generated in the software tables instead of location 40000_{16}.

2-56. When a module is inserted or removed, the $\overline{INT}$ line is momentarily grounded. This causes an interrupt of the software and signals that there has been a physical movement of one of the modules. The software then reconfigures the system.

2-57. MEMORY ORGANIZATION

2-58. The HP-71 can directly address 1,048,576 nibbles of memory. (Refer to table 2-5.) The lower 131,072 nibbles are permanently allocated to the operating system. The next 62,464 nibbles are used only by I/O devices, if present. The following 3,072 nibbles are allocated to the display driver RAM. Note that the configuration table is in the middle of this space. All RAM is configured starting at address 30000_{16}. Plug-in ROM can only be configured in the space between the end of the RAM and address $FFC00_{16}$. The remaining 1,023 nibbles are allocated as a configuration reserved area.

2-59. SYSTEM TIMING

2-60. The HP-71's timing consists of three states; awake, light sleep, and deep sleep. These states are controlled by software which turns the CPU on or off depending on the current state. The system bus clock ($\overline{STR}$) is generated by an oscillator associated with the CPU. During the awake state the oscillator frequency is divided down to provide an $\overline{STR}$ of approximately 640 kHz. When the CPU is shut down during light and deep sleep the $\overline{STR}$ stops and is held high. The timer clock is located in the display drivers (U1-U3) and is not affected by $\overline{STR}$. Only removal of all power will affect the timer. The real time clock uses a 32.768 kHz quartz crystal (Y1) for its reference signal. This signal is divided down to 512 Hz for use in the display-drivers.

2-61. The awake state is the normal operating and highest power-usage state of the HP-71. During this state programs are run and interrupts are processed. This condition is reached any time the system is instructed to wake up either by a keyboard entry, an interrupt, or a due alarm.

2-62. The characteristics of the awake state are:

- The CPU is awake and active.
- $\overline{STR}$ is running (600 kHz TO 650 kHz). 640 Nom.
- $\overline{CD}$ is active.
- The bus is active.
- The LCD is powered and being driven.
- Current drain is approximately 10 ma (mainframe only).

2-63. Light sleep is the idle state of the HP-71. It uses less power than the awake state. When the CPU does not have any processing to do, software invokes light sleep. A half-second timer is set and a SHUTDOWN command is executed that stops $\overline{STR}$ and pulls both it and $\overline{CD}$ high through a high impedance. The bus is precharged low and held low through a high impedance. After 0.5 seconds the timer causes the display driver RAM to wake up the CPU. It then blinks the cursor and goes back to light sleep. This sequence repeats until the CPU is either awakened to service a key entry or a service request, or the 10 minute "time-out" timer forces the HP-71 into deep sleep.

2-64. The characteristics of the light sleep state are:

- $\overline{STR}$ has been stopped and forced high through a high impedance.
- $\overline{CD}$ has been forced high through a high impedance.
- The bus is inactive and held low through a high impedance.
- The LCD is powered and is being driven.
- The CPU is awakened every half second in order to blink the cursor.
- Average current drain is below 750 uA.

2-65. Deep sleep uses the least power of any of the three operating states. It is nearly identical to light sleep with the exception that the LCD is turned off and not driven. Since the maximum setting of the display/RAM timer is four hours, the CPU is awakened by the timer every four hours during deep sleep. On wakeup software updates the timer for another four hours, and then shuts down the CPU. This continues until an internal interrupt occurs such as when a device is plugged into an access port, or the [ON] key is pressed, or until all power is removed. If the [ON] key is pressed, the system enters into light sleep. If all power is removed, the state of the machine will be saved for a minimum of 30 seconds except when the CPU is running.

2-66. The characteristics of the deep sleep state are:

- $\overline{STR}$ has been stopped and forced high through a high impedance.
- $\overline{CD}$ has been forced high through a high impedance.
- The bus is inactive and held low through a high impedance.
- The LCD rows and columns are held high.
- The CPU is awakened every four hours in order to service the real time clock.
- Average current drain is below 30 ua.

Disassembly and Reassembly

3-1.The following procedures describe the steps necessary to disassemble and reassemble the HP-71 HHC in order to replace or repair components that are faulty.

- Separating the Case (procedure 3-3).
- Removing the I/O PCA (procedure 3-4).
- Removing the Flex Cable (procedure 3-5).
- Soldering the Flex Cable (procedure 3-6).
- Reassembling the HP-71 (procedure 3-7).

3-2.Disassembly and reassembly tools are listed in table 3-1. For additional aid, see the exploded view, figure 6-1.

Table 3-1. Recommended Tools

HP PART/MODEL NUMBER	DESCRIPTION
0470-1026	Adhesive, RTV (GE102 or Dow-Corning 732).
	Hot bar:
8690-0009	Handle.
8690-0332	Heater, (110V only).
8690-0333	Desolder bar.
8690-0334	Heater, (220V only).
8700-0003	Knife, X-acto.
8710-1394	Screwdriver, bit, Torx #6.
8710-1404	Screwdriver, handle.
8730-0008	Screwdriver, small, flat blade.
N/A	Screwdriver, '00', flat blade.
8090-0892	Solder, 63/37, 1% flux.
00071-60902	Soldering Clamp, flex.
N/A	Soldering Iron, temp. controlled (371° C (700° F)).
8710-0026	Tweezers.

CAUTION

Be sure you take adequate precautions regarding electrostatic discharge. All the ICs in the HP-71 are CMOS. Work at a bench setup that is electrostatically protected. Otherwise, components may be permanently damaged or degraded.

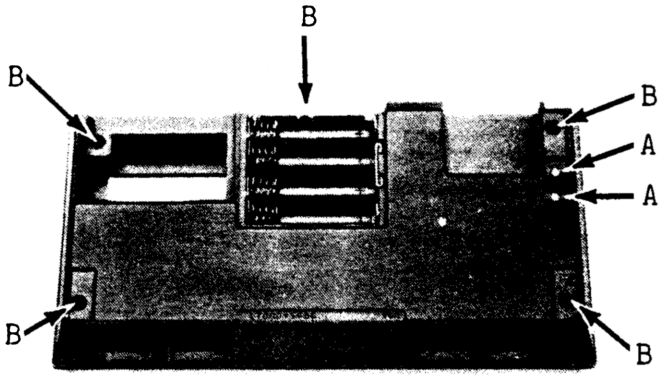
3-3. SEPARATING THE CASE

a. Remove all plug-in modules and/or module doors in the four front ports. Also remove the HP-IL and card reader modules.

b. Place the HP-71 on the repair bench face down with the ROM/RAM ports towards you.

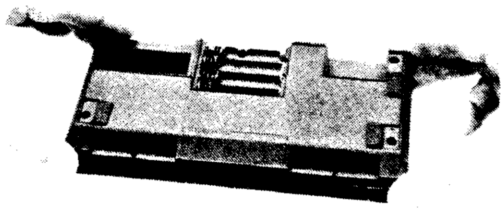
c. Remove the battery access door and batteries. Remove and discard badly worn or defective rubber feet to expose the three screws. Peel them off using a sharp knife.

d. Remove the two 00-90 screws near the edge of the bottom case (A).



e. Using a Torx #6 screwdriver, remove the five screws (B).

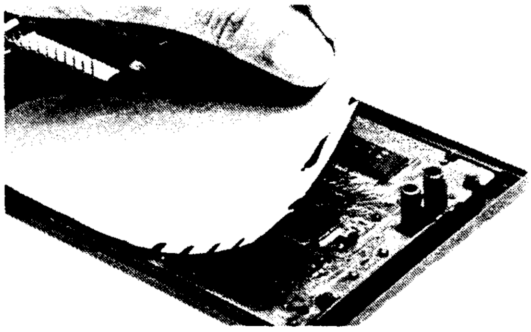
f. Carefully lift off the bottom case by gently pulling it towards you to unsnap the cases. When unsnapped, lift the bottom case off to the left of the keyboard assembly being careful not to pull on the flex cable. Place the bottom case down so the I/O PCA is visible.



CAUTION

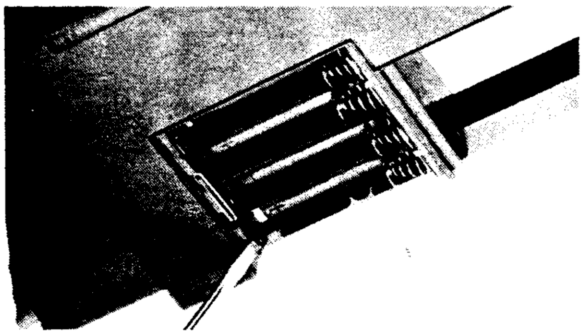
Do not put excessive strain on the flex cable. You may break a solder connection or crack traces in the flex cable if you do.

g. Lift the ESD shield off of the keyboard PCA.

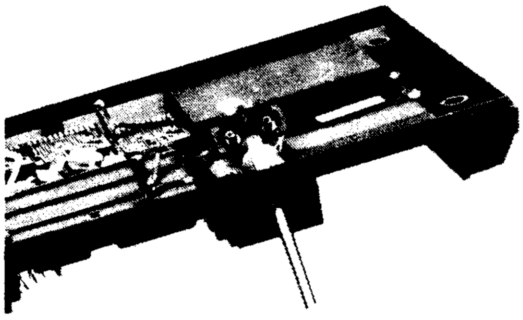


3-4. REMOVING THE I/O BOARD.

a. Using a small screwdriver, press the two battery contacts up and out of the bottom case.

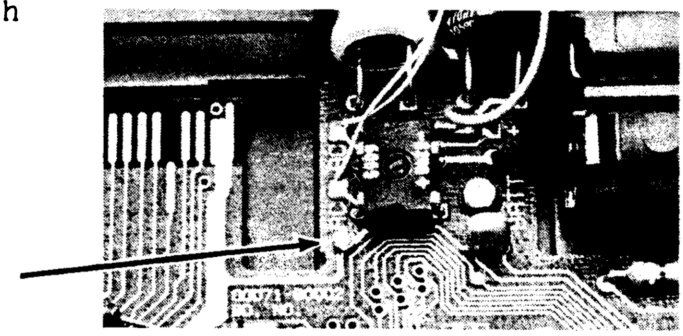


b. Using a small screwdriver, press the ac adapter up and out of the bottom case.

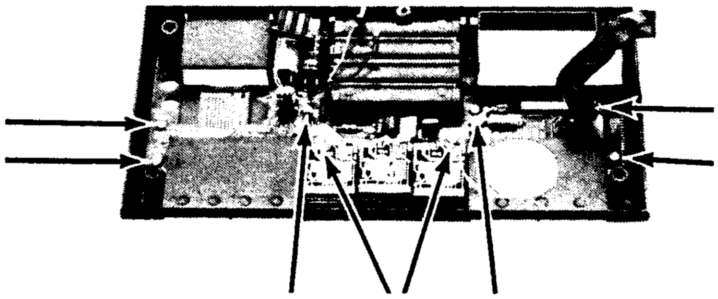


c. Unsolder the beeper leads from the beeper being careful not to overheat the beeper.

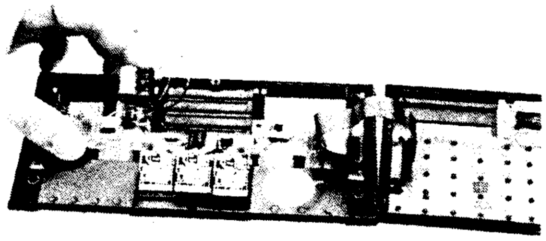
d. Remove the 00-90 screw and 5/64 inch nut near CR3 on the I/O PCA.



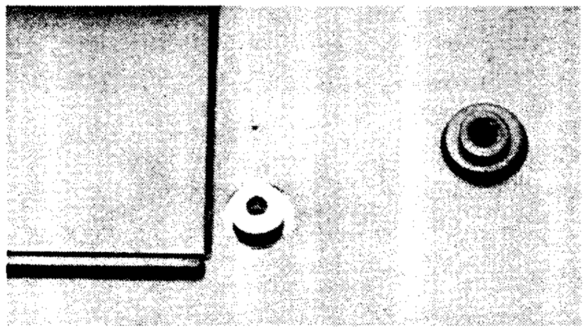
e. Remove the eight screws holding the I/O PCA in the bottom case using a Torx #6 screwdriver.



f. Grasp the I/O PCA near the power supply, tip it up, and slide it out of the case.

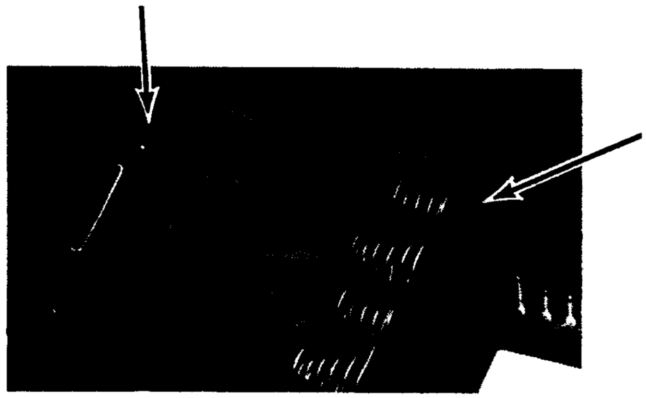


g. Remove the spacer in the bottom case.



h. To reinstall the I/O PCA, perform steps a through g in the reverse order.

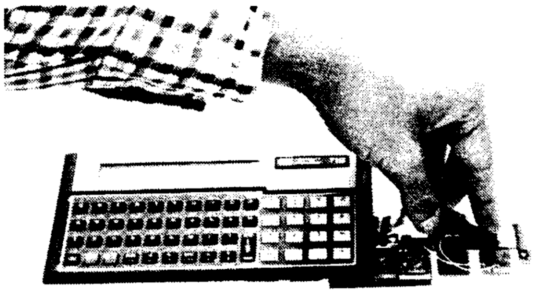
i. Measure the resistance between the back label and battery ground. The resistance should be one ohm or less. If the resistance is greater than one ohm, check that the standoff is making good contact with the I/O PCA and back label. Clean and/or replace the standoff as required.



3-5. REMOVING THE FLEX CABLE

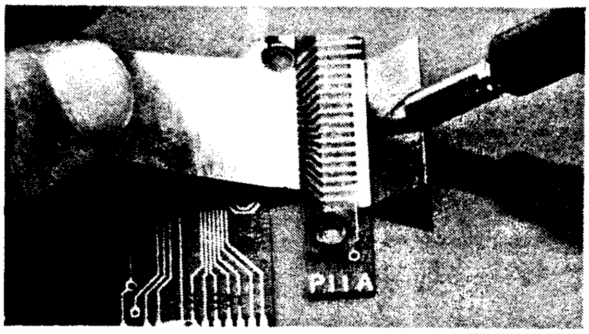
> **NOTE**
>
> Normally, it is necessary only to remove the flex cable from the I/O PCA. New keyboard assemblies come with flex cables already attached. If a flex circuit is defective, both ends of the cable must be unsoldered from the PCAs.

a. When unsoldering the I/O end of the flex cable, it is necessary to remove the I/O PCA from the bottom case (paragraph 3-4). Place the silicone rubber insulator under the flex cable end of the I/O PCA. When unsoldering the flex cable from the top case, remove the strain-relief clamp from the top case.

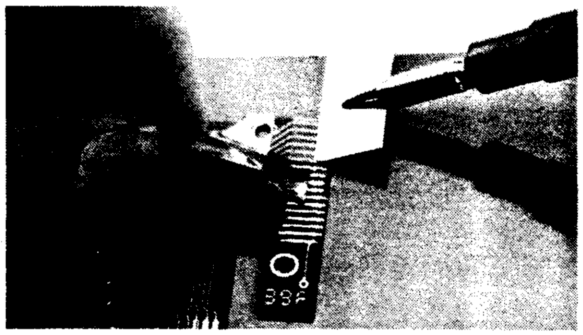


> **CAUTION**
>
> Do not pull hard on the flex cable. You may pull it off the I/O PCA or top case PCA damaging both the flex cable and the PCA.

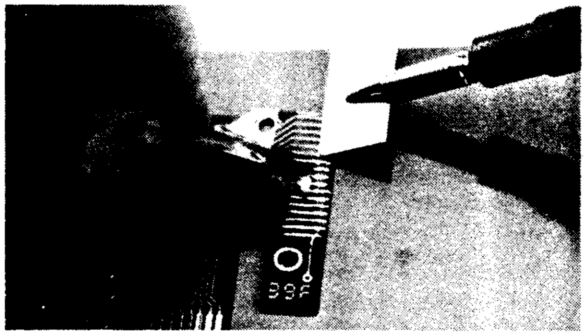
b. Apply the hot bar evenly to the ends of the traces on one side of the PCA.



c. As soon as the solder is melted, gently lift the flex cable away from the PCA.



d. Move the hot bar over to unsolder the remaining traces. As soon as the solder melts, lift the flex cable from the PCA.

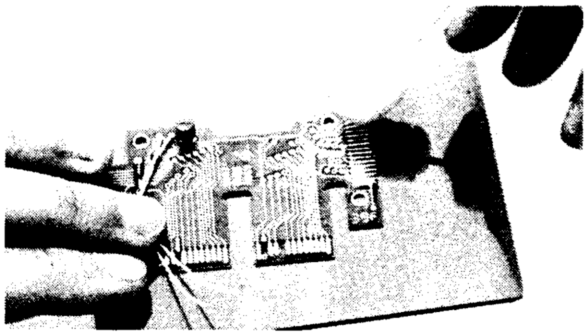


3-6. SOLDERING THE FLEX CABLE

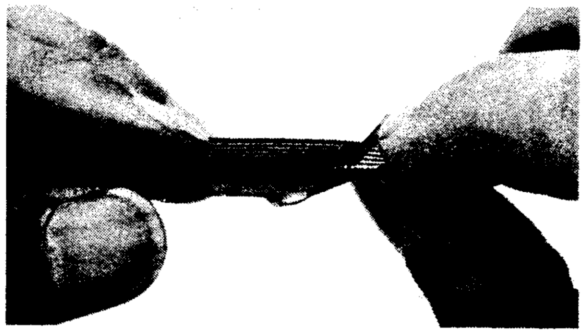
> **NOTE**
> To perform this step on the I/O PCA, the PCA must be removed from the bottom case. A temperature-controlled soldering iron and the specified solder and flux must be used. Otherwise, the PCA can be damaged and/or the reliability of the flex connection reduced.

a. Reflow the solder on the PCA traces in the direction shown by the arrow in the picture. Add a small amount of solder if needed to cover each trace with a nice semi-round dome of solder. Too much solder may cause bridging between the traces.

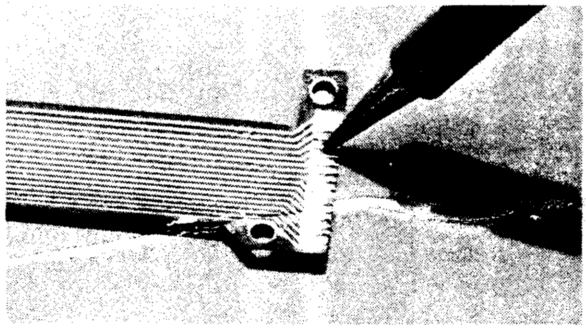
b. Spread a small amount of flux across the middle of the traces on the PCA.



c. Using your fingers, flatten the edge of the flex circuit.



d. Reflow the solder on the edge of the flex cable.

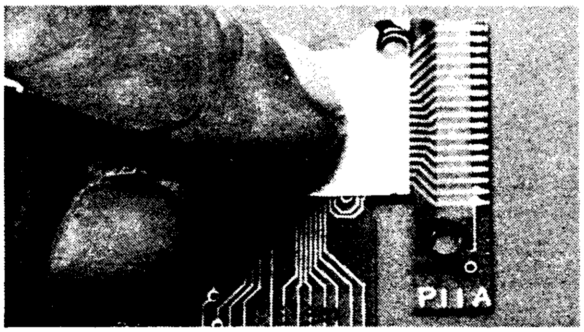


CAUTION

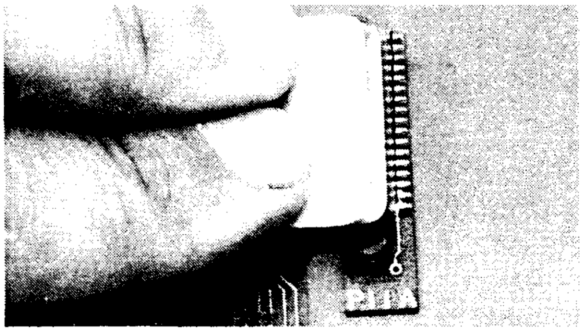
Do not touch a trace of the flex cable with the soldering iron for more than 2 seconds. Excessive heat may build up causing the flex circuit to delaminate.

e. Depending on which end of the flex cable is being soldered, position the PCA on the other end on top of the PCA to be soldered so that the flex cable almost covers the PCA traces.

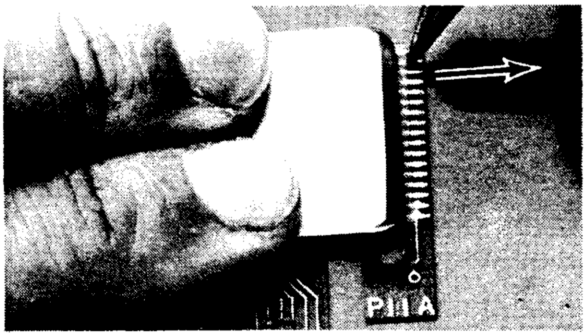
f. Align the traces of the flex cable with the traces of the PCA. It may be helpful to use a small piece of double sided tape to hold the flex circuit in place for soldering.



g. Position the flex holder on the flex cable so that 1mm of cable is exposed at the end.



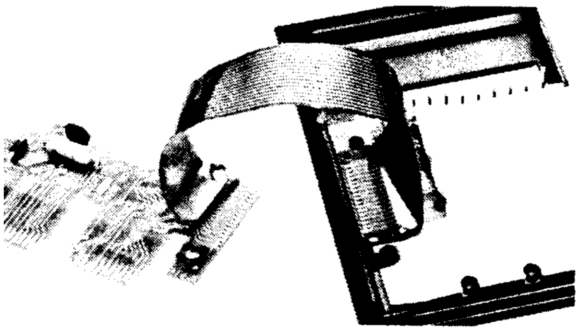
h. Heat each trace on the PCA (one at a time) for 3 seconds. Do not press down on the traces with the soldering iron. Traces may break or delaminate from the PCA. Remove the iron by sliding it off the edge of the PCA.



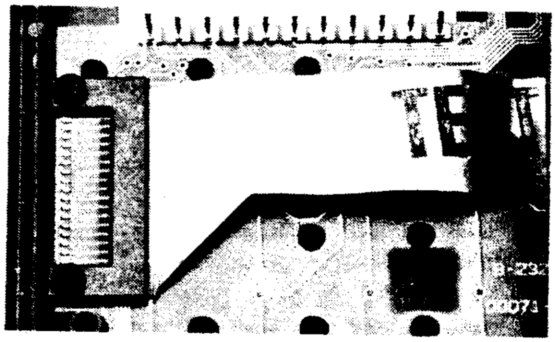
i. Remove the flex holder.

j. Inspect for bad solder connections and bridging between traces.

k. With an ohmmeter, test the resistance of all solder connections from keyboard traces to the I/O PCA traces. The resistance should be less than 0.5 ohms.



l. After soldering the flex cable to the top-case PCA reinstall the strain-relief clamp.



3-7. REASSEMBLING THE HP-71

> **NOTE**
>
> In order to perform this step, the I/O PCA must be secured in the bottom case, and the flex circuit must be soldered to both the I/O and keyboard PCAs.

a. Measure the resistance between the bezel and the top label. The resistance should be less than one ohm. If it is greater than one ohm, the welded connection between the bezel and the top label is faulty, and the top case should be replaced.

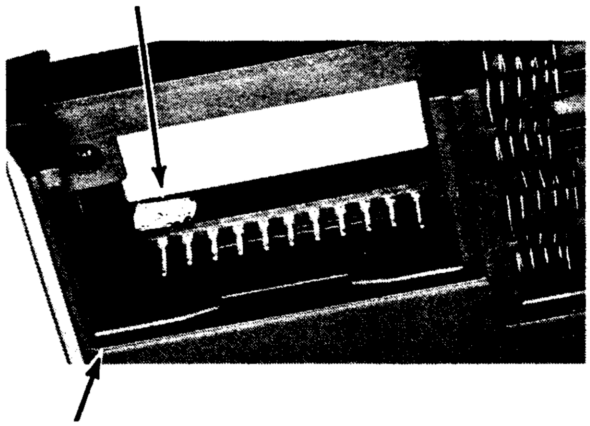
b. Replace the ESD shield.

c. Place the bottom case on top of the top case. Be careful not to pull on the flex cable.

d. Insert and tighten the 5 Torx screws.

e. Install the two 00-90 screws.

f. Measure the resistance between the bezel and the back label and between the top label and the back label. If either measurement is greater than one ohm, make sure that the screws in the standoffs are secure and that the screw heads are making good electrical contact with the back case.



g. Replace the three feet.

h. Insert the batteries and port covers. Insert the card reader and HP-IL module if any.

SECTION
IV

Troubleshooting and Testing

4-1. INTRODUCTION

4-2. This section contains the procedures you should follow to isolate the cause of a problem in an HP-71 Hand-Held Computer. It also gives the procedure to verify that a unit is good. Tools that facilitate service are listed in table 4-1.

CAUTION

Ensure that adequate precautions are taken regarding electrostatic protection. Work at a bench set-up that is electrostatically protected. Otherwise, components may be damaged.

Table 4-1. Recommended Tools

HP PART/MODEL NUMBER	DESCRIPTION
82059D	AC Adapter
5061-7246	Diagnostic ROM
HP3468A	Digital multimeter
00071-60901	Jumper-cable
HP1220A	Oscilloscope
8690-0227	Solder Sucker, ESD resistant
N/A	Soldering iron, 371 C (700 F) temperature controlled

4-3. This section contains four troubleshooting tables. The first is table 4-2, Test Procedures. This table will guide you to the particular troubleshooting tables. It is the main structure of the repair process. Table 4-3, Power Supply and Clocks Troubleshooting, is used to verify and troubleshoot the power supply, CPU clock, and the real time clock. Table 4-4, Beeper Troubleshooting, is used to verify and troubleshoot the beeper circuit. Table 4-5, Logic Troubleshooting, is used with the diagnostic ROM to verify and troubleshoot the operation of the logic circuits in the HP-71.

4-4. When troubleshooting the HP-71, start with table 4-2, Test Procedures. Sequentially follow the steps in this table. If an error occurs, follow the instructions and branch to the described troubleshooting table. When you have completed the instructions in the troubleshooting table return to the place in the table 4-2 from which you branched, and continue. For

example, if the unit under test did not beep upon turn on and the display turned on, then you would branch to table 4-4, Beeper Troubleshooting. After performing the required steps in table 4-4, you should branch back to table 4-2 where you left off and then be directed to table 4-5, Logic Troubleshooting.

4-5. If a component part or assembly must be replaced, replace it and then perform the entire troubleshooting table again to verify that the fault has been repaired.

4-6. Some steps will tell you to check all of the solder connections on various ICs. In doing so, gently try lifting the leads one at a time. If a lead can be lifted, solder the lead to the trace with a narrow tipped, temperature controlled soldering iron. Be careful not to desolder the surrounding leads. After you have resoldered the lifted lead, do not attempt to clean the PCA. It is very easy to contaminate any one of the exhaust holes under the snap domes on the keyboard PCA. If three or more leads are lifted on one topcase assembly, replace that PCA. After any soldering, return to and repeat the step where the failure occurred. A magnifying lens can be very helpful in finding and repairing poor or bridged solder connections.

4-6. INITIAL PREPARATION

4-7. Perform the following steps before attempting to troubleshoot the HP-71:

a. Visually inspect the unit for physical damage. Replace any assemblies or parts that are physically damaged.

b. Determine the customer's concern if possible. Frequently the customer includes a message with the unit describing the problem.

- If the problem relates to the AC adapter, Card Reader, or HP-IL, test it according to the procedures in section 6.
- For functional problems with the unit, perform the test and repair procedures beginning with table 5-2, Test Procedures.
- For application problems refer to application documentation.

Table 4-2. Test Procedures

STEP	ACTION
1. Insert a set of known good test batteries.	

Table 4-2. Test Procedures (Continued)

STEP	ACTION
2. Plug the AC adapter into the HP-71 under test. 3. Make sure the HP-71 is turned off. 4. Plug the diagnostic ROM into port one. *	
5. Press [ON].	If the display turns on and the beeper beeps, then repeat step 5 once with only batteries and once with only the AC adapter connected. If the display and beeper continue to work, proceed to step 6. If only the display turned on, then proceed to the following tables in order: A. Table 4-4, Beeper Troubleshooting. B. Table 4-5, Logic Troubleshooting. C. Table 4-3, Power Supply and Clock Troubleshooting. If only the beeper beeped, proceed to the following tables in order: A. Table 4-5, Logic Troubleshooting. B. Table 4-3, Power Supply and Clock Troubleshooting. C. Table 4-4, Beeper Troubleshooting.

* If the flex cable has been removed and the jumper cable is being used to connect the I/O board and keyboard, Ports 2, 3, 4, and the Beeper will be disabled.

Table 4-2. Test Procedures (Continued)

STEP	ACTION
	If neither the display turned on nor the beeper beeped, disconnect the AC adaptor and momentarily short the end pins (VDD and GND) in the card reader port. If unit fails to turn on, proceed to the following troubleshooting tables in the following order: A. Table 4-3, Power Supply and Clock Troubleshooting. B. Table 4-5, Logic Troubleshooting. C. Table 4-4, Beeper Troubleshooting.
6. Run the multiple test. In response to 'SELECT TEST' press [M].	If any test fails, proceed to table 4-5.
7. Run the Low Battery Indicator (LBI) test. In response to 'SELECT TEST' press [B].	The Low Battery Indicator bit should be set if battery voltage is between 4.3 and 4.5 Vdc and "BATT:LOW" is displayed. "BATT:NONE" if bit battery voltage is above 4.5 Vdc.
8. Reassemble the HP-71.	
9. Run the multiple test.	If any test fails, proceed to table 4-5.

Table 4-3. Power Supply and Clock Troubleshooting.

STEP	ACTION
1. Disassemble the unit and place it with the PCAs exposed if not already done.	
2. Plug in the AC adapter.	
3. Measure VDD.	If VDD is between 5.5 and 6.4 Vdc, proceed to step 11.
4. Measure the AC voltage across the CR3 side of T1.	If the voltage is not between 9 and 14 Vac, replace T1.
5. Measure the DC voltage across the + side of CR3 (or the + side of C2) and ground.	If the voltage is less than 10 Vdc, replace CR3.
6. Measure the voltage at the cathode end of VR7.	If the voltage is less than 6.4 Vdc, replace VR7.
7. Measure the voltage across the base and emitter of Q1.	If the voltage is greater than 0.6 Vdc, replace Q1.
8. Remove the AC adapter.	
9. Measure the voltage across the collector and emitter of Q1.	If the voltage is less than 3.0 Vdc, replace Q1.
10. Measure the voltage across CR2.	If the voltage is greater than 0.6 Vdc, replace CR2.
11. Press [ON].	

Tabl 4-3. Power Supply and Clock Troubleshooting (Continued)

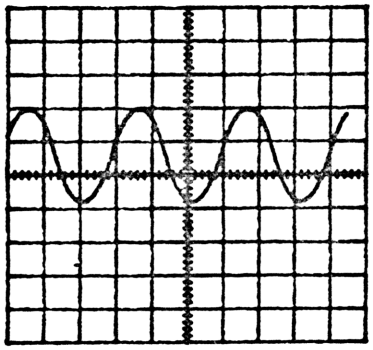
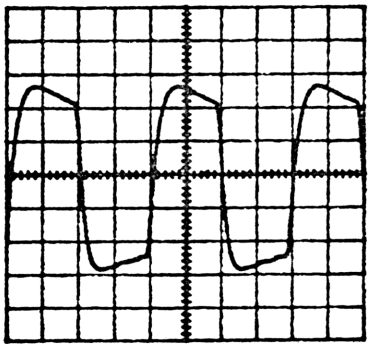
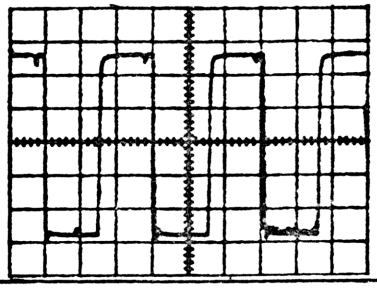
STEP	ACTION
12. With an oscilloscope, probe OSC B on the master display RAM.	If a 32.768 kHz. signal is not present, replace Y1. Check the master display RAM (U1) solder connections. If the signal still is not present, replace the top case.
 10 usec/div 1 volt/div	
13. With an oscilloscope, probe the OSC 1 line of the CPU.	2.56 Nom. If a 2.5 MHz. signal is not present, check the CPU solder connections, then replace in order L1, C5, and C4. If the signal still is not present, replace the top case.
 0.1 usec/div 1.0 volt/div	

Table 4-3. Power Supply and Clock Troubleshooting (Continued)

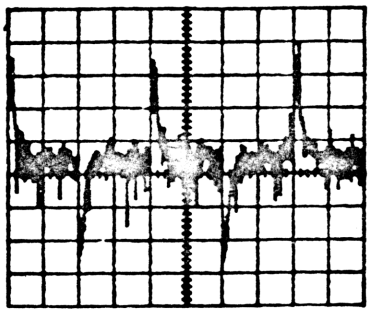
STEP	ACTION
14. With an oscilloscope, probe the STR line of the CPU.	If a 640 kHz signal is not present, replace top case.



0.5 usec/div
1.0 volt/div

Table 4-4. Beeper Troubleshooting.

STEP	ACTION
1. Dissassemble the unit under test.	
2. Plug in the AC adapater.	
3. Check the beeper wires and flex cable for continuity.	Replace or resolder bad wires and connections.
4. With an oscilloscope, probe the base pin of Q2. Then press [ON] to make the beeper beep.	If a signal cannot be seen, check the solder connections on CPU leads OR10 and OR11, capacitor C9, and resistors R20 and R21. If good, replace Q2, and then the top case.



0.2 msec/div
0.2 volt/div

Table 4-4. Beeper Troubleshooting (Continued)

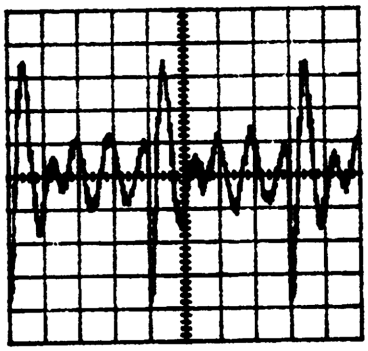
STEP	ACTION
5. With an oscilloscope, probe the collector pin of Q2. Then press [ON] twice.  0.2 msec/div 1.0 volt/div	If a signal cannot be seen, replace Q2, Y2, and L2 in order.
6. Are steps 3, 4, and 5 good?	If so, then replace the beeper transducer. Use a small amount of RTV on the back of the new unit to secure it in place.

Table 4-5. Logic Troubleshooting.

STEP	DISPLAY	ACTION
1. Remove all plug-in RAMs and ROMs.		
2. Disassemble the HP-71.		
3. Install a known good set of batteries.		
4. Make sure the HP-71 is turned off.		

Table 4-5. Logic Troubleshooting (Continued)

STEP	DISPLAY	ACTION
5. Insert the diagnostic ROM into port one.		
6. Press [ON]. (The CPU test is executed. The clock frequency should be between 600 and 650 kHz.	CPU OK HP71 CLOCK 640KHZ SELECT TEST	The CPU is good. Proceed to step 7. If clock frequency is out of range, replace L1, C5, and C4 in order.
	CPU BAD nnnn	Check the CPU and display RAM lead solder connections for lifted leads. If n does not equal 9 or B, the CPU is bad. Replace the top case. If n equals 9 or B, perform the tests in step 8 (RAM test). If any of these tests fail, perform the indicated repair, then repeat step 6.
		If display does not turn on, check the flex cable and IC solder connections. Check the power supply if you haven't already done so, then replace the top case.

Table 4-5. Logic Troubleshooting (Continued)

STEP	DISPLAY	ACTION
7. Press [M] Multiple Test	DRCTD MUTPL CPU TEST	If "CPU OK" is displayed, proceed to step 8. If "CPU BAD" is displayed, check the solder connections on the CPU. If the CPU is still bad, replace the top case.
8. M/F RAM Test	M/F RAM TEST CHKG RAM #n	This message is displayed while the the display RAM chips are being tested.
	RAM OK	The display RAM tested good.
	RAM BAD #n	Check the CPU and display RAM solder connections. If the display RAM test still fails, replace the top case.
9. P/I ROM Test **NOTE** When a hybrid RAM/ ROM is replaced, apply a small amount of RTV to the top edge of the RAM/ROM to secure it to the I/O PCA.	P/I ROM TEST Pnd XXK ROM #m: OK Chip # in ROM module. ROM size in nibbles. Device # Port number.	If BAD is displayed, replace the ROM in the port indicated, and repeat the test.

Table 4-5. Logic Troubleshooting (Continued)

STEP	DISPLAY	ACTION
10. P/I RAM Test. Includes soft configured internal RAM.	P/I RAM TEST Pnd XXK RAM #m: OK Chip #in module. RAM Size in Nibbles. Device # Port number.	If 'BAD' is displayed, then replace that module and repeat the test. Note that for the internal soft configured RAM port 0 is located on the I/O PCA. The sequence '#m' (1 to 4) will be repeated four times. The RAM device numbers are 1 for U9, 2 for U8, 3 for U7 and 4 for U6.
11. Display Test	DISPLAY TEST TIMERS OK (Four Patterns) DSP RAM OK ABC123XYZ +=END TEST READY	Watch display for missing annunciators or row/column dots. Display is good. Press <+>, and proceed to step 12.
	TIMERS BAD n	Check solder connections on Display RAMs for lifted leads. If n=S, repeat this test. If n=S again, repeat step 4 and repair as required. If the unit still fails, replace the top case. If n=1, 2, or 3, check Y1 (U1-OSC B) with an oscilloscope for the presence of a 32.768 kHz. signal. If the signal is absent, replace Y1 and repeat

TABLE 4-5. Logic Troubleshooting (Continued)

STEP	DISPLAY	ACTION
		the test. If the signal is still absent, replace the top case. If the signal is present but the timers are bad, the master display driver is bad. If there is no $\overline{CLK}$ signal, replace the top case.
12. Keyboard Test.	KEYBD TEST START AT 1-0	Press keys from to right, top to bottom row. If a dead or double enter key is encountered with normal key strokes, replace the top case.
13. Key Bounce Test	BOUNCE TEST START AT 1-0 1-0: n/m . . . . 4-13: n/m MAX n/m	Press keys from left to right, top to bottom row. If either n or m is greater than 15 milliseconds with normal keystrokes, replace the top case.
14. a) Sleep Test	DEEP SLEEP "ON"=DP SLEEP	The unit is in light sleep.
b) Press any key except [ON].	WAKEUP LT SLEEP OK "ON"=DP SLEEP	The unit has passed the light sleep test.
		Repeat step 11, and repair as required.
	CPU ERRORS	Repeat step 6, and repair as required.

Table 4-5. Logic Troubleshooting (Continued)

STEP	DISPLAY	ACTION
	LT SLEEP ERRS	Replace the top case CPU and display connections are good.
	"ON"=DP SLEEP	
c) Press [ON].*	TIMER WAKEUP 1 OK TIMER WAKEUP 2 OK TIMER WAKEUP 3 OK	The unit is in deep sleep. If any timer is 'BAD' retest and run the display test. Check the display RAMs for good solder connections. Replace the top case if timers are still bad.
d) Press [ON] again.	WAKEUP DP SLEEP OK CPU OK HP71 CLOCK 640KHZ	The unit passed the test.
	DP SLEEP ERRS	Replace the top case.
	WAKEUP ERRORS	Deep sleep test has failed. The CPU did not wake up properly. Replace the top case.

* If the customer complains of short battery life (high current drain), measure the current drain from the batteries during the deep sleep test. Disconnect the ac adapter when making this measurement. If the current is greater than 30 ua, isolate the PCA with high current. Check for solder bridges and replace keyboard assembly if faulty. If the I/O board is faulty, check the power supply circuit (table 4-3). If the problem still exists, isolate the hybrid with excessive current and replace it.

Table 4-5. Logic Troubleshooting (Continued)

STEP	DISPLAY	ACTION
15. Remove the diagnostic ROM. Press the [ON] and [/] simultaneously, then press [2][endline] to run the mainframe	INIT:1 INIT:2 ROM TEST 1G 2G 3G 4G	If any number is followed by the letter B, check the flex cable solder connections. If OK, replace the system ROM on the I/O PCA, and repeat the test.

Table 4-6. Error Codes

DISPLAY	DESCRIPTION
"CPU OK"	CPU test passes.
"CPU BAD nnnn"	CPU test failure. n=1: to 8: internal CPU error. n=9: clock error in CPU/Display timer or system bus. n=B: read/write error to RAM CPU/Display RAM/system bus failure. n=C to F: fatal CPU operation error
"RAM OK"	RAM test passes.
"RAM BAD #n"	n=1: Display RAM Chip U3 fails. n=2: Display RAM Chip U2 fails. n=3: Display RAM Chip U1 fails.
"ROM OK"	ROM test passes.

Table 4-6. Error Codes (Continued)

DISPLAY	DESCRIPTION
"ROM BAD #n"	n=1: Self-Check ROM Failure.
"TIMERS OK"	Display timers pass test.
"TIMERS BAD #n"	Display timers bad. n=S: CPU service request error. n=1: Display Chip U3 timer fails. n=2: Display Chip U2 timer fails. n=3: Display Chip U1 timer fails.
"DISPLAY RAM OK"	Display RAM passes test.
"DISPLAY RAM BAD #n	Display RAM bad. n=1: Display Chip U3 fails read/ write. n=2: Display Chip U2 fails read/ write. n=3: Display Chip U1 fails read/ write.
"Pnd xxK RXM #m": OK"	Plug-in RAM/ROM under test passes.
"Pnd xxK RXM #m": BAD"	Plug-in RAM/ROM under test fails. n=port number. d=device number (hexadecimal) xx=size of RAM/ROM in nibbles. m=chip number in device group (d).
"P/I RXM OK"	Plug-in RAM/ROM test passes.
"P/I RXM BAD"	Plug-in RAM/ROM test fails.

Accessories

5-1. INTRODUCTION

5-2. This section identifies electrical accessories that are available for the HP-71 HHC. Defective accessories should be replaced rather than repaired since the cost of a new unit is usually less than the cost of repair.

5-3. HP 82400A CARD READER

5-4. The HP 82400A card reader is shown in figure 5-1. This is a hand pulled card reader unique to the HP-71.

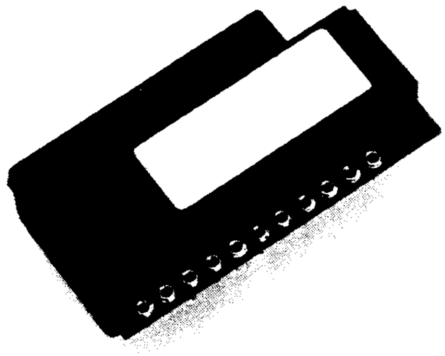


Figure 5-1. HP 82400A Card Reader

5-5. The date code located on the card reader indicates the week and year that it was manufactured. The format is described below:

```
YYWW
----
|  |
|  +----------Week manufactured.
|
|
|
+-------------Year Manufactured
              (years since 1960).
```

5-6. INITIAL PREPARATION

5-7. Perform the following steps before attempting to troubleshoot the card reader:

a. Remove the card reader from the HP-71 and visually inspect it for physical damage. Replace the card reader assembly if the case or connector pins are damaged.

b. Check the connector pins on the HP-71 for damaged or missing pins. Replace the top case assembly if defective.

c. Verify the operation of the HP-71 by performing the procedures in section IV, table 4-2.

d. Reinstall the card reader in the HP-71 and proceed to table 5-1.

Table 5-1. Card Reader Troubleshooting

STEP	DISPLAY	ACTION
1. Turn the HP-71 off and plug the diagnostic ROM into port one.		
2. Plug an ac adaptor into the HP-71.		
3. Insure the card reader is properly installed.		
4. Turn the unit on.		If the unit fails to turn on, proceed to section IV.
5. Press [*] key to run the card reader test. (Do not insert the card before pressing the key.)	"WRITE CARD"	Align the test card.
	"PULL CARD"	Pull card at the normal speed. If the card is pulled too fast or too slow or a bad SOC start of card) occurs, the test will repeat.
6. Follow instructions in the display.	"READ CARD (FAST)"	Align the test card.
	"PULL CARD"	Pull card fast enough to generate a too-fast error. If the pull was too fast, the test continues; if not, an error message is displayed, and the test is repeated.

Table 5-1. Card Reader Troubleshooting (Continued)

STEP	DISPLAY	ACTION
	"READ CARD (SLOW)"	Align the test card.
	"PULL CARD"	Pull card slowly. An error message is generated. Test continues. If pull is too fast, an error message is generated, and the test is repeated.
	"READ CARD (TEST)	Align the test card.
	"PULL CARD"	Pull card at normal speed.
	"CARD RDR: OK"	The card reader is good.
	"CARD RDR: NN"	The card reader is bad. NN=EN Request Enable =RQ Request Register =DT Data Error =CN Control Error If the card reader fails, repeat the test to verify the failure; replace the card reader if it is still bad.

5-8. HP 82401A HP-IL MODULE

5-9. The HP 82401A HP-IL Module is shown in figure 5-2. It is unique to the HP-71.

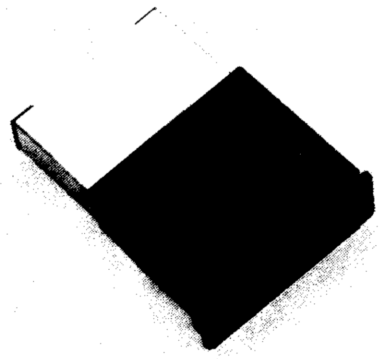
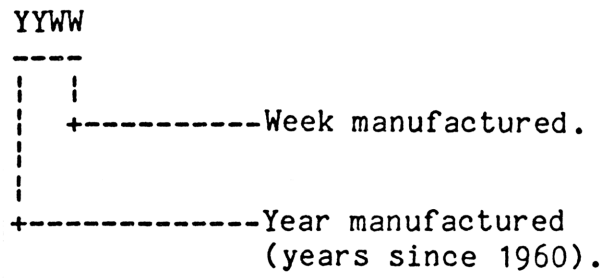


Figure 5-2. HP 82401A HP-IL Module

5-10. The date code located on the HP-IL module indicates the week and year that it was manufactured. The format is described below:



5-11. INITIAL PREPARATION

5-12. Perform the following steps before attempting to troubleshoot the HP-IL module:

a. Remove the HP-IL module from the HP-71, and visually inspect it for physical damage. Replace the module if the case or connector pins are damaged.

b. Verify the operation of the HP-71 by conducting the test procedures in section IV, table 4-2.

c. Reinstall the HP-IL module in the HP-71, and proceed to table 5-2.

Table 5-2. HP-IL Troubleshooting

STEP	DISPLAY	ACTION
1. Turn the HP-71 off, and plug the diagnostic ROM into port one. 2. Plug an ac adaptor into the HP-71. 3. Insure that the HP-IL module is properly installed. 4. Turn the unit on.		

Table 5-2. HP-IL Troubleshooting (Continued)

STEP	DISPLAY	ACTION
5. Press the [3] key to run the P/I ROM test.	"P/I ROM TEST" "Pnd xxK ROM #m: OK"	The HP-IL ROM under test is good.
	"Pnd xxK ROM #m: BAD"	The HP-IL ROM under test is bad. n=port number d=device number xx=size of ROM in nibbles m=chip number in device Replace the HP-IL module.
6. Connect an HP-IL cable across the HP-IL port to form a loop.		
7. Press the [/] key to run the HP-IL test.	"HP-IL TEST" "HP-IL OK"	The HP-IL module is OK.
	"HP-IL: NNN	The HP-IL module is bad. NNN=MB Bus interface =CPU HP-IL CPU =TMR HP-IL Timers =LP Loop data error Replace the HP-IL module.

5-13. AC ADAPTER

5-14. Various ac adapters (table 5-3) are available for use with the HP-71 HHC. These adapters are the same as those used with the HP-75C HHC and the HP-IL peripheral devices .

Table 5-3. AC Adapters

MODEL NUMBER	VOLTAGE*	IDENTIFICATION
HP 82059D	110	US
HP 82066B	220	Europe
HP 82067B	220	UK desktop
HP 82067B Opt. 001	220	UK with RSA plug
HP 82068B	220	Australia
HP 82069B	110	Europe

* indicates nominal voltage; acceptable ranges are 90 to 120 Vac and 210 to 250 Vac.

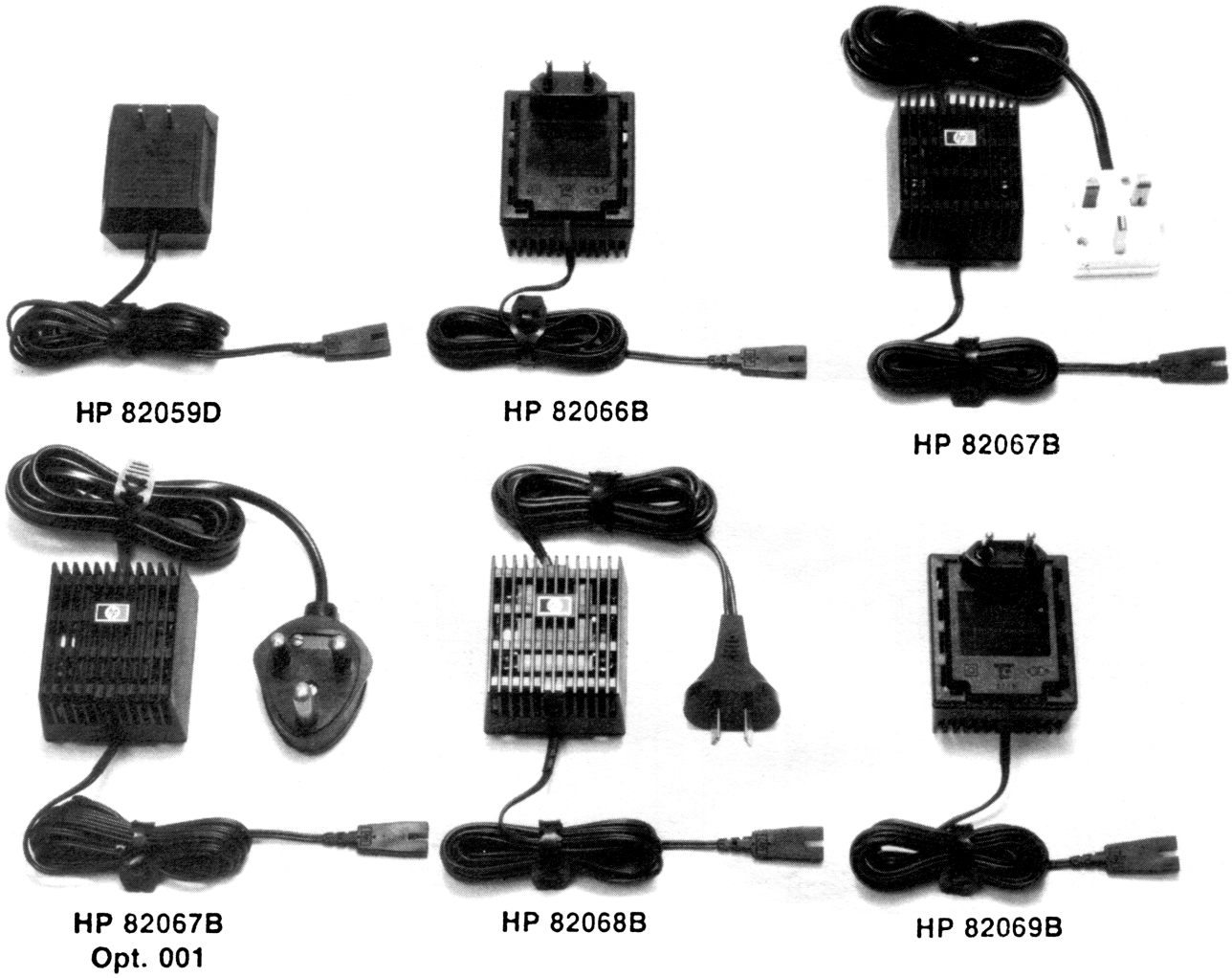
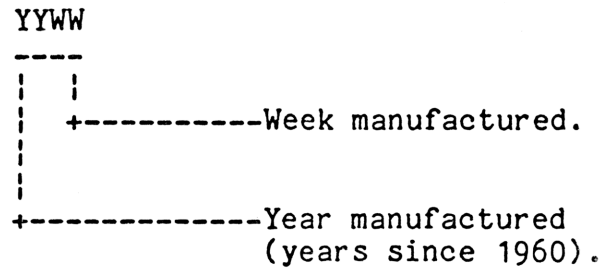


Figure 5-3. AC Adapters

5-15. The date code located on the adapter indicates the week and year in which it was manufactured. The format is described below.



5-16. To determine whether the adapter is functioning properly, follow the procedure in table 5-3.

Table 5-3. AC Adapter Troubleshooting

STEP	SPECIFICATION	ACTION
1. Plug the AC adapter into an outlet of the proper voltage.		
2. Measure the output voltage with an ac voltmeter.	9.9 to 13.3 Vac for an input voltage of 110 or 220 Vac.	If in range proceed to step 3. If out of range, replace the ac adapter, and stop testing here.
3. Connect a 12 ohm, 2 watt resistor to the terminals of the voltmeter.		
4. Measure the output voltage.	5.3 to 7.3 Vac for an input voltage of 110 or 220 Vac.*	If in range, proceed to step 5. If out of range, replace the ac adaptor, and stop testing here.

* More generally, VOUT should equal (VIN / 110) X 11.6 Vac + or - 1.7V or (VIN/220) X 11.6 Vac +or- 1.7. (VIN is the ac voltage of the power outlet.)

Table 5-3. AC Adapter Troubleshooting (Continued)

STEP	SPECIFICATION	ACTION
5. While masuring the voltage, wiggle and pull the wires at the transformer and at the connector.	Greater than or equal to 5.3 Vac.*	If in range, the ac adaptor is good. If the voltage drops below range, replace the ac adaptor

* More generally, VOUT should equal (VIN / 110) X 6.3 Vac + or - 1.0V or (VIN/220) X 6.3 Vac +or- 1.0. (VIN is the ac voltage of the power outlet.)

Replaceable Parts

6-1. INTRODUCTION

6-2. This section lists the replaceable parts and assemblies of the HP-71 hand-held computer. The reorder number for the HP-71 is 00071-69902.

6-3. Replaceable parts for assembly-level repairs are listed in table 6-1. Additional replaceable parts for component-level repairs are listed in tables 6-2 and 6-3. Part descriptions, HP part numbers, quantities, and reference desigations are included in the tables.

6-4. The HP-71 is illustrated in figure 6-1.

6-5. Component-location diagrams are shown in figures 7-1 and 7-2.

6-6. ORDERING INFORMATION

6-7. To order replacement parts or assemblies, address your order or inquiry to the Corporate Parts Center or Parts Center Europe. Specify the following information for each part ordered:

a. Product model and serial number.

b. HP part number.

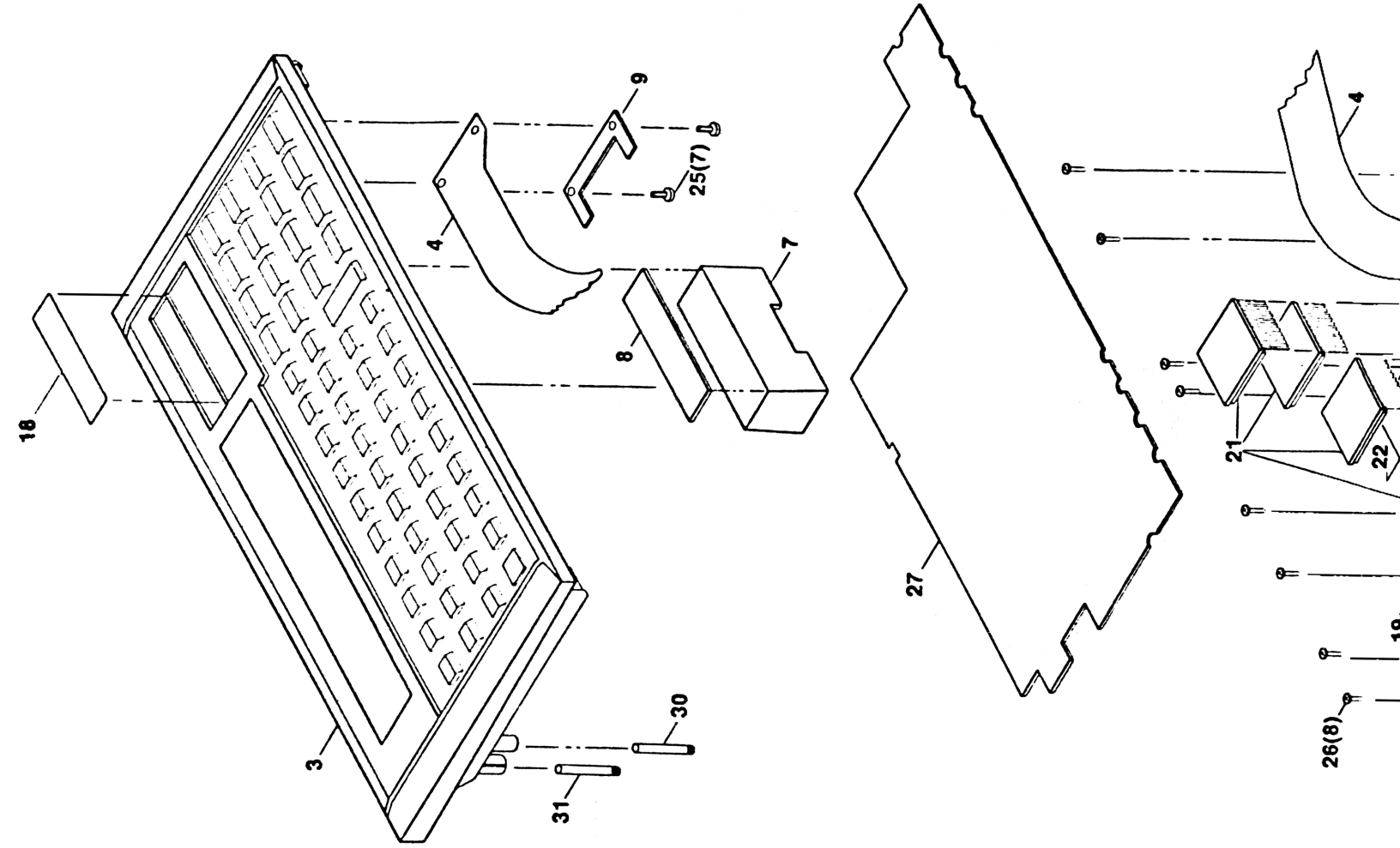
c. Part description.

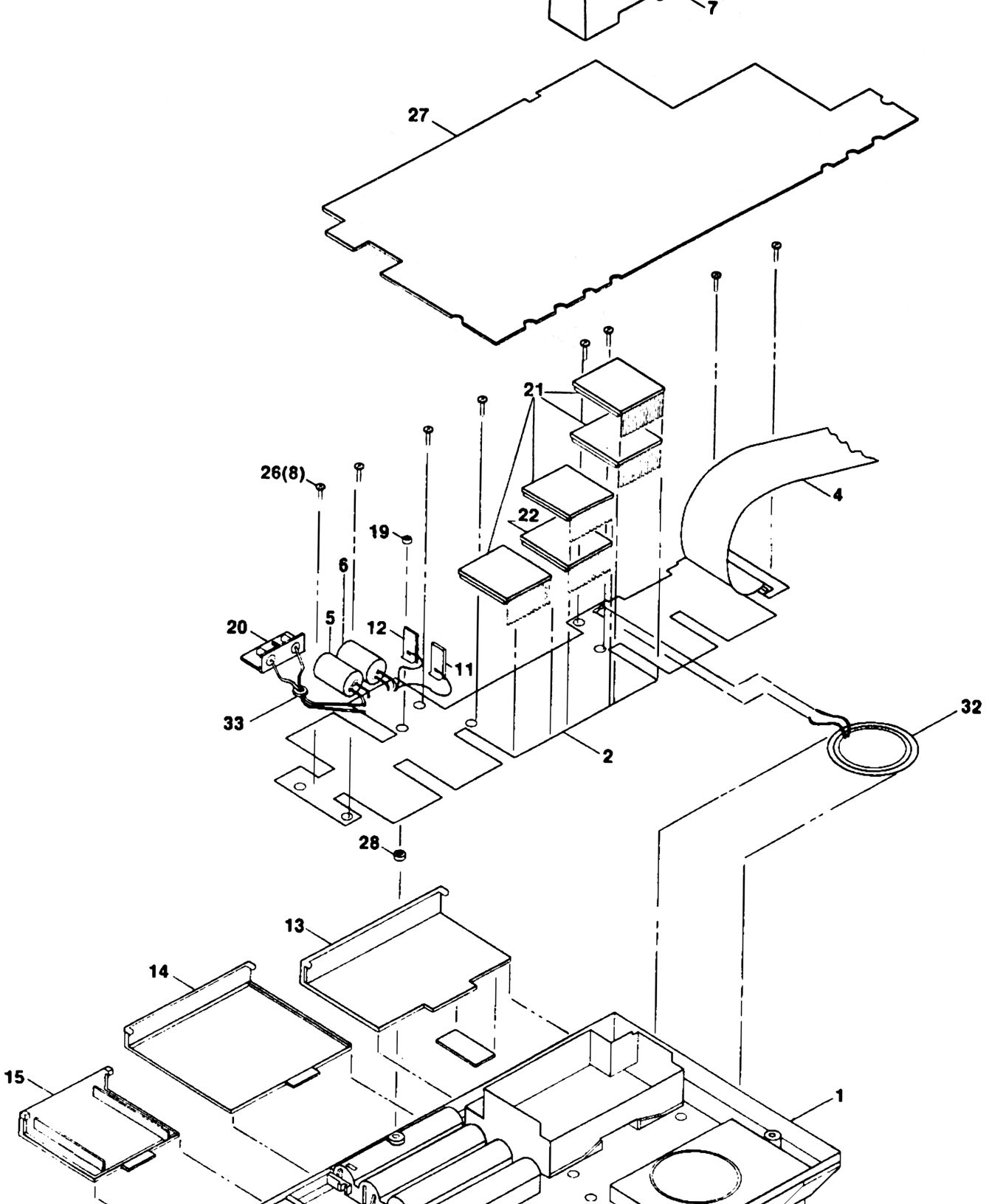
d. Complete reference designator.

Table 6-1. HP-71 Replaceable Parts

INDEX NUMBER, FIGURE 6-1.	HP PART NUMBER		DESCRIPTION	QUANTITY
1	00071-60905		ASSEMBLY. bottom-case	1
2	00071-80002		ASSEMBLY, I/O printed-circuit	1
3	00071-60906	*	ASSEMBLY, top-case	1
4	00071-80003		CABLE, flex	1
5	0180-3352		CAPACITOR, 330 uF, 16V, 20%	1
6	0180-3351		CAPACITOR, 470 uF, 10V, 20%	1
7	00071-40007		CARD READER, blank	1
8	00071-00002		CARD READER, blank, cover	1
9	00071-40016		CLAMP, strain relief	1
10	00071-00006		CONTACT, battery bridge	1
11	00071-60008		CONTACT, battery, negative	1
12	00071-60007		CONTACT, battery, positive	1
13	00071-40003		DOOR, card reader	1
14	00071-40004		DOOR, battery	1
15	00071-40005		DOOR, HP-IL	1
16	00071-40006		DOOR, module	4
17	0403-0279		FOOT	4
18	00071-20003		NAMEPLATE	1
19	0608-0005		NUT, hex, 5/64 inch	1
20	00071-60006		PLATE, adapter pin	1
21	5061-5265	*	RAM, hybrid, 4-int	4
22	5061-5266	*	ROM, hybrid, 4-int	1
23	0516-0098		SCREW, 1/8 inch	2
24	0516-0099		SCREW, 1/4 inch	1
25	0624-0570		SCREW, 0-42, 0.125 inch	7
26	0624-0599		SCREW, self-tapping, 2-28	8
27	00071-20005		SHIELD, ESD, keyboard	1
28	00071-20008		SPACER	1
29	00071-20004		SPRING, battery	2
30	00071-20006		STANDOFF, 0.805 inch	1
31	00071-20007		STANDOFF, 0.873 inch	1
32	0960-0509		TRANSDUCER, piezo	1
33	00071-80016		TRANSFORMER, ac	1

* - This part requires ESD protection.


18
3
4
9
25(7)
8
7
30
31
27
4
21
22
26(8)


7
27
21
26(8)
4
22
19
6
5
12
20
11
33
32
2
28
13
14
15
1

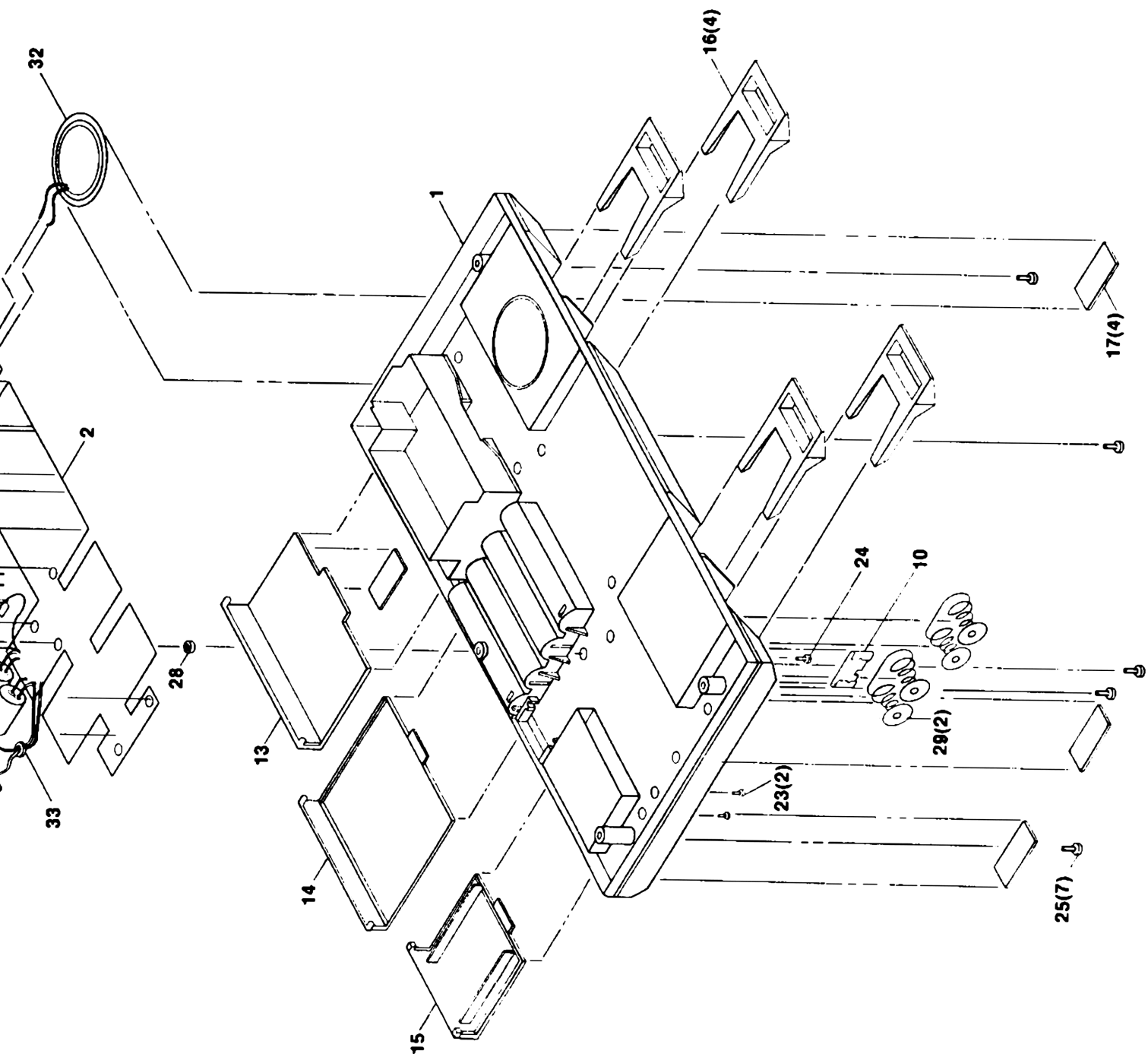


Figure 6-1. HP-71 HHC Exploded View

Table 6-2. Top-Case Assembly Replaceable Parts

INDEX NUMBER, FIGURE 7-1	HP PART NUMBER	DESCRIPTION	QUANTITY
C4,C5	0160-5789	CAPACITOR, 33 pF, 50V, 5%	2
C6,C7	0160-5790	CAPACITOR, 0.1 uF, 25V, 20%	2
C9,C10	0160-5787	CAPACITOR, 1000 pF, 5V, 20%	2
C11,C14	0160-5788	CAPACITOR, 220 pF, ±5%	2
L1	9140-0802	INDUCTOR, 180 uH, 5%	1
R20,R21	0699-1141	RESISTOR, 10K, 5%, 1/8W	2
Y1	0410-1381	CRYSTAL, quartz	1

Table 6-3. I/O Assembly Replaceable Parts

INDEX NUMBER, FIGURE 7-2	HP PART NUMBER	DESCRIPTION	QUANTITY
C1	0180-3351	CAPACITOR, 470 uF, 10V, 20%	1
C2	0180-3352	CAPACITOR, 330 uF, 16V, 20%	1
C8	0160-0576	CAPACITOR, 0.1 uF, 50V, 20%	1
C12	0160-3879	CAPACITOR, 0.01 uF, 20%	1
C13	0160-4441	CAPACITOR, 0.47 uF, 10%	1
CR2	1901-0999	DIODE, Schottky	1
CR3	1906-0069	DIODE, bridge, full-wave, 400V	1
CR7	1901-0704	RECTIFIER, silicon	4
L2	9140-0794	INDUCTOR, 56 mH, 10%	1
Q1	1854-0932	TRANSISTOR, NPN	1
Q2	1854-0973	TRANSISTOR,	1
R22	0683-3915	RESISTOR, 390 ohms, 5%, 0.25W	1
R23,R24	0683-1035	RESISTOR, 10 K-ohms, 5%, 0.25W	2
VR7	1902-1390	DIODE, Zener	1

SECTION
VII

Reference Diagrams

7-1. This section includes reference diagrams for the HP-71 hand-held computer.

7-2. The component location diagrams for the top-case assembly and the I/O PCA are shown in figures 7-1 and 7-3 respectively. (Replaceable parts are listed in section VI.)

7-3. The schematic diagrams for the top-case assembly and the I/O PCA are shown in figures 7-2 and 7-4 respectively.

7-4. The signal lines to ICs and connectors on the I/O PCA are shown in figure 7-5.

7-5. The signal lines to ICs and connectors on the keyboard PCA are shown in figure 7-6.

7-6. The display driver connections are shown in figure 7-7.

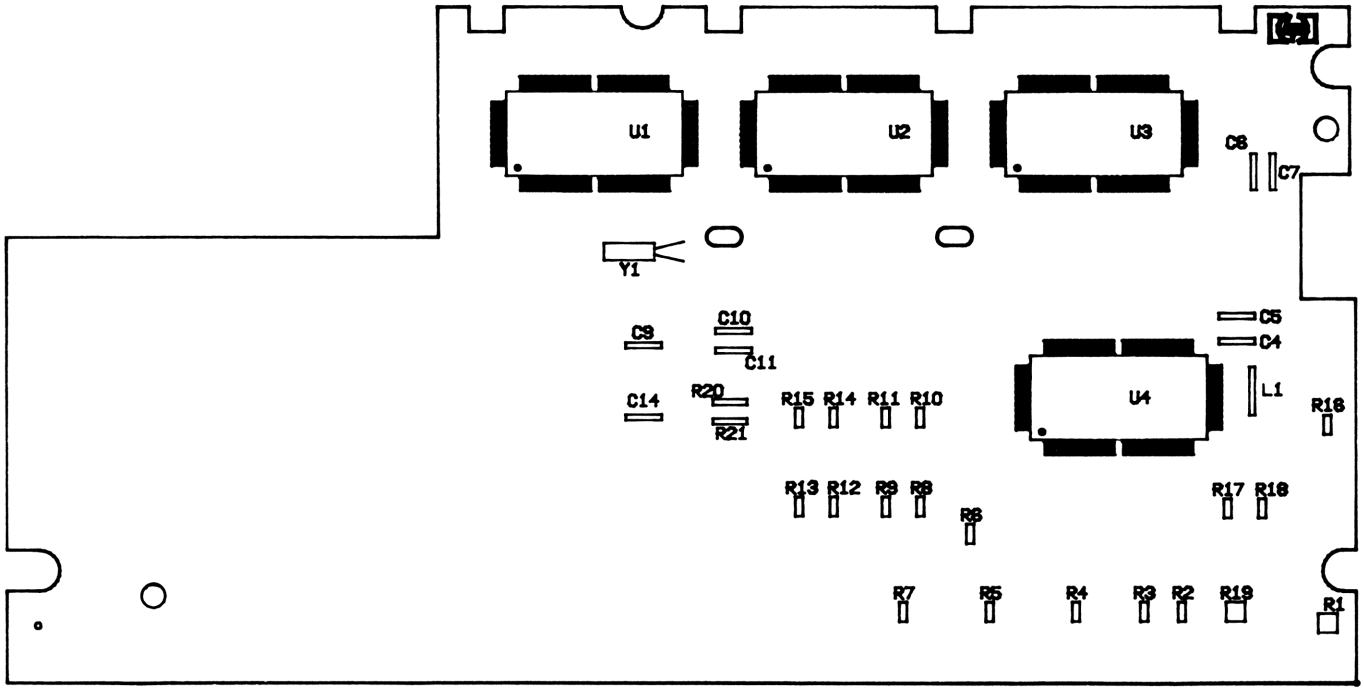
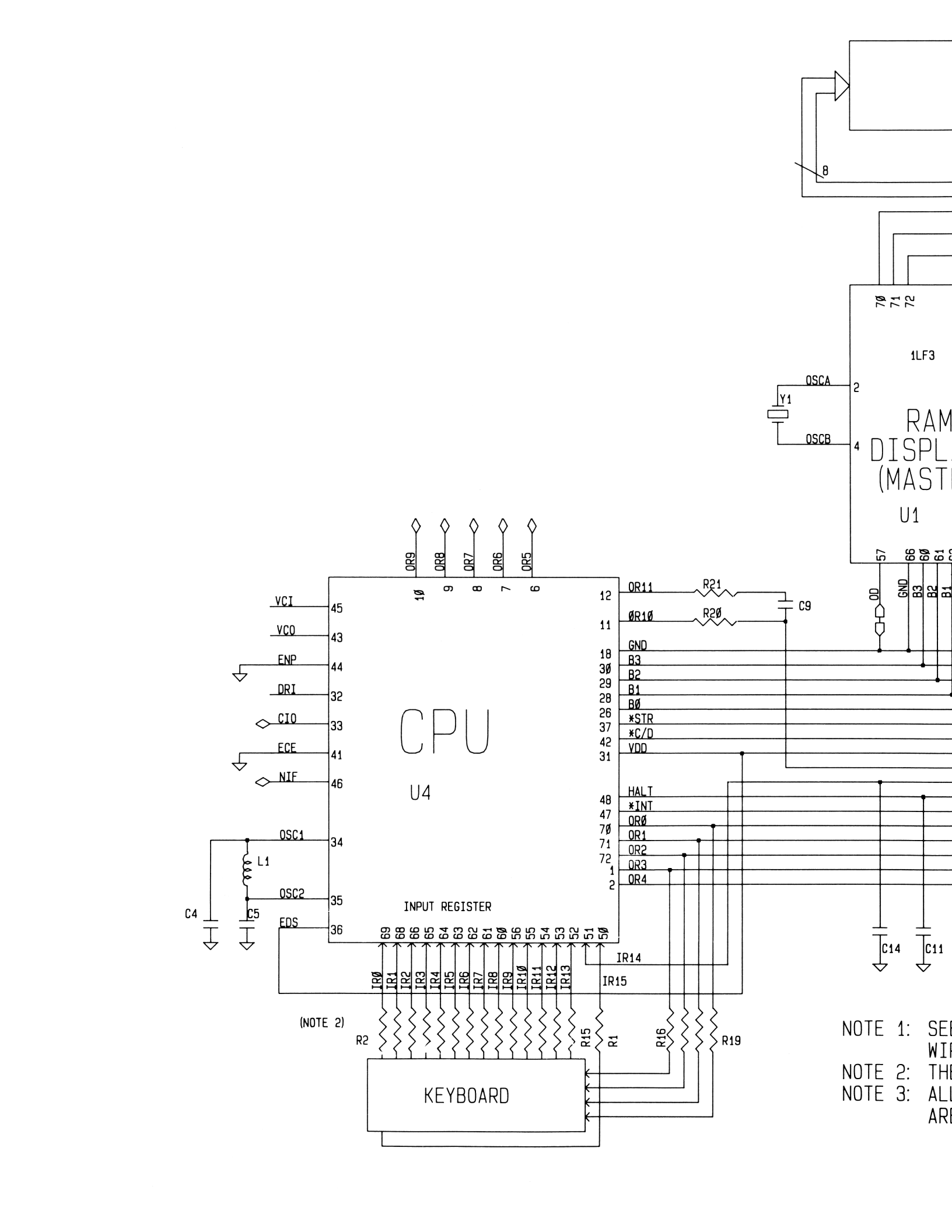
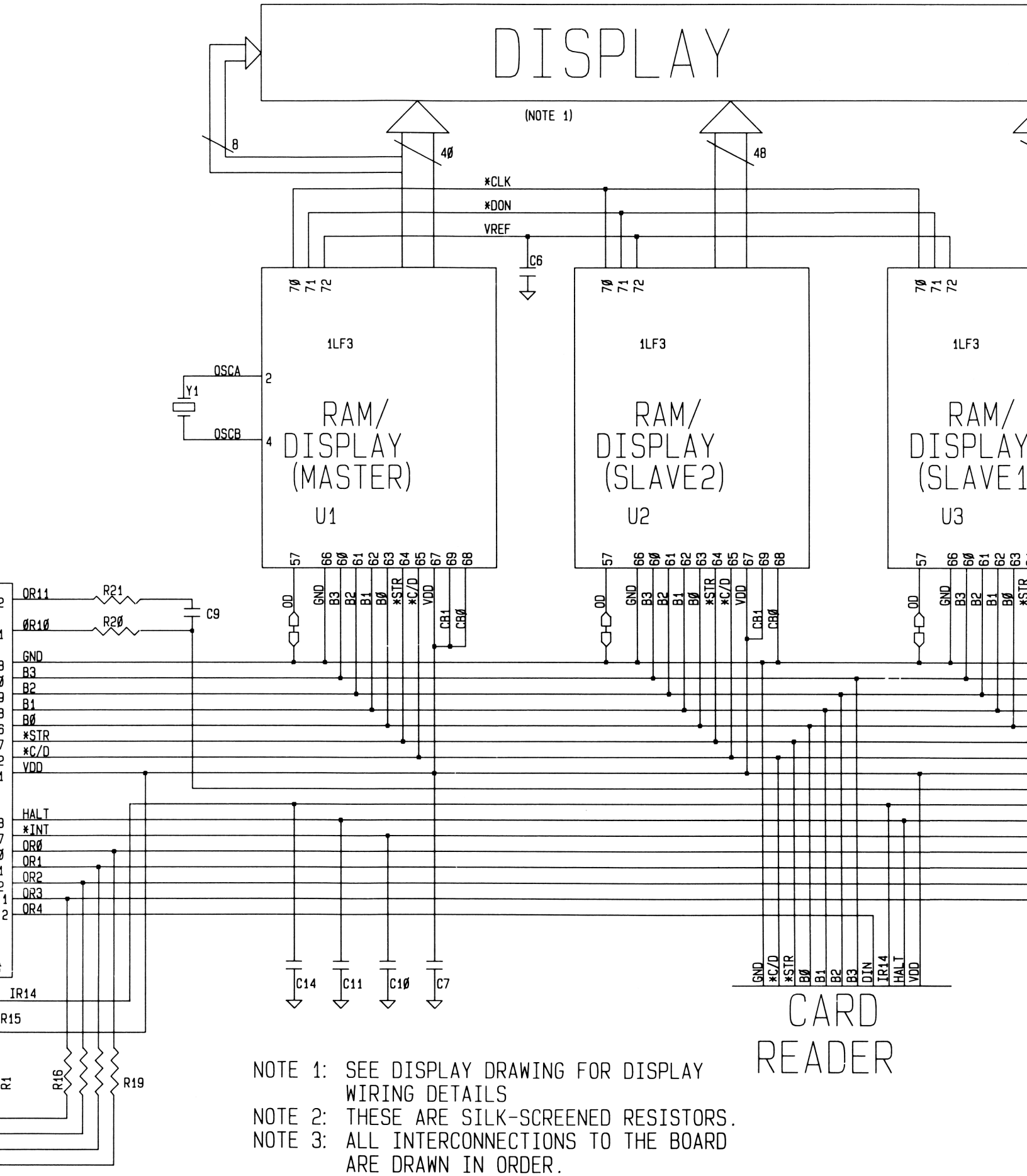


Figure 7-1. Top-case Assembly Component Location Diagram


8
70
71
72
1LF3
OSCA
2
Y1
OSCB
4
RAM
DISPL
(MAST
U1
57
66
60
61
OD
GND
B3
B2
B1
OR9
OR8
OR7
OR6
OR5
10
9
8
7
6
VCI
45
VCO
43
ENP
44
DRI
32
CIO
33
ECE
41
NIF
46
CPU
U4
OSC1
34
L1
OSC2
35
C4
C5
EDS
36
INPUT REGISTER
OR11
12
R21
C9
ØR1Ø
11
R2Ø
GND
18
B3
3Ø
B2
29
B1
28
BØ
26
*STR
37
*C/D
42
VDD
31
HALT
48
*INT
47
OR0
7Ø
OR1
71
OR2
72
OR3
1
OR4
2
C14
C11
69
68
66
65
64
63
62
61
60
56
55
54
53
52
51
5Ø
IR14
IR15
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
IR8
IR9
IR10
IR11
IR12
IR13
(NOTE 2)
R2
R15
R1
R16
R19
KEYBOARD
NOTE 1: SEE
WI
NOTE 2: THE
NOTE 3: ALL
ARE



NOTE 1: SEE DISPLAY DRAWING FOR DISPLAY WIRING DETAILS

NOTE 2: THESE ARE SILK-SCREENED RESISTORS.

NOTE 3: ALL INTERCONNECTIONS TO THE BOARD ARE DRAWN IN ORDER.

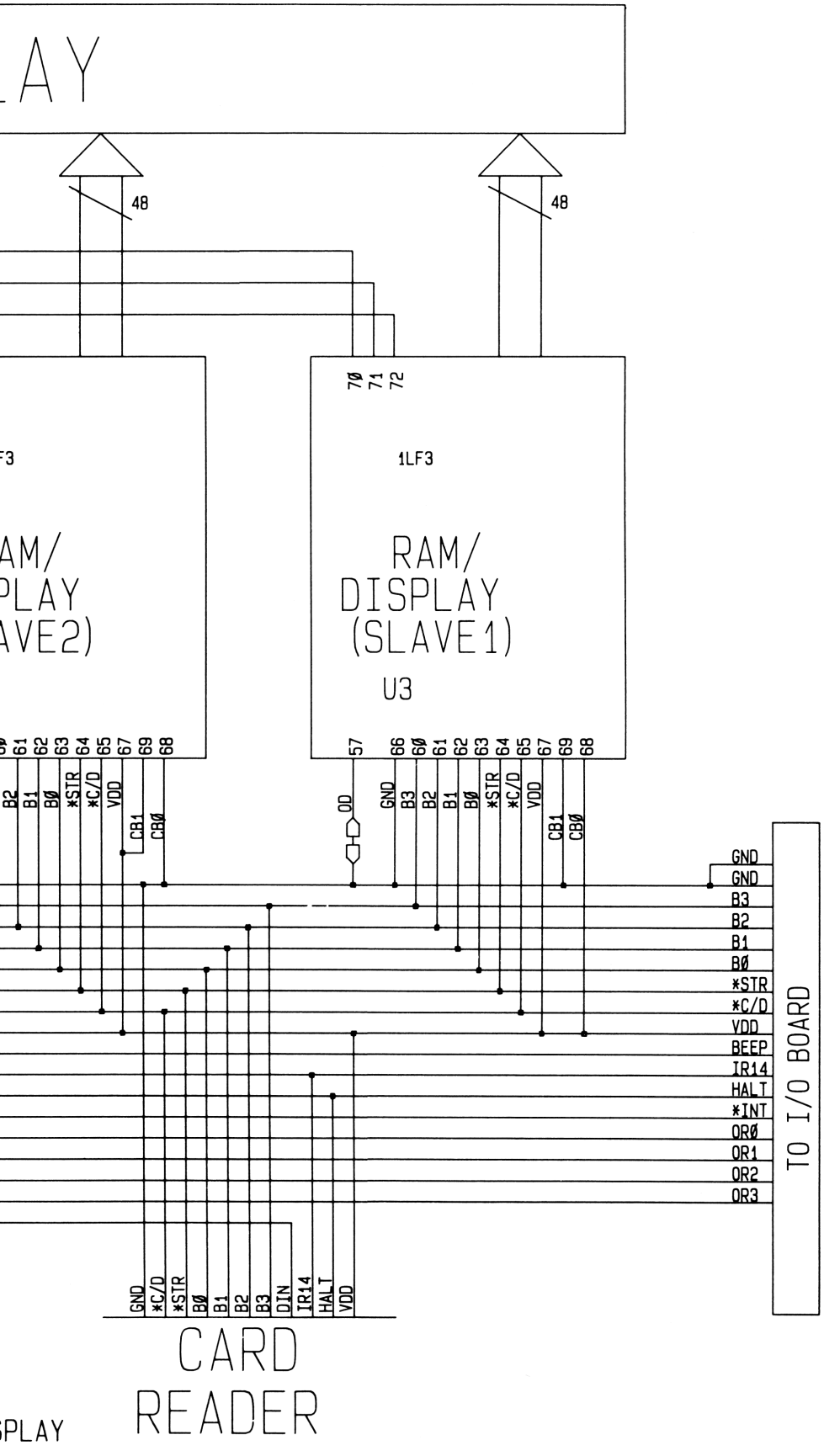


Figure 7-2.
Top-case Assembly Schematic Design

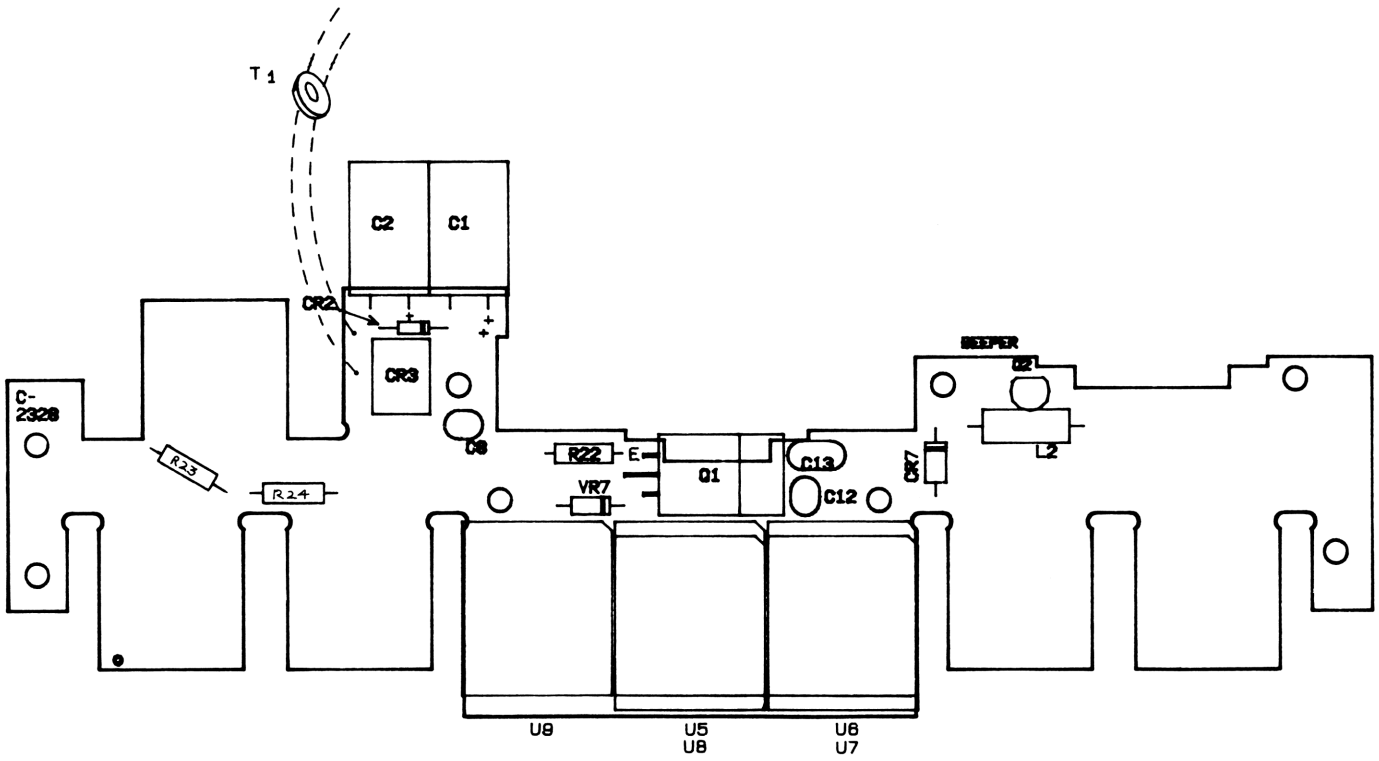
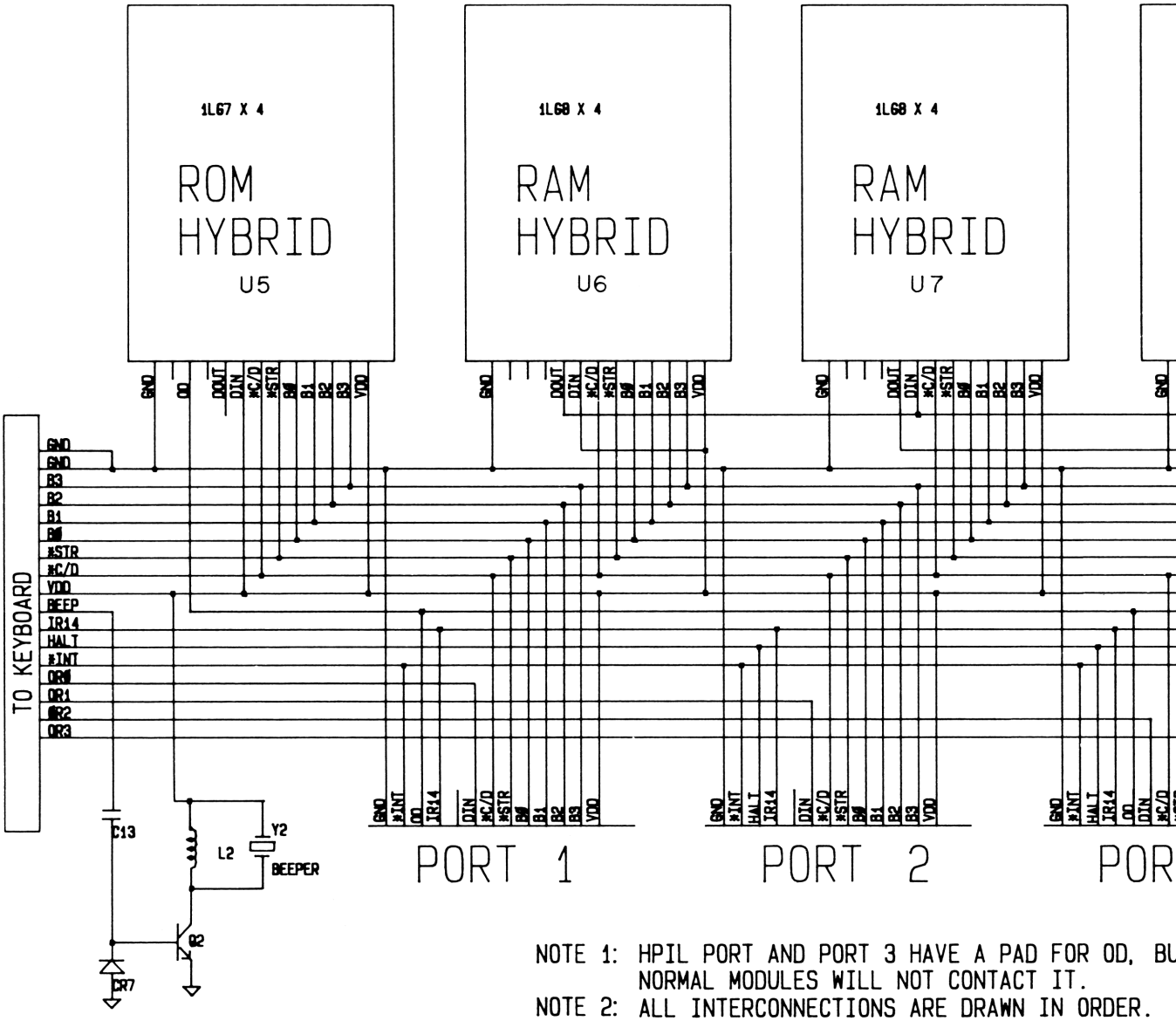
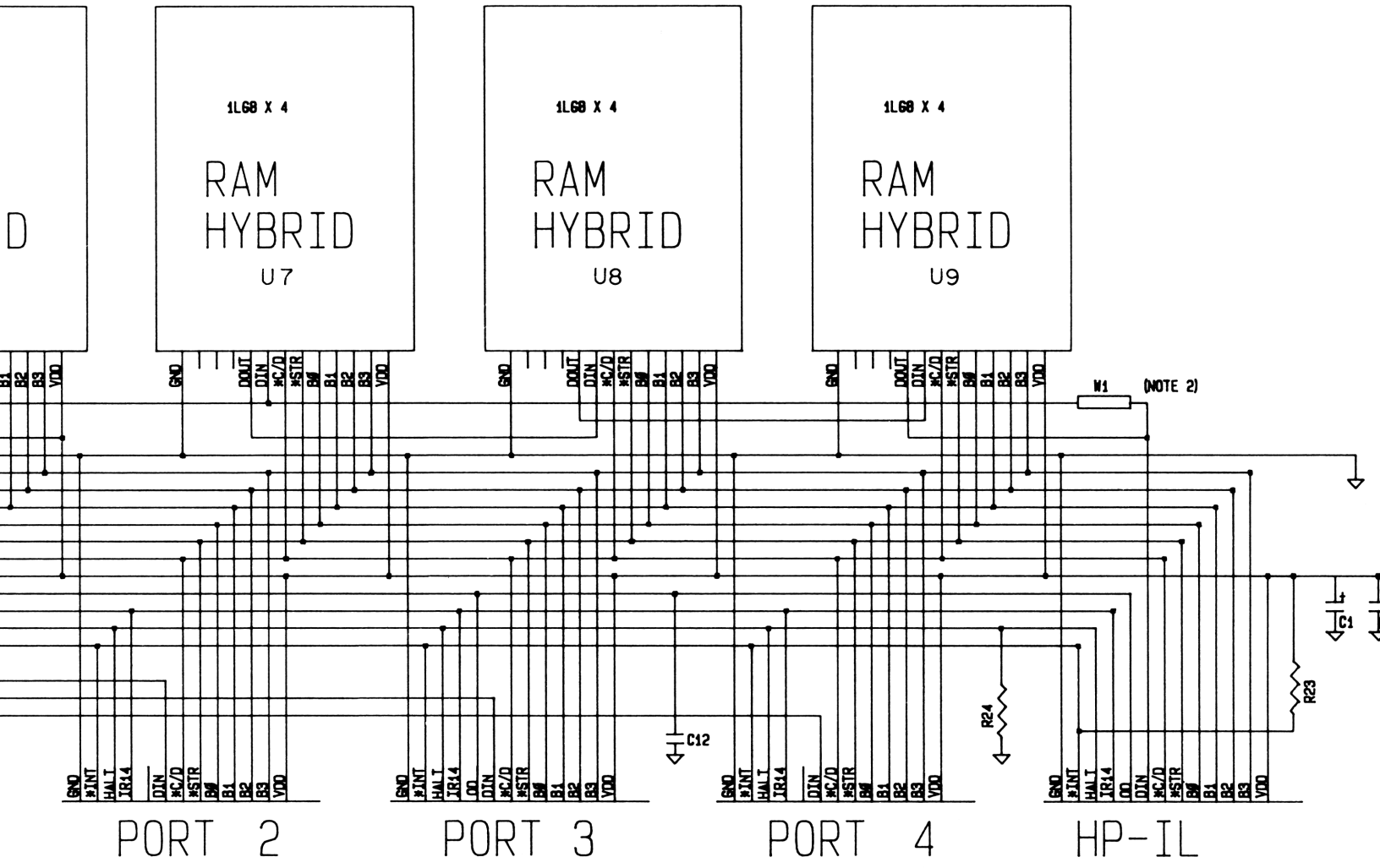


Figure 7-3. I/O PCA Component Location Diagram



NOTE 1: HPIL PORT AND PORT 3 HAVE A PAD FOR OD, BU
NORMAL MODULES WILL NOT CONTACT IT.
NOTE 2: ALL INTERCONNECTIONS ARE DRAWN IN ORDER.



HPIL PORT AND PORT 3 HAVE A PAD FOR OD, BUT
NORMAL MODULES WILL NOT CONTACT IT.
ALL INTERCONNECTIONS ARE DRAWN IN ORDER.

PULL *INT TO GND
TO INTERRUPT

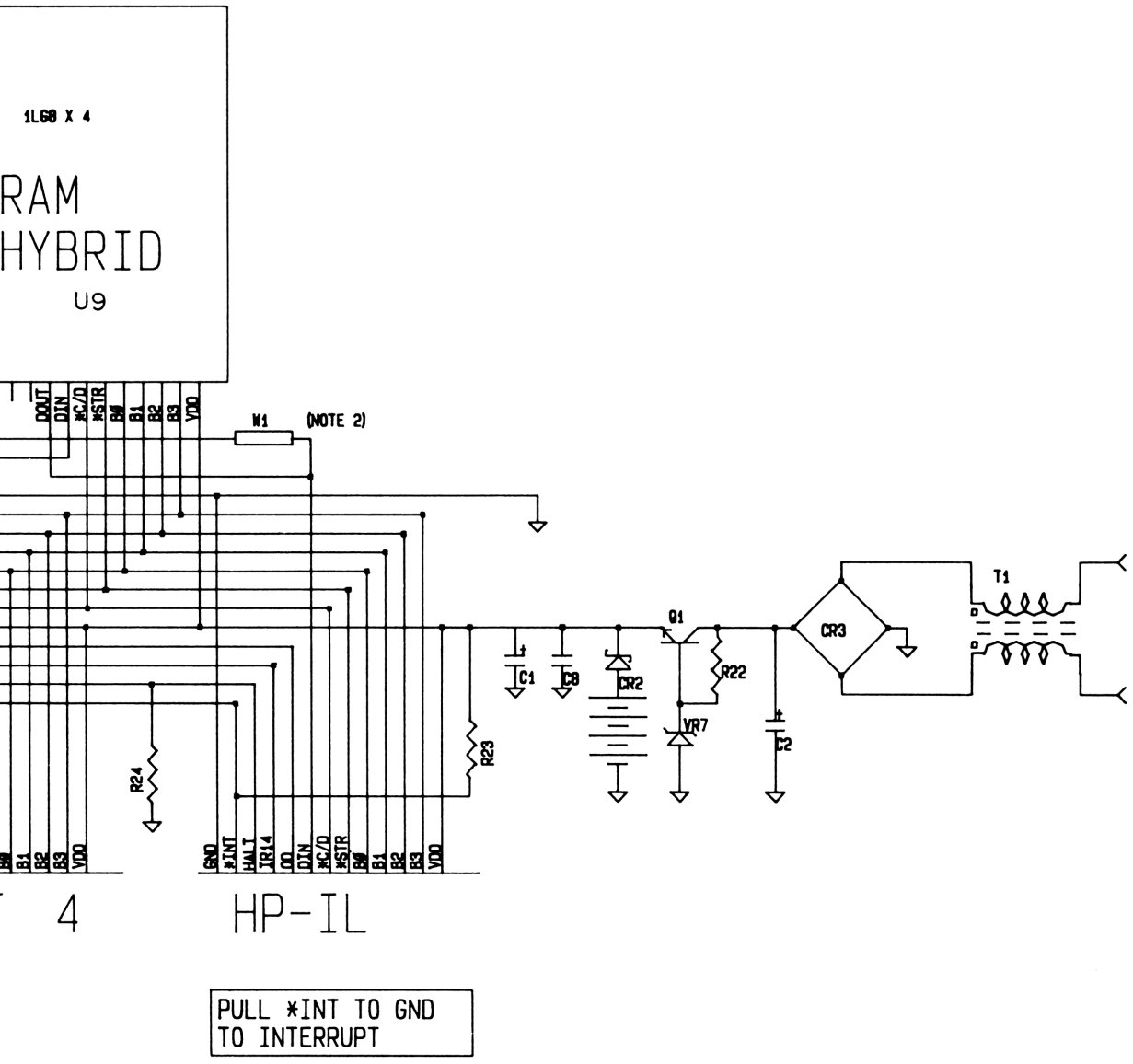


Figure 7-4. I/O PCA Schematic Diagram

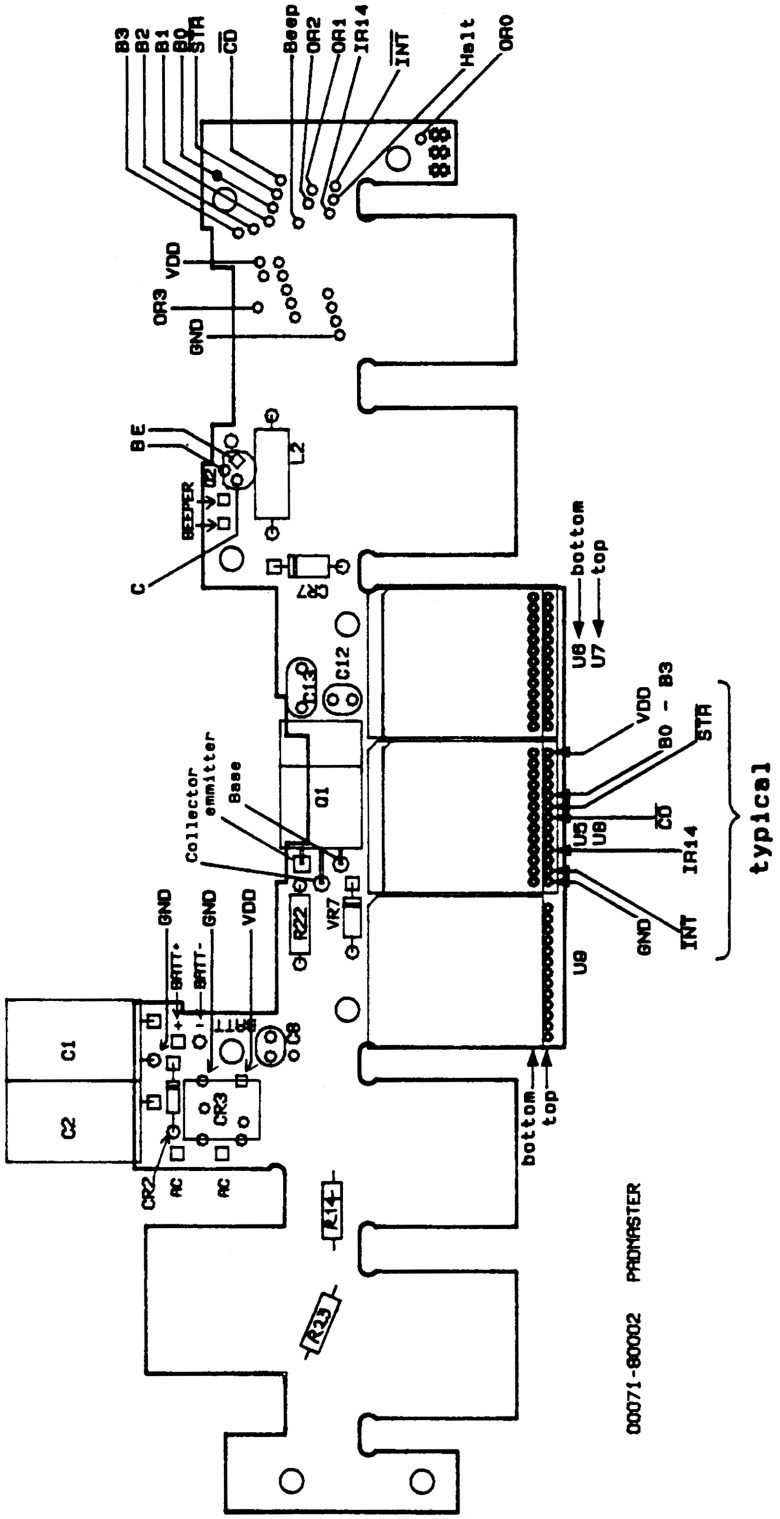


Figure 7-5. I/O PCA Signal Diagram

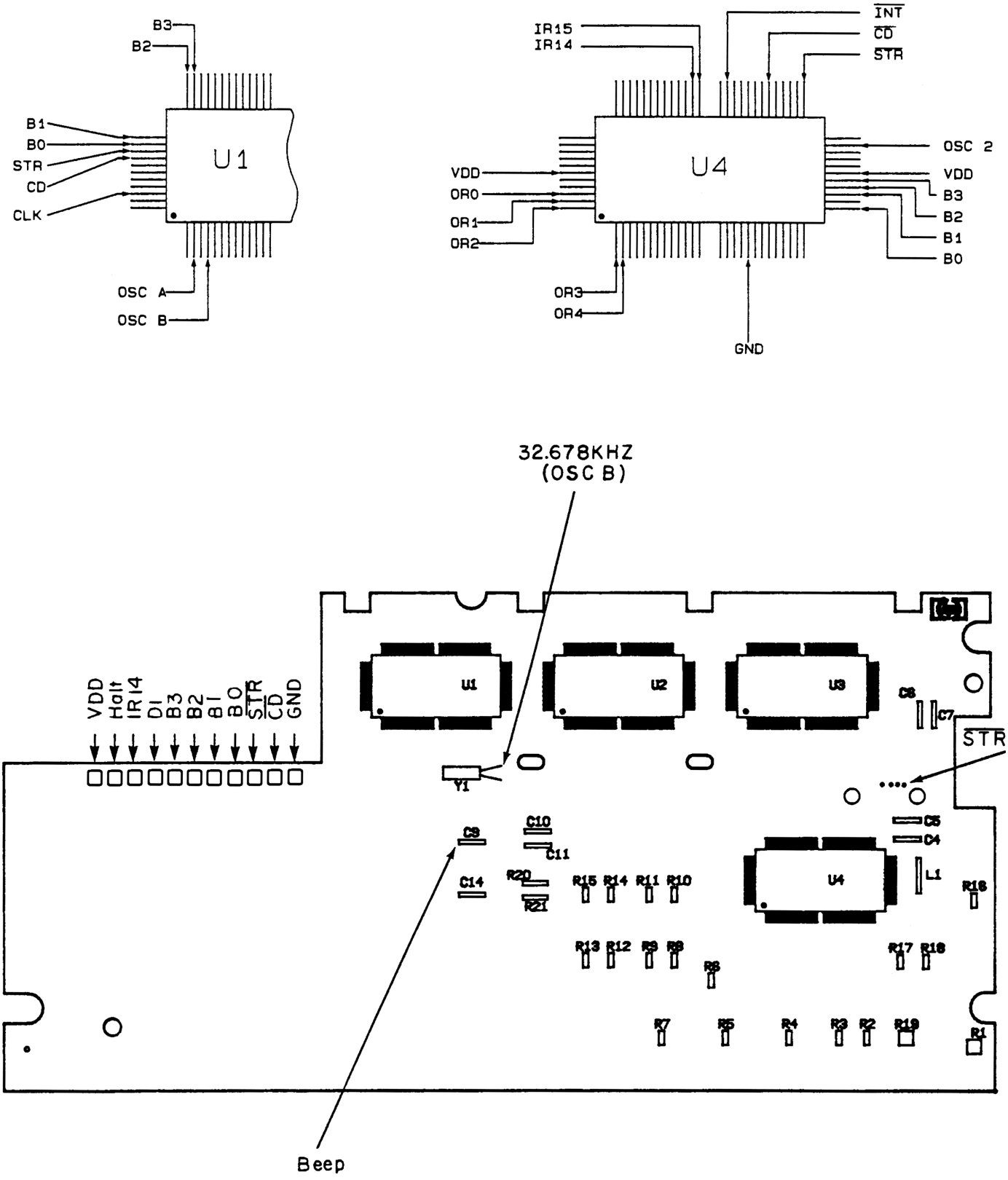


Figure 7-6. Keyboard Signal Diagram

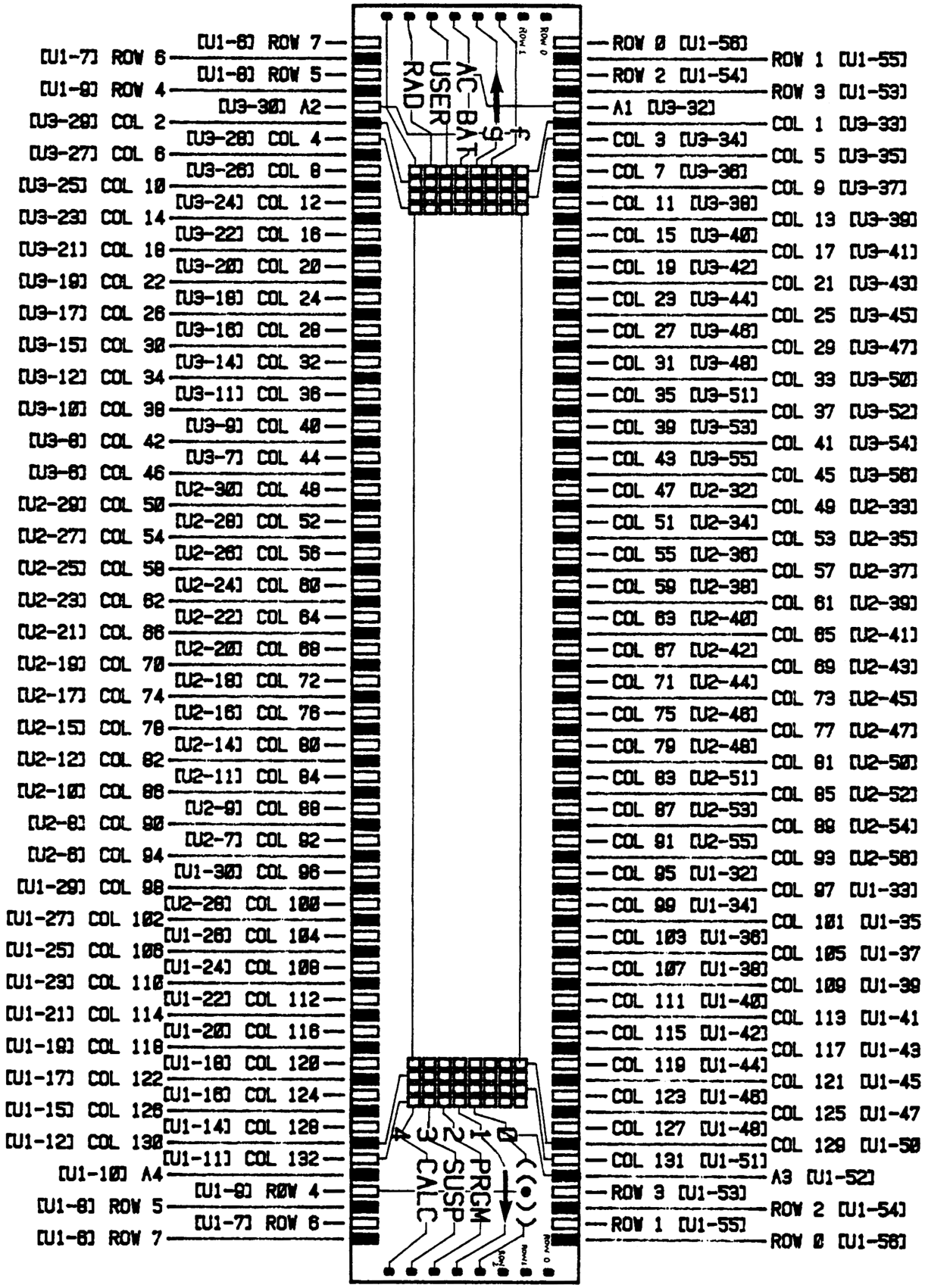


Figure 7-7. Display Driver Connections

APPENDIX
A

Diagnostic ROM

A-1. INTRODUCTION

A-2. This appendix describes the features of the diagnostic ROM and the way it tests the HP-71. You should read this section to familiarize yourself with the ROM.

A-3. The diagnostic ROM is used as part of the testing procedures in section IV. However, section IV uses only the multiple test feature of the ROM. Depending on what testing you need to do, you may find some other features of the ROM useful. For example, you may need to do a burn-in on a unit that came in for repair. In that case, the auto test feature should be used. Paragraph A-62 covers the built-in mainframe ROM test which is not a part of the diagnostic ROM.

A-4. DESCRIPTION OF THE DIAGNOSTIC ROM

A-5. The diagnostic ROM is a preprogrammed ROM (read only memory) module designed to be inserted into port number one (the left front port) of the HP-71. It is designed to take control of the HP-71 by disabling the system ROM. It will detect most hardware failures by exercising all of the ICs and the bus. It can not, however, determine if software is operating properly except when certain software responses are expected in a particular test and are not received.

A-6. In order to use the diagnostic ROM, the following kernel of hardware must be in operating condition: the timer on the master display/RAM IC (U1), the system bus, a portion of the CPU, and a number of discrete components connected to the CPU that regulate the system clock. In addition, address 2FD04 (hexadecimal) in IC U1 must be available. If the particular portion of the CPU or any of the discrete components are not working, the HP-71 either will not turn on or will behave erratically. If the timer, or the bus are not working, or the RAM location is not available, the HP-71 will complete the CPU test but will attempt to display a fail code. In this case, other tests are used to pinpoint the source of the problem. (For certain types of bus failure, the CPU test is not completed.)

A-7. After the initial kernel of hardware has been tested, the diagnostic ROM proceeds to test the other components in the HP-71. When the test of a good component is completed, "<test> OK" is displayed and a high-pitched beep is sounded. If the component is not good, an error message is displayed and a low pitched warble is sounded. Thus, if the display is not working when the diagnostic ROM is first turned on, you can tell if the diagnostic ROM is working by listening for the beeps.

A-8. The diagnostic ROM reassigns the keyboard when it comes on. Before using the diagnostic ROM, acquaint yourself with the key assignments as shown in table A-1.

A-9. Once a test has been run individually, during the multiple test, or during the auto test, the outcome of the test(s) will be maintained in a status table. The table can be cleared by turning the HP-71 off and back on again (except when executing the deep sleep test). To access the status of tests already performed press [A] and then [C].

Table A-1. Key Assignments

Key	Test or Function
[ON]	ON/Off
[H]	Test Directory (Help List)
[A]	Auto Repeat Testing
[A] then [C]	Test Status Listing
[B]	Battery Indicator Check
[M]	Directed Multiple Testing
[0]	Self-Check Rom Test
[1]	CPU Test
[2]	Mainframe RAM Test
[3]	Plug-in ROM Test
[4]	Plug-in RAM Test (soft configured)
[5]	Display Test
[6]*	Keyboard Test
[7]*	Key-Bounce Test
[8]*	Sleep Test
[9]*	Electrostatic Discharge (ESD) Test
[*]	Card Reader Test
[/]	HPIL Module Test
* Will not execute in 'AUTO' mode.	

A-10. Troubleshooting with the diagnostic ROM

A-11. When using the diagnostic ROM, be sure you do the following:

a. Make sure the computer is off by pressing [f][ON] before you insert the ROM.

b. Insert the diagnostic ROM into port one (the left front port).

c. Press [ON] to turn on the HP-71 (it may be necessary to press [ON] more than once). When the computer turns on, the ROM will automatically take control of the CPU. The diagnostic ROM automatically runs the CPU test when it comes on. If the test is passed, then you will be asked to select a test. Refer to paragraph A-29 for an explanation of the CPU test.

d. The test you will use to troubleshoot the HP-71 in section IV is the multiple test. In addition to this test, you can run the auto test or run individual tests for special purposes.

e. After you have completed the diagnostic ROM tests, press the [ON] key to turn the HP-71 off. Then remove the ROM.

A-12. DIAGNOSTIC ROM GROUP TESTS

A-13. There are two group tests that can be run by the diagnostic ROM. They are:

- The directed multiple test (requires manual input for some tests).
- The auto test (self running loop).

Each test is made up of various individual tests that are run in a specified order for maximum error checking. Descriptions of the individual tests start in paragraph A-25.

A-14. Directed Multiple Test

A-15. This is the test used in section IV to troubleshoot the HP-71.

A-16. The multiple test automatically runs most of the diagnostic tests. Certain tests require operator input. When the HP-71 runs one of these tests, it will prompt you by displaying a message indicating the type of input it is looking for.

A-17. To interrupt the testing cycle, press any key except [ON] between the tests. The HP-71 will again prompt with 'SELECT TEST', and the status of the completed tests will not be changed. If the [ON] key is used to interrupt the multiple test, the HP-71 will turn off, and the status of the completed tests will be lost.

A-18. The following tests are run during the multiple test:

- CPU test.
- Mainframe RAM test.
- Plug-in ROM test.
- Plug-in RAM test.
- Display test.
- Keyboard tests.
- Key-bounce test.
- Sleep test.

A-19. As the tests are run, messages are displayed. The first message for a given test names the test being run. Then the results of the tests are given; either "OK" or an error message is displayed.

A-20. Some tests are made up of several subtests. The result of each subtest is reported after it is run.

A-21. Auto Mode

A-22. The auto test is designed to run an individual test or a series of tests repeatedly. You enter auto mode by pressing the [A] key. After you press [A], "(AUTO) SELECT" will be displayed. You can then select either an individual test or the multiple test. If you select an individual test, it will be run until you tell it to stop by pressing any key except [ON]. If you select the multiple test by pressing the [M] key, the following tests will be run repeatedly:

- CPU test.
- Mainframe RAM test.
- Plug-in ROM test.
- Plug-in RAM test.
- Display test (display RAM only).
- 10 Second Electrostatic Discharge (ESD) Test

A-23. You can stop any auto test and still retain the status of the tests by pressing any key except [ON] between test cycles. If the [ON] key is pressed, the HP-71 will turn off, and the status of the tests will not be saved. To interrupt the ESD test, hold any key except [ON] down until 'KEY DOWN: X-X' is displayed. ESD test errors do not effect the operation of the HP-71.

A-24. The status of any test run in or out of auto mode can be determined by pressing the [C] key while in auto mode.

A-25. INDIVIDUAL TESTS

A-26. This section describes what each test does. The tests can be run separately when initiated from the keyboard. Many of these tests are run as part of one or both of the group tests.

A-27. Self Check (S/C) Diagnostic ROM Test

A-28. The S/C ROM Test performs a checksum test on the contents of the diagnostic ROM. This test can be executed by pressing the [0] key. If the ROM tests good, 'ROM OK #1' is displayed; if the ROM tests bad, 'ROM BAD #1' is displayed. This test should be run as a routine procedure. A bad diagnostic ROM leads to errors in troubleshooting.

A-29. CPU Test

A-30. The CPU test attempts to run the entire CPU instruction set. If some part of the instruction set does not work, the message "CPU BAD nnnn" is displayed, where n is the error code (n=B,C,D,E,F, or 0-9). The error code indicates the type of error. Refer to table 5-6 Diagnostic ROM Error Messages for an explanation of the messages.

A-31. With the diagnostic ROM installed, the CPU test is run automatically when the HP-71 is first turned on. It can also be run from the keyboard by pressing the [1] key.

A-32. M/F (MainFrame) RAM Test

A-33. The mainframe RAM test performs a write and a read to the RAM on the display driver chips (U1,U2,U3). If what is read back from RAM does not match what was written, an error message is displayed. If the RAM passes this test "OK" is displayed.

A-34. The mainframe RAM test can be run by either running the multiple test or by pressing the [2] key.

A-35. P/I (Plug-In) ROM Test

A-36. The plug-in ROM test performs a checksum on all ROMs plugged into the HP-71, including the ROM in the HP-IL module. The test can be run by pressing the [3] key or the [M] key. As each ROM is tested, the port and device number and ROM size are displayed.

A-37. P/I (Plug-In) RAM Test

A-38. The plug-in RAM test is functionally identical to the mainframe RAM test. However, it performs the write, read, and compare operations on RAM located on the I/O Board (U6,U7,U8,U9) and any RAM modules that might be present. "Plug-IN RAM" refers to any soft configured RAM. As each RAM is tested, the port and device number and RAM size are displayed.

A-39. The plug-in RAM test can be run by pressing the [4] key or by running the directed multiple test by pressing the [M] key.

A-40. Display Test

A-41. The display test runs through four phases (if run in auto test, only phases 1 and 2 are completed):

Phase 1. Check timers.

Phase 2. Display a sequence of 3 checkerboard patterns. This is a visual test. First, all the dots in the dot matrix will turn on along with the annunciators. Then three checkerboard patterns will be displayed. During this time, watch the display for any missing or added dots, rows, columns, or annunciators. Pressing any key freezes the current pattern.

Phase 3. Scroll characters from right to left. As the characters scroll across the screen, watch for missing or added dots, columns, and rows. Any key pressed in the top row, second row, third row, and bottom row (except the [+] key) slows the scroll to 1/2, 1/4, 1/8, 1/16 speed, respectively. The [+] key aborts the scroll.

Phase 4. Keyboard directed check of the dot matrix. During this phase, pressing any key in the top row of keys causes an X-checkerboard pattern to be displayed. The pattern rolls up in the display until the key is released. Keys in the other three rows each turn on four display columns, or three columns and an annunciator. When a key is held down, the even bits in a column are turned on. When the key is released the odd bits turn on. The [+] key, when held down, rolls the annunciators and ends the test when released. This is a visual test. It should be used as a backup for the other tests.

A-42. Pressing the [+] key at any time will abort the display test.

A-43. The display test can be run by pressing the [5] key or as part of the directed multiple test.

A-44. Keyboard Test

A-45. The keyboard test requires the operator to press the keys in order starting with the [Q] in the upper left-hand corner and proceeding across the keyboard to the right. Then start at the left of the next row of keys down, and proceed across the keyboard to the right. Each key is displayed by a row-column location designator. For example, the [Q] key location is "1-0" (first row, key 0). Any key may be pressed more than once. The display will indicate this occurrence with "1-0*" (for the [Q] key). A "piano stroke" in which the next key is pressed before the first key is released may be used in this test except when passing over the [END LINE] key in the bottom row. It must be pressed separately. If an error occurs, the test may be resumed by pressing any key twice except the [ON] key which would turn the HP-71 off.

A-46. The keyboard test can be run by pressing the [6] key or as part of the

directed multiple test by pressing the [M] key. Pressing the [+] key and holding it down for two seconds aborts this test.

A-47. Keybounce Test

A-48. The keybounce test is run the same way the keyboard test is run with the exception that a "piano stroke" cannot be used. When a key is pressed, a code is displayed. In the case of the [M] key, "3-6: 0/2" could be displayed. This indicates that the [M] key was pressed and there was 0 milliseconds of downbounce and 2 milliseconds of up bounce. Neither of these numbers should be greater than 15 milliseconds. These numbers will aid in determining if a marginal key is present. If a key is entering multiple characters, the message "DBL ENTR" will be displayed. If keys are pressed too quickly, the message "TOO FAST" is displayed, and "DOUBLE KEY" is displayed if two keys are pressed at the same time.

A-49. This test can be run from the keyboard by pressing the [7] key or as part of the directed multiple test. It can be aborted by pressing the [+] key and holding it down for two seconds.

A-50. Sleep Test

A-51. The sleep test tests the HP-71's ability to enter and exit deep sleep. As soon as the test is run, the HP-71 goes into light sleep. At this point, any key except the [ON] key will wake it up to perform the RAM test and a CPU test, after which it goes back into light sleep. Pressing the [ON] key sends the HP-71 into deep sleep after testing the ability of the timers to wake up the CPU. Only the [ON] key can then wake it up. The HP-71 then performs the CPU test. At no time during this test is the status of any test lost.

A-52. Pressing the [8] key will start the sleep test. There are two ways to abort this test:

1. After the HP-71 has been awakened from light sleep, by pressing the [+] key during reporting.

2. Pressing the [ON] key twice in response to the "ON=DP SLEEP" message exits this test by beginning the CPU test.

A-53. Battery Indicator Test

A-54. The battery indicator test reads the display timer control nibble to determine the battery voltage level. Bit 3 in the control nibble is set when the battery voltage level is between 4.3 and 4.5 Vdc. When bit 3 is set and the diagnostic ROM is in use, "BATT:LOW" will be displayed. When the battery voltage drops 0.8 to 1.2 Vdc below the bit 3 set point (4.3 to 4.5 Vdc), bit 2 is set. When bit 2 is set "BATT:LOW VLW" will be displayed. At no time should bit 2 be set when bit 3 is clear. When neither bit is set "BATT: NONE" will be displayed.

A-55. When this test is run in auto mode the low battery indicator is

continously tested. As the batteries discharge (or power supply voltage is lowered) the display should change from "BATT: NONE" to "BATT:LOW" when the bit 2 set point is reached.

A-56. Pressing the [B] key will start this test; pressing the [+] key and holding it down for two seconds will abort the test.

A-57. Card Reader Test - see Section V, Accesories

A-58. HP-IL Test - see Section V, Accessories

A-59. Help List

A-60. The help list is a listing of all of the tests contained in the diagnostic ROM. It shows what is available in the current mode (auto or manual). Pressing any key except the [+] key will slow the speed of the listing.

A-61. Pressing the [H] will display the listing; pressing the [+] key will abort the listing at any time.

A-62. System ROM Test

A-63. The diagnostic ROM disables the system ROM; therefore, it cannot be used to test the system ROM. A self test routine is built into the system ROM. The diagnostic ROM must be removed before running this test.

A-64. The system ROM self test can be run by doing the following: press the [ON] and the [/] keys at the same time. "INIT:1" will be displayed. Then press [2] and [ENDLINE] at the same time.

A-65. The test then performs a checksum test on the system ROM. "ROM TEST 1G 2G 3G 4G, displayed after a few moments, indicates the ROM is good. If any number in the display is followed by the letter B, the system ROM is bad.