HP-75
PORTABLE COMPUTER

SERVICE MANUAL

HEWLETT PACKARD

HP-75

Portable Computer

SERVICE MANUAL

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General Information

1-1. INTRODUCTION

1-2. This service manual contains information to help you troubleshoot and repair the HP-75C Portable Computer.

Note: This manual will use HP-75 to designate the HP-75C.

1-3. This section describes the HP-75 and outlines how to use this manual.

1-4. The remainder of this manual is divided into 7 sections:

- o A description of the HP-75 and how it operates (section II).
- o Assembly/disassembly procedures (section III).
- o A description of the diagnostic ROM (section IV).
- o Troubleshooting procedures (section V).
- o Accessories (Section VI).
- o Lists of replaceable parts (section VII).
- o Reference diagrams (section VIII).

1-5. Before using this manual in actual repair, read through sections I and II to become familiar with the HP-75 and its operation. Then read sections III through V to become familiar with the repair proceedures.

1-6. Additional information related to service is included in the HP-75 Owner's Manual:

- o Section 8, Card Reader Operations, detail the use of the card reader.
- o Appendix A lists the power cords and other accessories used with the HP-75.
- o Appendix B explains the use and installation of the plug-in ROM modules and the memory module.

1-7. PRODUCT DESCRIPTION

1-8. The HP-75 Portable Computer is an integrated system which features:

- Three operating modes:
  - Edit mode consisting of both enhanced ANSI BASIC programming language and text writing.
  - Time mode.
  - Appointment mode.
- 16K read/write memory, expandable to 24K.
- Battery-powered circuitry.
- CMOS circuitry for low power consumption.
- HP-IL for general I/O operations.
- Built-in magnetic card reader/writer.
- Typewriter keyboard and editing keys.
- 32-character LCD display.

1-9. Specifications for the HP-75 are listed in table 1-1.

Table 1-1. Specifications

Physical Properties
o Width: 25.7 centimeters (10.11 inches). o Depth: 12.9 centimeters (5.09 inches). o Height: 3.0 centimeters (1.17 inches). o Weight: 680 grams (1.50 pounds).

Table 1-1. Specifications (Continued)

Environmental Limits

- Operating Temperature: 0 to 45 degrees C (32 to 113 degrees F).
- Charging Temperature: 10 to 40 degrees C (50 to 104 degrees F).
- Storage Temperature: -40 to 55 degrees C (-40 to 131 degrees F).
- Operating and Storage Humidity: 0 to 90 percent relative humidity.

Power

- Primary: HP 82001B battery Pack.
- Recharging time for pack: 9 hours.
- Usage:

On (Awake)	200 milliwatts
Idle (light sleep)	100 milliwatts
Off (deep sleep)	200 microwatts

Display

- Type: LCD (liquid crystal display).
- Number of characters: 32.
- 5 x 9 apparent dot matrix.

Keyboard

- 65 key QWERTY typewriter style.
- Consists of three groups:
  - Typewriter Keys.
  - Edit keys.
  - System keys.

Interface

- Type: HP-IL (Hewlett-Packard Interface Loop).
- Default on Power Up: system controller.

Magnetic Card

- Length: 25.4 centimenters (10 inches).
- Width: 1.0 centimeter (0.38 inches).
- Thickness: 0.2 centimeters (0.09 inches).
- Temperature Limits: 4 to 32 degrees C (40 to 90 degrees F).
- Humidity Limits: 20 to 80 percent relative humidity.

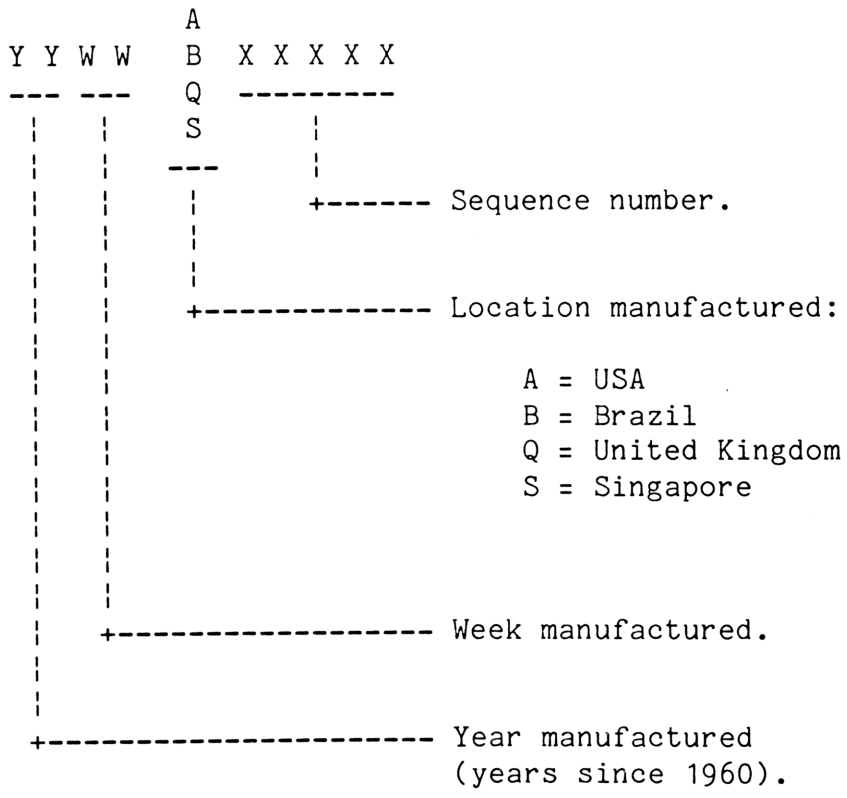
Table 1-1. Specifications (Continued)

Card Reader

- Maximum read/write speed: 76.2 centimeters (30 inches) per second.
- Minimum read/write speed: 12.7 centimeters (5 inches) per second.
- Number of tracks: 2 data and 2 timing.
- density: 315 bits per centimeter (800 bits per inch).
- Format: 8 bits per byte.
- Formatted capacity: 650 data bytes per track.
- Encoding method: MFM (modified frequency modulation).

1-10. IDENTIFICATION.

1-11. The serial number of the computer is used for identification and determination of the warranty status. It is located along the top edge of the back cover near the battery door. Its format is shown below:



SECTION
II

Theory of Operation

2-1. FUNCTIONAL DESCRIPTION

2-2. The HP-75 Portable Computer (see figure 2-1) consists of eight primary logic circuits:

- o CPU (central processing unit).
- o Clock/Keyboard/RTC (real-time clock).
- o RAM (random-access memory).
- o ROM (read-only memory).
- o LCD (liquid-crystal display).
- o Card Reader.
- o HP-IL (Hewlett-Packard Interface Loop).
- o Power supply.

2-3. The HP-75 provides several methods for the user to transfer information to and from the computer. Standard input entry is through a 65-key modified typewriter keyboard. Standard output is through the 32-character LCD display. The remaining I/O consists of:

- o 8K, 16K, 24K, 32K, 40K, or 48K plug-in RAM or ROM modules (BASIC or assembly files) up to a total of 144K.
- o Programmable 1 Hz to 1.7 kHz audio speaker.
- o Hand-operated card reader providing both input and output capability. There are two tracks per card with a maximum of 650 bytes per track.
- o HP-IL interfacing, which allows up to 30 input and/or output devices on the loop.

2-4. Additionally, the HP-75 is able to expand its random-access memory using a plug-in 8k byte memory module.

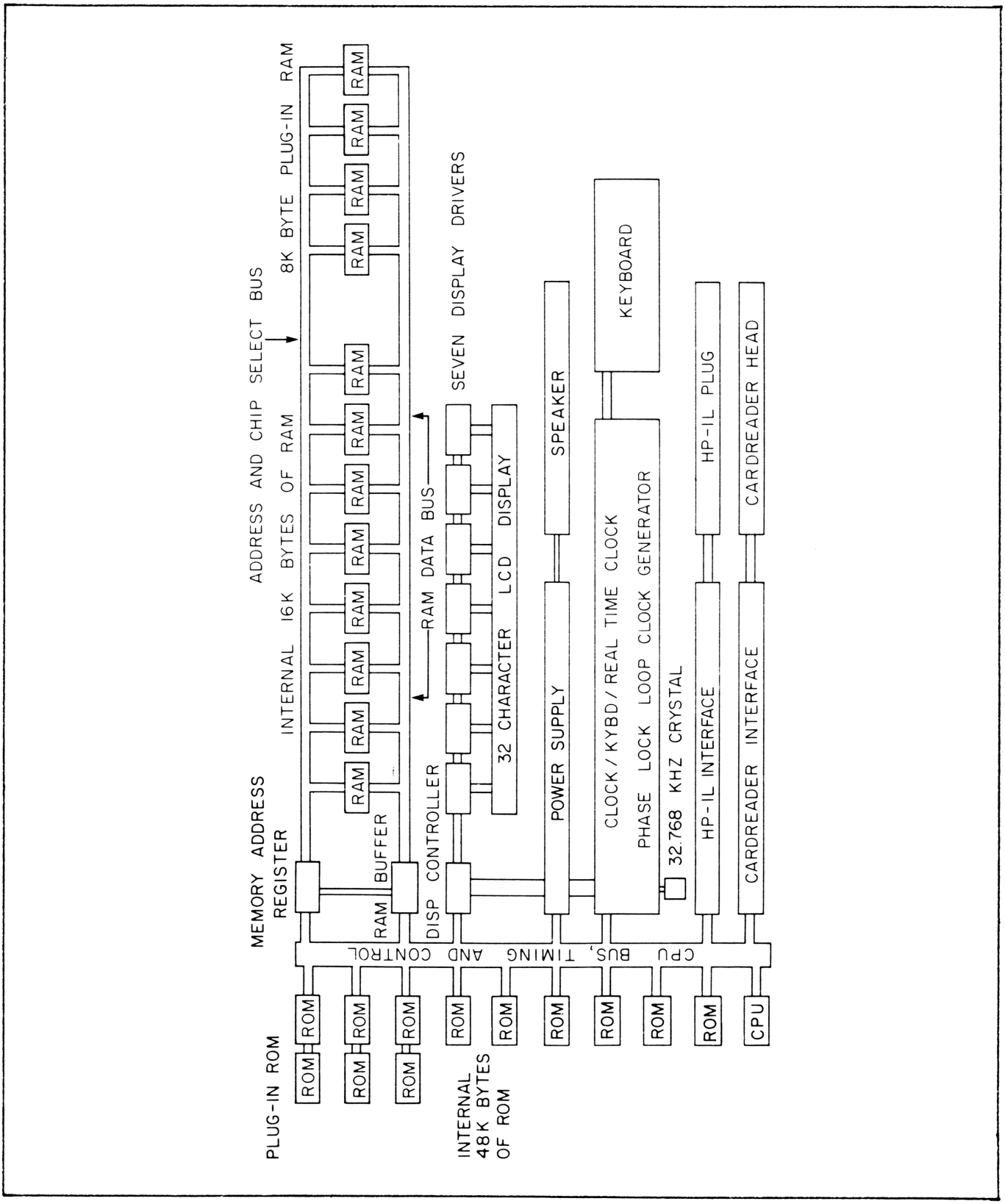


Figure 2-1. HP-75 System Block Diagram

2-5. The logic PCA (printed-circuit assembly) (A2) contains the following:

- o CPU IC (integrated circuit) (U3).
- o Clock/Keyboard/RTC IC (U2).
- o Six system ROM ICs (U8 through U13).
- o MAR IC (memory-address register) (U6).
- o Buffer IC (U7).
- o HP-IL IC (U4).
- o Card reader IC (U5).
- o Card-reader head assembly.
- o Display controller IC (U1).

2-6. The display assembly (A3) contains the following:

- o Seven display driver ICs (U1 through U7).
- o 32-character (apparent 5x9 dot matrix) LCD.

2-7. The power supply/memory PCA (A1) contains the following:

- o Dc-to-dc converter.
- o Battery level detect.
- o Battery charger circuit.
- o Generator for the display reference voltages.
- o Buzz circuit.
- o Automatic reset circuit.
- o 16K of RAM.
- o 8K memory module connector.
- o HP-IL interfacing.

2-8. CPU

2-9. The CPU (see figure 2-2) used in the HP-75 was designed to ease the software task in developing calculator type products. The CPU can uniquely address 65,536 bytes of memory (16-bit address). It has multilevel vectored interrupt capability and allows a crude form of direct memory access (DMA). It also contains 64 general-purpose eight-bit registers. Binary and decimal arithmetic and shift operations can be easily performed. To simplify multibyte arithmetic operations and allow string manipulations, the CPU performs instructions that operate on data one to eight bytes in length.

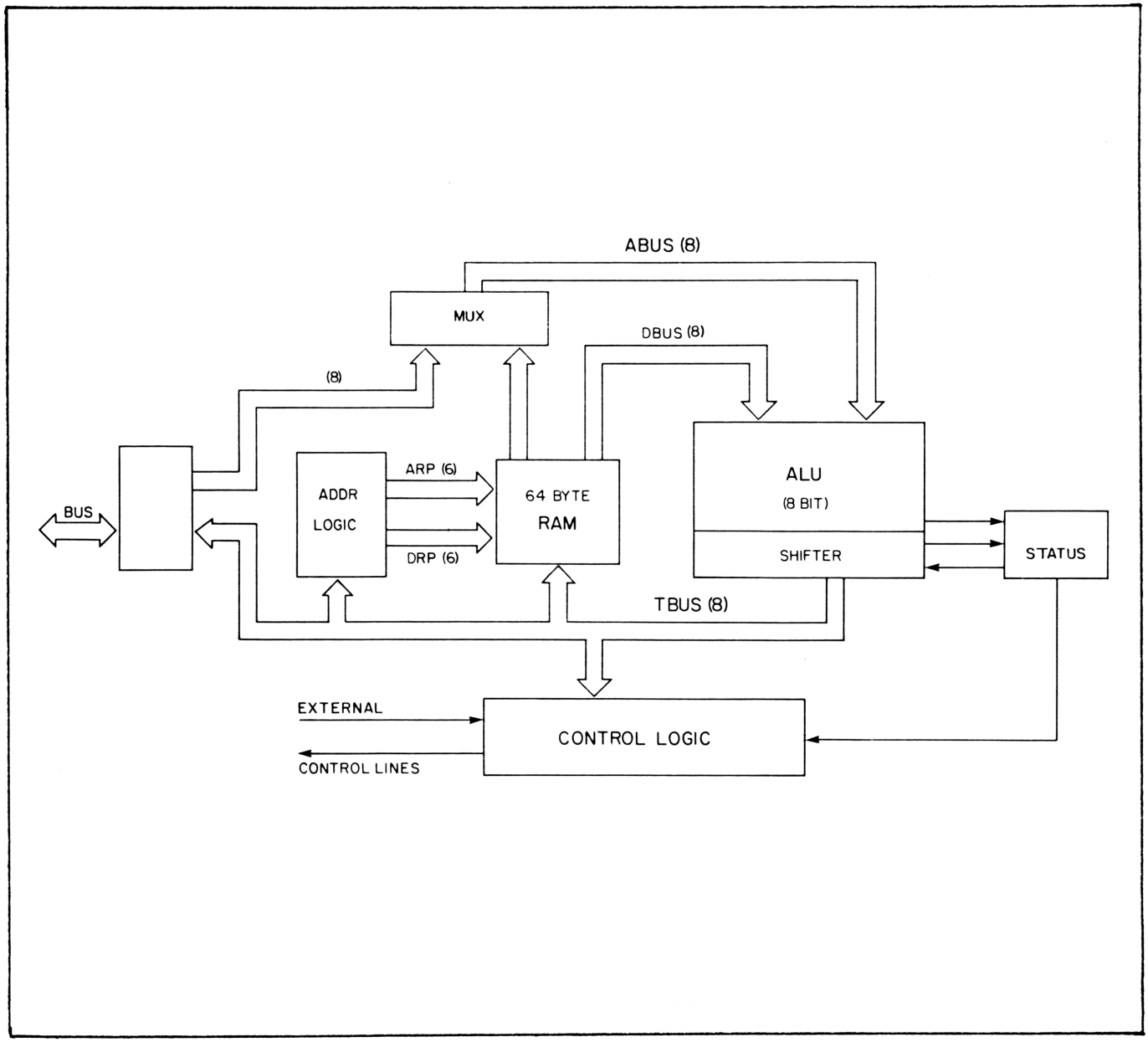


Figure 2-2. CPU Block Diagram

2-10. When the CPU branches to a subroutine or a program call, the CPU stores the return address in a stack that the CPU creates in RAM. The stack is controlled by a stack pointer in a CPU register (see figure 2-3). Because the return address is stored in RAM, the CPU can handle an almost unlimited nesting of subroutines and program calls. Any of the CPU register pairs can be used as a stack pointer. Both direct and indirect operations can be performed on both increasing and decreasing stacks.

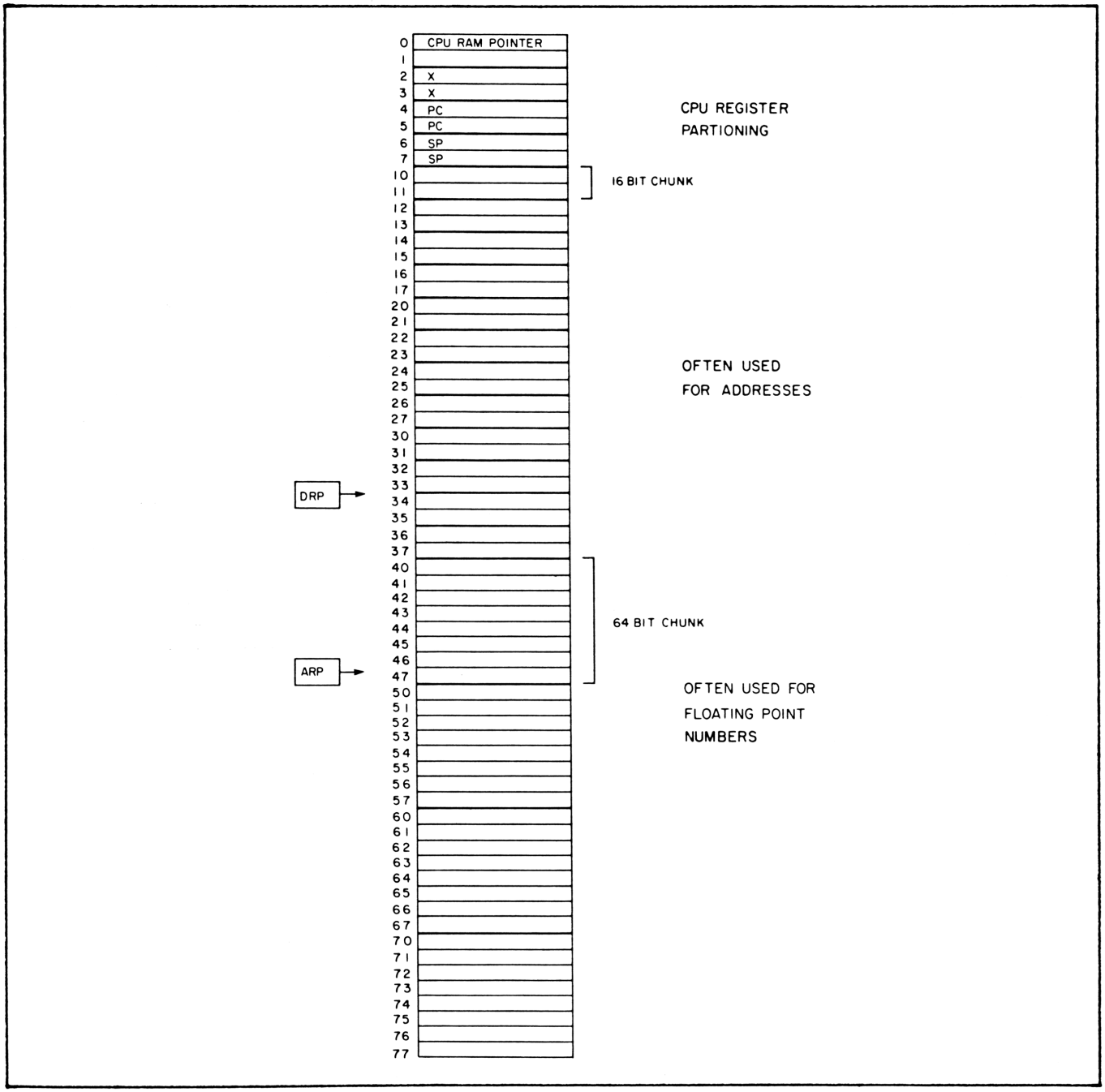


Figure 2-3. CPU Register Diagram

2-11. An eight-bit bus handles all communication with the other ICs. This eight-bit multiplexed bus transports data, instructions, and addresses. When more than one byte of data is sent on the bus, an address is needed only for the first byte. The remaining data is assumed to be in consecutive memory locations. Therefore, the bus primarily moves data and instructions while minimizing the movement of addresses. Signal names are listed in table 2-1.

2-12. The memory in the HP-75 handles the implementation of this method by incrementing the address register upon receiving a read or write command. Also, the instruction-fetch sequence does not require an updated address when fetching from most consecutive locations.

2-13. RAM

2-14. The RAM in the HP-75 is fabricated in CMOS (complentary metal-oxide-semiconductor). This process allows the RAM to retain its contents when the CPU is inactive and the power supply is in its powered-down state. While the computer is off, a fully charged battery pack can retain the contents of the RAM for at least two months. A capacitor inside the computer allows the user at least 30 seconds to change the batteries without losing the contents of the RAM, providing the computer is first turned off.

2-15. The HP-75 has the capability of supporting up to 24K bytes of RAM. The HP-75C has eight RAM ICs, which are fabricated in a 2K x 8-bit structure, for a total of 16K bytes of RAM. The computer is allowed to accept an 8K byte plug-in memory module to expand the allotted memory to 24K. The HP-75's internal operating system checks memory at turn on to determine if there is a plug-in memory module.

2-16. Two ICs interface the CPU's bus to the RAM. The memory address controller (MAR) and the buffer function together as one unit.

2-17. MAR

2-18. The primary functions of the MAR IC are:

- Holds the 16-bit current memory address.
- Accepts a new address from data bus as two sequential bytes.
- Increments the address after each memory access (except I/O accesses).
- Drives IC select and address lines for the RAM ICs.
- Selectively activates 12 memory IC enables.
- Drives read/write control line for RAM ICs.

Table 2-1. Signal Descriptions

SIGNAL	DESCRIPTION
A0-A11	Address output lines to RAM
AGND	Analog ground
AVI	Analog intermittent power supply
B	Bank select, brought out to center port
B0-B7	System data bus lines, valid during PH1
BDK	Battery K detect line
BDR	Battery R detect line
BUZZ	Speaker control line
C0-C25	Column outputs used to drive LCD, on display PCA only
C0-C7	Keyboard column lines
CAP	Internal oscillator, frequency set by capacitor.
CDS	Address code select, used to determine I/O address
CLK	Clock, clocks data from A2U1 to A3U1-A3U7
CS1-CS3	Chip select, 8K address space enable
CTL	Control keyboard line
DOT ON	Dot on, turns dots on in A3U1-A3U7
DOT OFF	Dot off, turns dots off in A3U1-A3U7
DATA	Data, sends data to display drivers
DATA IN	Serial data input
DATA OUT	Serial data output

Table 2-1. Signal Descriptions (Continued)

SIGNAL	DESCRIPTION
DGND	Digital ground
DT1/DT2	Differential inputs from data track read coil
DVI	Digital intermittent power supply
E0-E11	Decoded chip enable outputs to RAM ICs
FI	Output of phase comparator
FO	Output of low pass filter, input to VCO
GND	Ground
H	Half select, selects 32K-56K memory address
HALT	HALT, CPU finishes current instruction and releases data bus control
INH	Inhibit, inhibits the ROM from responding to its address
IRL	Interrupt Request Line, system
LC1/LC2	HP-IL Timing
LE	Logic enable, sets positive or negative true logic on the RAM enable lines
LMA	Load memory address, system control line, valid during PH2
LW	Logic write, sets positive or negative true logic on the RAM write lines
PH1/PH2	System clocks
PRIL	Priority Low, daisy chain interrupt control line
PRIH	Priority High, daisy chain interrupt control line

Table 2-1. Signal Descriptions (Continued)

SIGNAL	DESCRIPTION
PWO	Power On, system reset line
R0-R9	Keyboard row lines
RB	VCO bias
RB0-RB7	RAM data bus lines
RD	Read, system control line, valid during PH2
RG	VCO gain
ROW1-ROW8	Row output drive lines of LCD
RV1-RV3	Reference voltage, used to drive LCD logic levels
RXD0, RXD1	HP-IL Receive Lines
S	Start-up address, grounded for start-up address 0
S1/S2	ROM select code, determines the address that the plug-in ROM will respond to
STROBE	Data latch into display drivers.
SCL	Power supply control line
SHIFT	Shift keyboard line
TSTR4	ROM P4B test line
TT1/TT2	Differential inputs from the timing track read coil
TXD0, TXD1	HP-IL Transmit Lines
VC	Continuous system power supply
VI	Intermitent system power supply

Table 2-1. Signal Descriptions (Continued)

SIGNAL	DESCRIPTION
W	Write, RAM write signal
W1/W2	Write amplifier outputs to the data track write coil
WCT	Write coil center tap
WR	Write, system control line, valid during PH2
XC1-XC14	External components connection lines
XI/XO	Crystal oscillator signal lines
2K/1K	2K or 1K select, selects 2K address spaces for chip enables (CE)

2-19. Buffer

2-20. The main functions of the buffer IC are:

- Buffer the eight-bit data bus to reduce capacitive loading to both the CPU and RAM.
- Monitor the MAR control lines to determine which bus, CPU or RAM, it should drive.
- Latch data in both directions during data transfer clock (PH1).
- Latch data to the RAM when not reading to reduce power consumption by not needlessly changing the RAM bus states.

2-21. ROM

2-22. The system ROM on the logic PCA is 48K bytes. It can be expanded up to 192K bytes. The HP-75 has three plug-in ROM ports, which can accept up to 48K (in 8K increments) in each port.

2-23. The ROM memory is built around six ICs (U8 through U13). Each ROM stores 64K bits in an 8K-byte format. The ROM ICs interface directly with the multiplexed system bus and use an internal MAR to hold the current address. The ICs have control circuitry that allow software to enable and disable the ROMs through the use of I/O addresses. This allows more than one ROM IC to exist in the same address space. The ROM inhibits its output drivers when the current address is in the I/O area.

2-24. LCD Display

2-25. The HP-75 uses a 32-character dot-matrix liquid-crystal display (LCD) as its primary output device. Included in the LCD are four annunciators that indicate the status of the battery, programming errors, appointments that are due, and program that are running. Each character position is represented by an apparent 5 x 9 dot matrix. The eighth row is extended downward to provide for underlining and descenders on lowercase letters. The eight rows on the display are multiplexed so only one is displayed at a time. The rows are cycled often enough so that the human eye can not see the multiplexing.

2-26. Eight ICs, a display controller (A2U1) and seven display drivers (A3U1 through A3U7), are used to drive and control the LCD. The display controller is the interface to the CPU and is part of the logic PCA. The display drivers are on the display PCA.

2-27. Display Controller

2-28. The display controller (U1) controls the display driver ICs. The display controller interfaces directly with the CPU. U1 generates the voltage levels and timing waveforms necessary to multiplex the LCD. This IC also contains a character pattern ROM, which translates the ASCII character codes to the display characters. These features allow the display to be independent of the CPU except for changing the data. Data is written by the CPU while addressing U1 through its I/O address. The CPU writes two bytes of data: the first is the position of the character on the display, the second is the ASCII equivalent byte. In addition, one of two types of cursor fonts may be chosen. Also, each character has the option of being underlined.

2-29. Display Driver

2-30. The HP-75 uses seven ICs to drive the column lines of the LCD. Each IC is able to drive 25 columns. Data for each row is sent to the display drivers from the display controller and is received serially while the previous row is being displayed (see figure 2-4). A strobe signal from the controller latches the data inside the display driver. This data then is used to determine the proper waveform to turn the dot on or off.

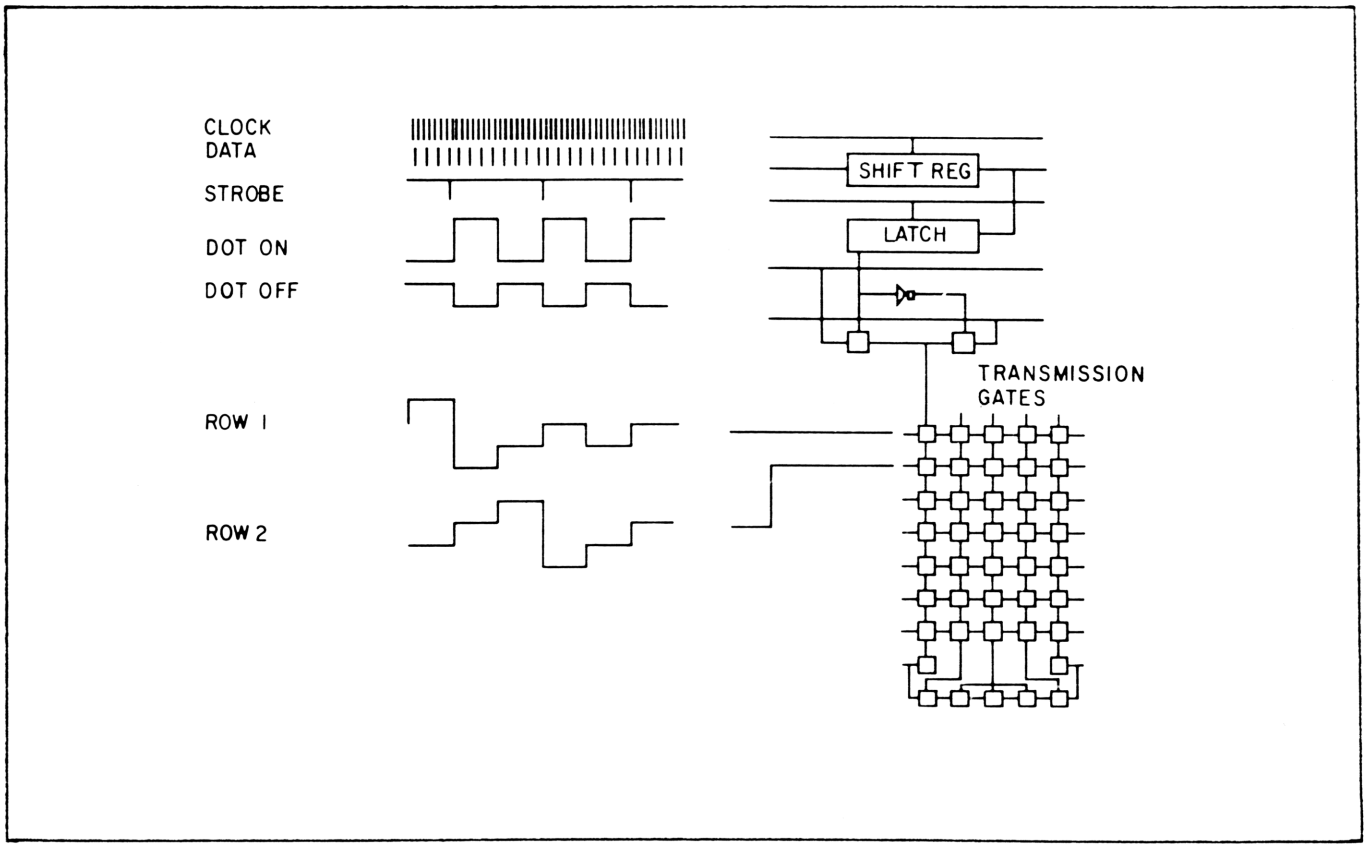


Figure 2-4. Display Waveforms

2-31. Card Reader

2-32. The card reader IC provides magnetic card storage capability for the HP-75. This IC is designed to interface directly with the CPU through an I/O address.

2-33. The magnetic card is manually pulled through the card reader slot. The card reader provides read and write functions for card speeds from 5 to 30 inches per second (ips) at 800 bits per inch (bpi).

2-34. Low and high speed error flags are set for card pull speeds outside the 5 to 30 ips speed range. An error occuring in the read decode process also sets an error flag.

2-35. Clock/Keyboard/RTC

2-36. The clock/keyboard/RTC (real-time clock) IC (U2) is used in the HP-75 to perform the following functions:

- o System clock generation.
- o Real-time clock (RTC).
- o Keyboard control.
- o Time comparator.
- o Buzzer interface.
- o Power detect and control.

2-37. This IC is designed to interface directly with the CPU in the HP-75. The above functions communicate with the 8-bit CPU bus by way of an internal bidirectional 8-bit bus. The I/O control section of this IC controls the reading and writing to different sections internal to the integrated circuit. The I/O control section also controls the data flow between the external bus and the CPU. All communication to U2 is through I/O addresses sent from the CPU.

2-38. U2 requests service from the CPU through use of the CPU's interrupt signal line. There are four different sections in U2 that can cause interrupts to be sent to the CPU by way of the IRL line. The timing and priority of these events are handled by an interrupt-control section in U2.

2-39. The system clock generation section has three different working states, which can be controlled by the CPU: deep sleep, light sleep, and awake. For more information about these states, refer to the section on system timing, paragraph 2-134.

2-40. Keyboard

2-41. The HP-75's primary input device is a 65-key touch type keyboard. Each key is located above a dome-shaped snap disc that is mounted over the keyboard printed-circuit board. When the system is on, U2's keyboard logic scans the eight column lines (C0 through C7) bringing each line low every 8 ms. When a key is pressed, the snap disc shorts the corresponding row and column lines. The row line is brought low by the column line and the scanning stops. There are 10 row lines (R0 through R9) that can contact the 8 columns lines. (See figure 2-5.)

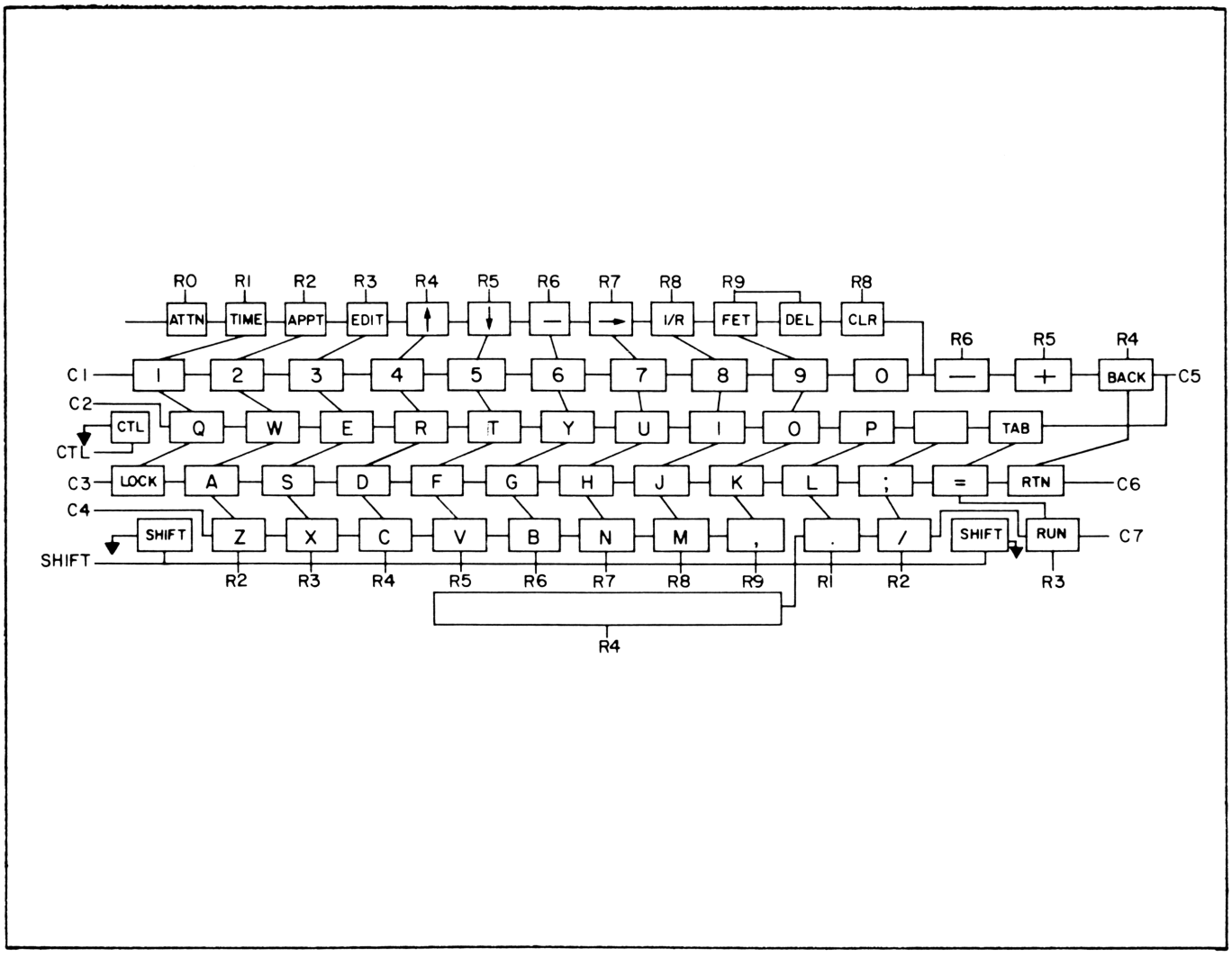


Figure 2-5. Keyboard Layout Diagram

2-42. After a key has been pressed, the logic circuitry waits 8 ms to see if the key is still down before requesting service from the CPU. This action prevents multiple key entries due to mechanical bounce of the snap disc. The CPU receives two bytes of information from the keyboard. One byte contains the 8-bit keycode of the key depressed. The other byte contains status of the keyboard at the time the information is being transferred. When shift and/or control are depressed, they affect bits in the status to the CPU. If a key is held down continuously (longer than 1 sec), the keyboard repeats the keycode every 128 ms until the key is released.

2-43. HP-IL IC

2-44. The Hewlett-Packard Interface Loop (HP-IL) is a serial interface that is designed to conserve power. HP-IL IC (U4) interfaces the loop directly with the CPU. This IC implements the controller, talker, or listener functions and allowable combinations.

2-45. HP-IL is structured to send groups of 11 bits, three control bits and eight data bits. A group of 11 bits is called an HP-IL message (see figure 2-6). Each HP-IL message should go completely around the loop and be returned to the device which originated the message for error checking. Messages that the HP-75 HP-IL IC sends are automatically error-checked when they return. The CPU is notified only if an error is detected.

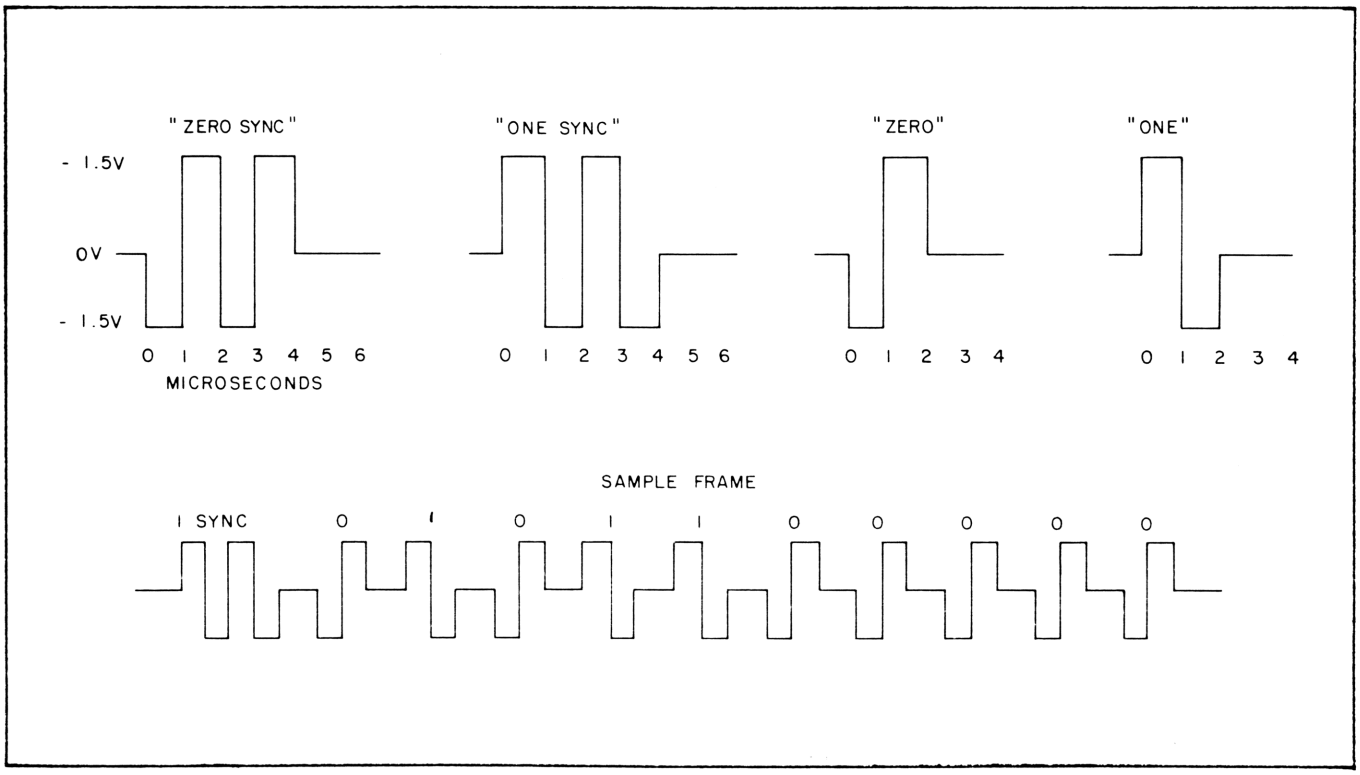


Figure 2-6. HP-IL Bit Encoding

2-46. In most circumstances, messages that do not affect this device are automatically retransmitted without any CPU action. This IC may also be set to send a service request or to automatically respond to a parallel poll.

2-47. Two 8-bit general-purpose scratch pad registers are included on the IC.

2-48. The HP-IL driver and receiver circuits are isolated from the actual interface lines with pulse transformers and a few discrete components. This circuit provides floating balanced pairs of input and output lines with proper loading, EMI (electromagnetic interference) reduction, and impedance matching. Each message consists of bits encoded in a three-level format, as shown in figure 2-6. The high and low pulses on the loop side are +1.5V and -1.5V nominal across the pair of wires. Pulses are typically 1 microsecond (us) wide, with at least 2 us delay between bits. The IC has an oscillator that requires an external LC network for frequency control.

2-49. U18 is the transformer package (two transformers for the receive circuit and one for the transmit circuit) used to interface the HP-IL IC to the loop. (This is used for noise reduction and loop isolation.) VR5 through VR8 are used to help reduce susceptability to ESD. R28 through R31 match impedence, and C21 and C22 reduce conducted and radiated interference. (See figure 2-7.)

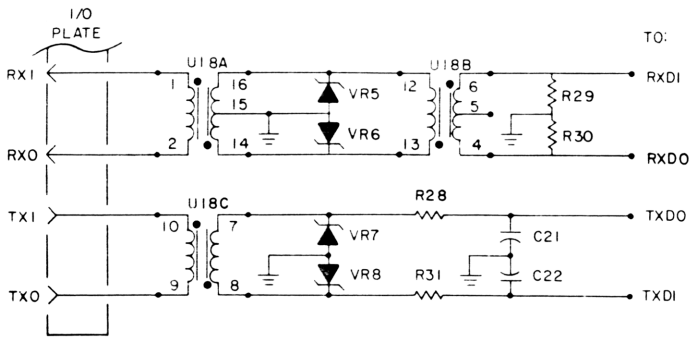


Figure 2-7. HP-IL Circuit

2-50. The CPU communicates with the HP-IL IC through I/O memory read and write cycles. There are eight locations or registers in the IC which the CPU may want to read from or write to. Each location or register requires a different addresses from the CPU. Additionally, the HP-IL IC may take different actions depending on the value of the bits in the registers. Reading or writing to different bits in the registers causes other U4 requests service from the CPU through the IRL line.

2-51. Power Supply

2-52. The power supply provides the properly regulated power to the various parts of the HP-75 system. The main system power is 5.5V provided by the dc-to-dc converter. Additionally the power supply provides the three reference voltages required by the LCD and drives the buzz circuit to the speaker.

2-53. The HP-75 normally operates from three rechargeable NICAD batteries or three nonrechargeable alkaline batteries. However, the power supply is designed to allow the computer to operate from only the rechager when no batteries are installed.

2-54. The power is supplied to the RAM to maintain their contents even when the computer is off.

2-55. CARD READER DESCRIPTION

2-56. The HP-75 card reader system consists of:

- o A two-track (read and read/write), flat-ground, three-coil, single-gap, head.
- o A precision-molded head mount/card guide.
- o Magnetic cards with four prerecorded and tested tracks.
- o A CMOS analog/digital IC circuit and associated external components that:
  - Communicate with the HP-75 bus.
  - Provides a state maching that decodes and encodes data into the MFM code used on the card and controls the IC operation.
  - Has an internal phase locked loop (PLL) to generate a 5-MHz clock for the IC and card reader timing.
  - Interfaces the digital circuitry to the head with write drivers and read sense amplifiers.

2-57. Magnetic Card

2-58. Each magnetic card has two tracks available for data storage. Each data track has an associated timing track used for speed indication during read and write operations. Up to 650 bytes of user information can be stored on each data track. Additionally, system data is also stored on the card. Figure 2-8 shows the general layout of the tracks and information.

2-59. There are four tracks on the card. The two timing tracks are recorded on the full length of the card at a constant 800 flux reversals per inch. The data tracks contain four records each. The data is recorded in MFM coded format which varies the density from 400 to 800 flux reversals per inch.

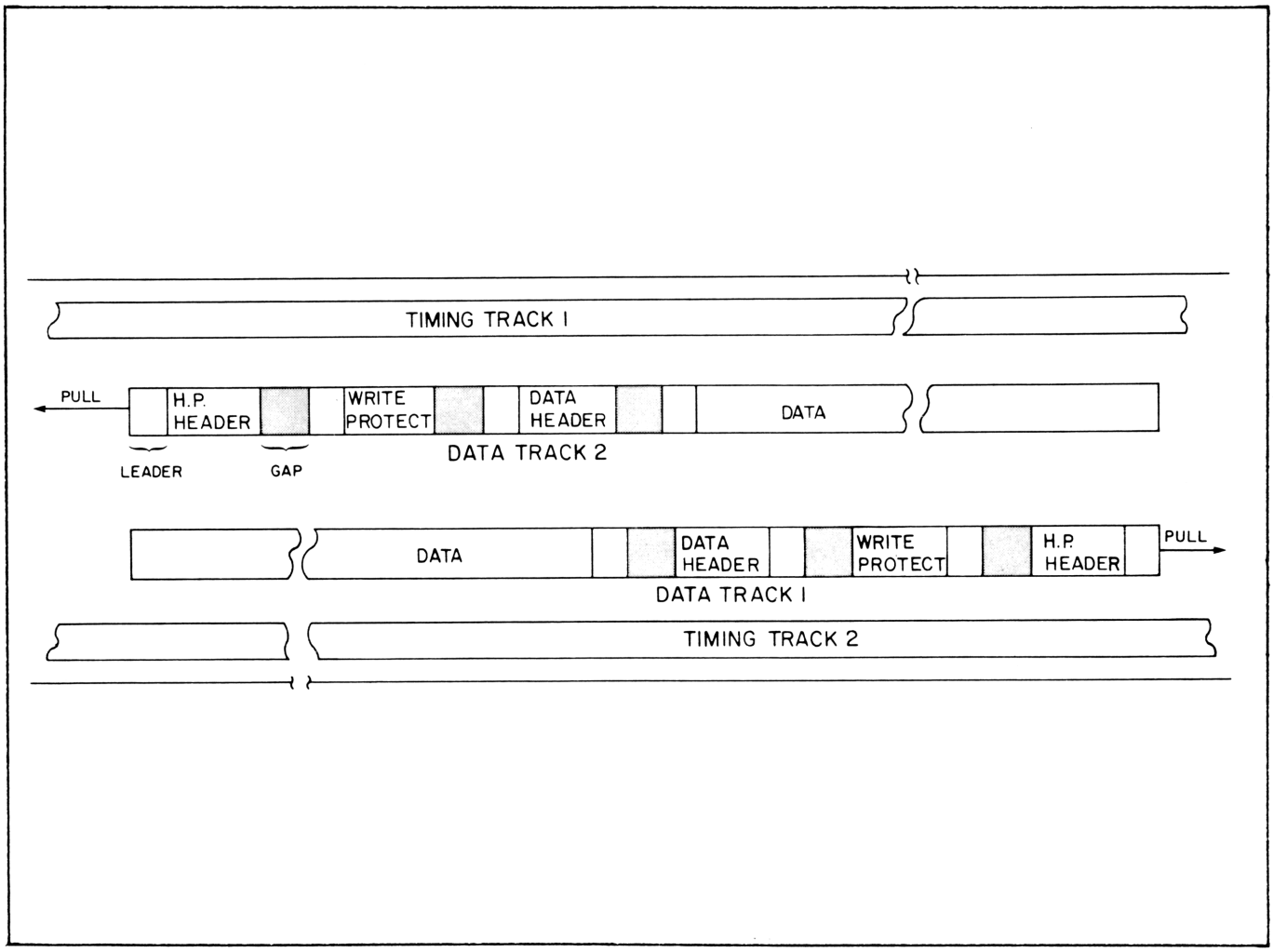


Figure 2-8. Magnetic card Layout

2-60. Card Reader IC Electronics

2-61. Figure 2-9 is a block diagram of the card reader electronics. The I/O and data control communicate with the HP-75 bus. The ROM controller, cell counter and other miscellaneous circuits constitute the main IC control. The phase locked loop (PLL) provides the 5-MHz clock needed to provide resolution to the cell counter. The analog circuitry interfaces the digital controller with the head.

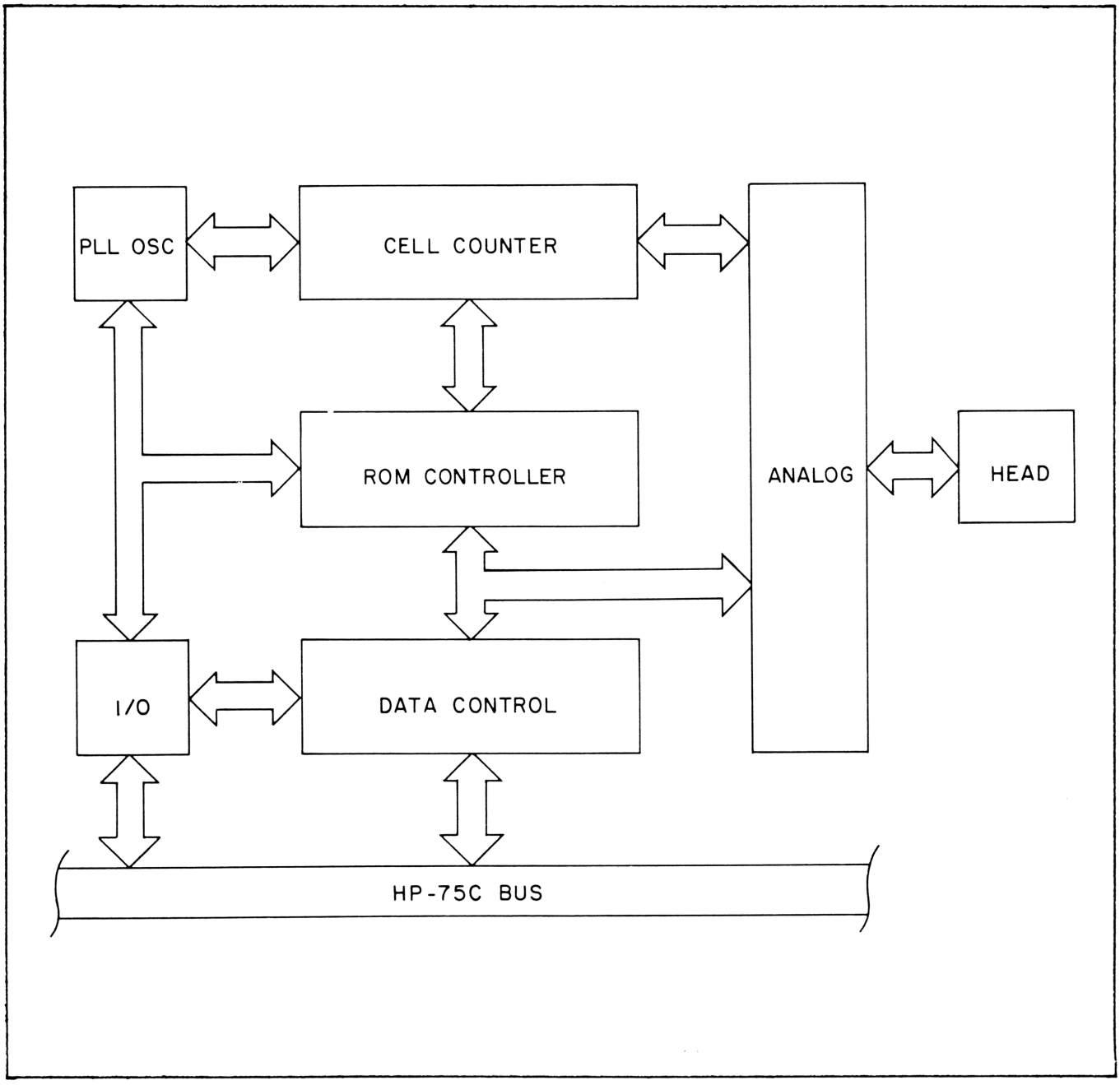


Figure 2-9. Card Reader Block Diagram

2-62. System Bus Communication

2-63. The U5 card reader IC communicates with the HP-75 via the system bus. Communication is by way of two-byte reads and writes--one byte of status and one byte of data for each card reader access. The IC does not use the interrupt capability of the system.

2-64. When the card reader IC is not turned on, the RB and RG are pulled high to VI, and the HFIO pad is pulled low. FO and FI will both be at the same level and can be either high or low.

2-65. When the CPU addresses the card reader IC and turns it on, the internal signal CLK ON goes high, the reference signal PH1 (PHI 1 ANDed with CLK ON) is supplied and the VCO allowed to run.

2-66. The VCO in the PLL is designed so that a more positive voltage at it's voltage control input (RC filter output FO) will cause a decrease in the frequency of the VCO. A decrease in controlling voltage results in an increase in operating frequency.

2-67. If during operation, the incoming reference frequency increases, the filter output voltage will decrease and the VCO will run faster to establish a lock condition. If the reference frequency decreases, the filter output voltage will go more positive to establish lock. If the reference frequency makes a sudden change in frequency, the loop will make a relatively slow over-adjustment and will respond with a damped sinusoid oscillation. The voltage at the filter output can be seen to exhibit this damped sinusoid oscillation and the VCO responds to this input according to its frequency vs input voltage characteristic. This situation occurs at IC turn on as the loop attempts to capture the reference frequency from a non-running condition.

2-68. An unstable loop will not exhibit a damped oscillation, but will respond with a continuing, non-decaying oscillation. The gain of the VCO (as determined by RG, the VCO devices, and the RC filter values) determine the loop stability.

2-69. Ideally, during steady state operation, the loop will lock and the VCO will run at a single non-varying frequency (assuming constant input frequency). However in order to assure stability and the capability of capturing a given range of incoming frequencies, jitter exists in the loop. This can be seen at the HFIO pad where the period of the clock continuously varies around some center value. Also, voltage ripple can be seen at the RC filter output. There are actually two components of ripple at the filter output FO. One component is a 305.85-kHz, 0.6V (approximately) sawtooth signal caused by the card reader PLL RC filter. The other is a 32.768-kHz component. The reference clock used by the card reader PLL is itself derived from a PLL. Its filter ripple frequency is 32.768 kHz, and therefore the reference frequency for the card reader PLL varies at this rate. This varying input frequency shows up as a low frequency component in the card reader PLL filter voltage output and as a low frequency component of jitter in the clock output.

2-70. In order to account for temperature extremes, power supply variation, VCO variations from IC to IC, jitter on the incoming reference clock, and component count, the U5 card reader IC PLL has considerable jitter. Card reader PLL jitter can be as high as approximately 7.5 of the center frequency.

2-71. Analog Circuitry

2-72. Figure 2-10 is a simplified diagram of the read sense amplifiers. There are two of these circuits on the IC. The signal points (XC5, for example) and components (R12, for example) refer to the timing track sense circuit. Those presented in parentheses refer to the data track circuit (XC8 and R13, respectively). The components shown with letters (Ra and Qa, for example) are internal to the IC.

2-73. Input/Variable Gain Stage

2-74. Ra provides a load for the read coil, which develops a signal to be amplified by A1. VMID is provided by a low impedence buffer and is set to half the supply voltage. XC1 is an AGC voltage provided by the AGC circuit. This AGC voltage controls the resistance of transistor Qa. The ratio of this resistance and that of resistor Rb control the gain of this input stage.

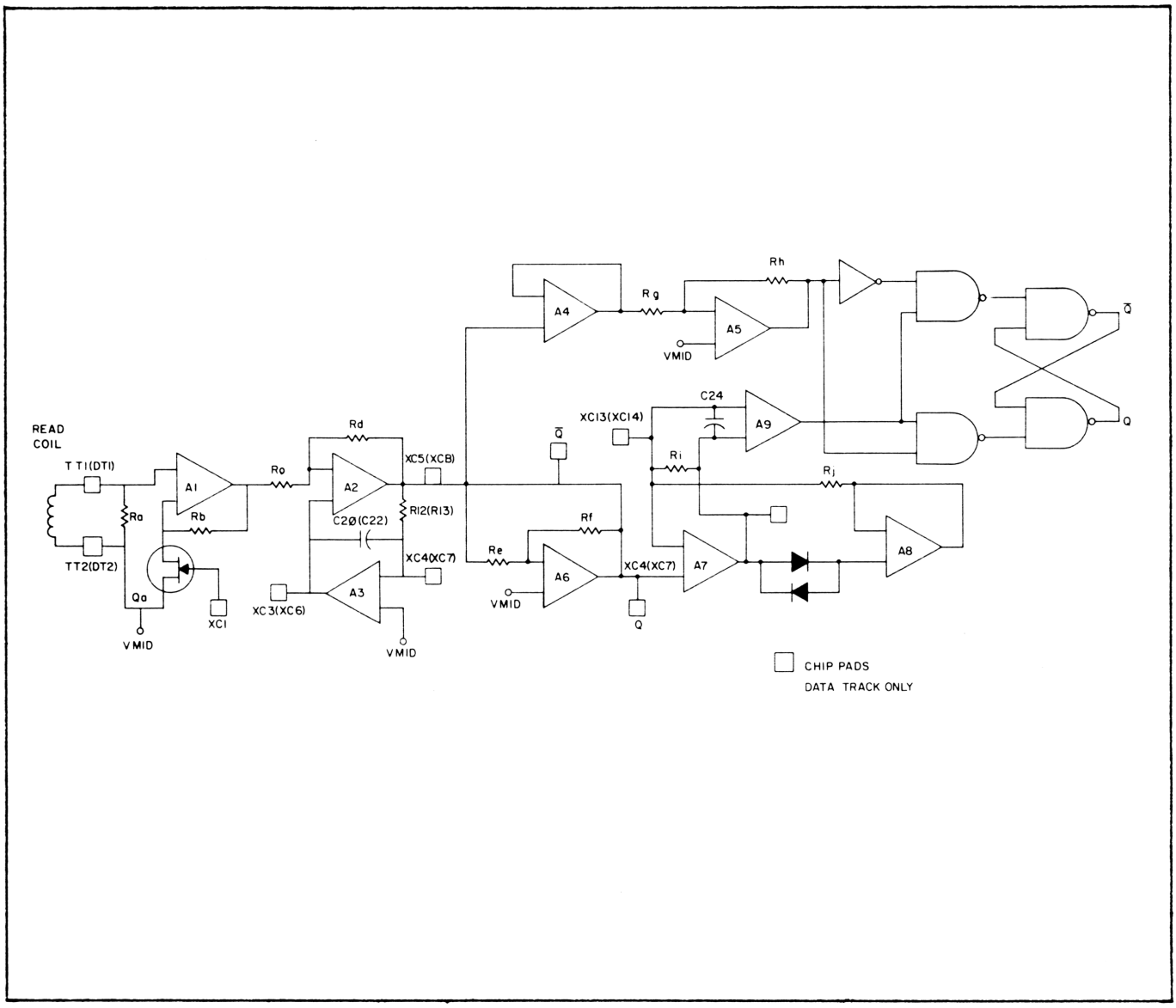


Figure 2-10. Read Sense Amplifier Diagram

2-75. Bandpass/Fixed Gain/Offset Correcting Stage

2-76. The input and feedback resistors Rc and Rd set the bandpass gain for amplifier A2. Amplifier A3 is an active filter feeding back the low frequency components of the signal to A2 providing the low frequency rolloff. External components R12 and C20 (R13 and C22 for the data track) are selected to reduce low frequency noise while still reproducing the read signal with minimal distortion at the frequency of interest. This signal presented at XC5 (XC8) is routed to two seperate detection circuits. Amplifiers A4 and A5 provide a threshold detect and A7, A8, and A9 (along with inverter A6 and some switching logic) provide a peak detect.

2-77. Schmitt Trigger

2-78. Amplifier A4 buffers the input to Schmitt trigger A5. The positive feedback provided by resistors Rg and Rh determine the level of hysteresis. They are set to switch the output at 0.6V above and below VMID.

2-79. Inverter

2-80. A6 is configured as a unity gain inverter with equal values for Re and Rf.

2-81. Peak Detector

2-82. The peak detect circuit consists of amplifiers A7 and A8 and comparitor A9. The output switching logic coupled with the input transmission gates provide a positive-going signal to the peak detect circuit. The peak detector only detects positive peaks. The output logic waits for a positive threshold from A5 and then fires on the next peak detect from A9. It then waits for a negative threshold from A5 and then waits for the next peak. The peak detector is very sensitive and will oscillate with no signal applied. This is one reason for using the Schmitt trigger to allow the signal to get out of the noise before a peak is to be detected.

2-83. During the rising of the input signal, A7 is in a unity gain configuration with its output a diode drop above its negative input. This keeps comparitor A9's output low. The top diode in figure 2-10 is conducting and charging up the capacitance on the positive input to A8. When the input signal reaches a peak and starts coming down, the diode stops conducting, A8 is held to the peak value, and A7 is now configured with a gain of 20. The output of A7 comes down quickly to overcome the diode drop difference, and comparitor A9 switches.

2-84. C24 is used to stabilize the detector on the data track. On the timing track the peak detector is not used; XC10 is tied to ground and XC13 is tied to VI. This sets the output of A9 always high so the circuit acts as a threshold detector.

2-85. Automatic Gain Control

2-86. The gain control circuitry provides a voltage at XC1 that sets the gain of both read sense amplifiers. In the HP-75 system, the timing track is recorded continuously over the length of the card, while the data track stops and starts in a series of records. The timing track signal amplitude is monitored at XC5 by the AGC circuit, which controls the gain of both tracks.

2-87. In figure 2-11, XC5 is the amplified timing track signal. TT2 is a dc voltage set internally at half the supply voltage. XC1 is the AGC control node. VREF is an internal voltage set at 0.7V above the voltage at TT2. C21, CR1, and CR2 act as a voltage doubler circuit. R11 and C18 provide the load for that circuit. The doubler circuit is such that the voltage developed across R11 is equal to the peak-to-peak voltage at XC5 minus the low current diode drops of CR1 and CR2. C18 and R11 provide a slow enough time constant to keep the current through the diodes small enough to ensure a drop of only 0.4V across each diode. R19 and C19 control the integration rate of the amplifier and are selected to provide the best time constant for compensation of variations in pull speed and recovery of dropouts. The integrator compares the voltage doubler output to VREF and increases or decreases the gain accordingly. The circuit is designed to hold the amplitude at XC5 to VREF-V(TT2)+two diode drops=1.5V peak-to-peak. The data track (XC8) gain is set by the same voltage but is not monitored. The data track signal at XC8 can be expected to vary by plus or minus 50 percent in amplitude and still provide a useful signal to the peak detector circuitry.

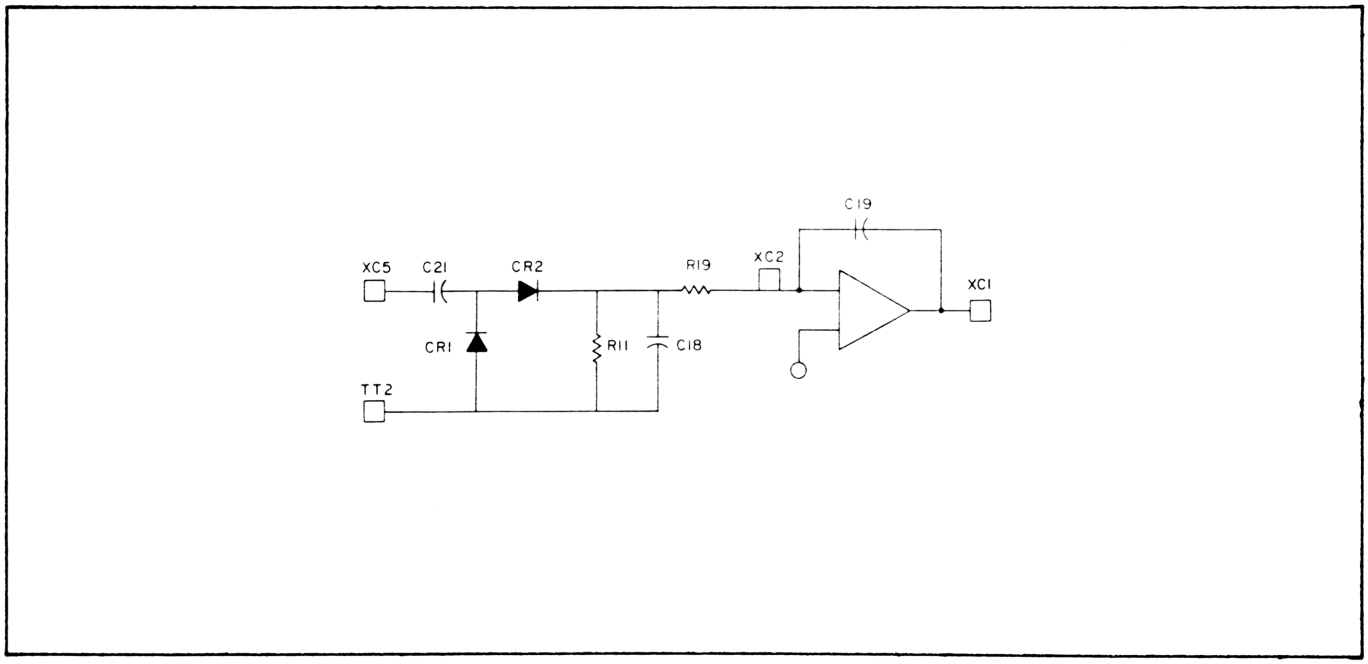


Figure 2-11. Automatic Gain Control Diagram

2-88. Noise Filtering

2-89. R10 and C14 provide low pass filtering for the power lines (see figure 8-2, Power Supply/Memory Schematic). C25 on the center tap of the head filters noise that would otherwise be coupled through the head. C23 provides filtering for the bias line (XC9).

2-90. Bias Set

2-91. R9 sets the bias currents for all of the op-amps.

2-92. Tracking Adjust

2-93. R16 is placed in series with the read data coil. It serves two purposes. It reduces wasted current through the read data coil during the write data operation. It also to reduces the relative amplitude of the data track relative to that of the timing track. This is necessary due to many factors, including track width differences, resolution differences, and effects of azimuth differences from HP-75 to HP-75.

2-94. Write Amplifier

2-95. The write coil is center tapped and the tap connects through resistor R9 to VI. During a write operation the coil ends W1 and W2 are alternately pulled to ground through large n-channel transistor switches. R9 sets the write current at 1.5 times the current needed to saturate the card material (VI / R9 = 7.5 ma).

2-96. POWER SUPPLY DESCRIPTION

2-97. DC-to-DC Converter

2-98. The dc-to-dc converter (see figure 2-12) is self-oscillating and alternately stores energy in an inductor and transfers it into capacitors. The energy in the capacitors is used to supply power to the load while the switching circuit begins storing energy into the inductor again. This converter is capable of providing 100 mA to a load at 5.5V with a minimum battery input voltage of 3.3V or of providing 50 mA at 5.5V with an input voltage of 2.5V.

2-99. The principal output voltages are VC and a switchable supply line, VI,that shuts down in the system OFF state called deep sleep to eliminate unneccesary leakage current. The power supply has two modes of operation: deep sleep (SCL high) and awake (SCL low).

2-100. In the deep sleep mode, VI is off and VC is at the battery voltage. This enables the RAM to retain its contents and the logic that is tied to VC to perform all of its normal housekeeping functions while in deep sleep.

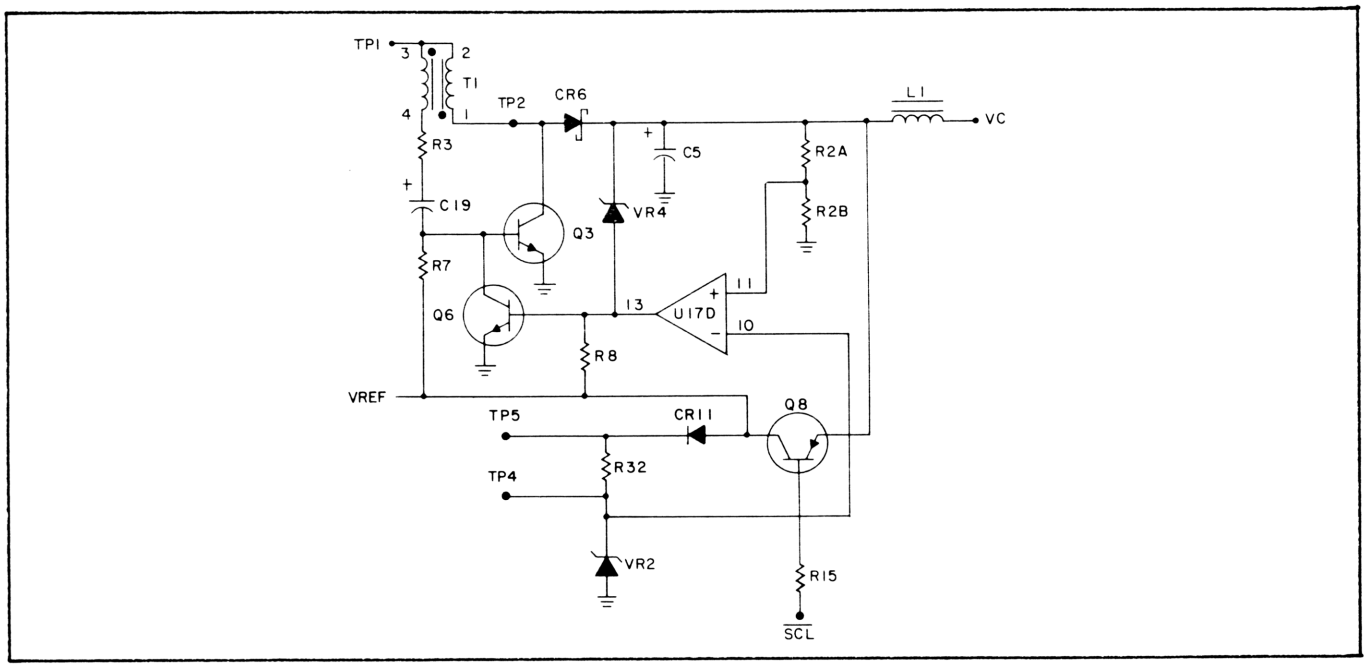


Figure 2-12. DC-to-DC Converter Circuit

2-101. The awake mode is characterized by SCL being held low. From the time SCL is pulled low, the system allows 56 ms for the power supply to bring VC and VI up to specifications (5.2V to 5.5V). When SCL is pulled low, Q8 is turned on and supplies voltage to R7, R8, VR2, and the quadcomparator package (U17). Power to these components is essential for the supply operation.

2-102. While the dc-to-dc converter is in normal operation, the voltage level is controlled by comparing the sense voltage, produced by R2A and R2B, to the reference voltage at VR2. When this sense voltage is above the reference voltage, U17D turns Q6 on, which in turn keeps Q3 turned off by pulling the base of this transistor below 0.6V. Any power required by the system during this period is provided by the capacitance of C5 on the power supply/memory PCA and a total of 253 uF of capacitance from the logic PCA. When this sense voltage drops below VR2, Q6 turns off and the base of Q3 is pulled to 0.6V by R7 and turns Q3 on. The collector of Q3 (and pin 1 of T1) is pulled to about 0.2V. Current then flows through the primary coil of the switching transformer and stores energy. During this time, transformer action forces more current into the base of Q3 from the secondary of T1 to reinforce the turn-on of the transistor. When this base current reaches its maximum (determined by R7, R3, and T1), the voltage across the primary starts dropping, and the secondary starts diverting current from the base of Q3. This transistor then switches off, and the energy stored in the primary of T1 is now transferred into the filter capacitors through CR6. The sense voltage rises due to an increase in VC. The whole process starts over whenever the sense voltage again drops below the reference level.

2-103. The filter capacitors are low-leakage type with the largest value possible to match the diameter restrictions set by the case size and voltage ripple requirements. CR6 is a Schottky diode to reduce the power loss and is used to ensure that the capacitors do not discharge back into the battery or through Q3 to ground during the switching sequence. C3 is used to filter some of the switching noise on the battery to help stablize the battery charging circuit and to supply current in deep sleep when the batteries are removed along with the ac adapter.

2-104. Battery Level Detect

2-105. R1 and C11 form a low-pass filter to reduce switching noise to the BDK line. The BDK line is used for detecting low battery voltage.

2-106. Alkaline/Nicad Detect

2-107. The alkaline/nicad detect circuit enables the HP-75 system to determine which battery pack is in use.

2-108. The BDR line from U2 is tied to the resistor divider formed by R35 on the power supply/memory PCA and R18 on the logic PCA. This divider is pulled between VI (to reduce leakage current) and VN when the alkaline pack is installed. (CR5 is forward biased for this operation.) When BDR is below 0.365V the system uses the LOW BATTERY detect levels assigned for alkaline batteries. When the nicad pack is installed, CR5 is reversed biased (the negative side of the battery is connected to VA) and the voltage on BDR is greater than 0.365V. The nicad low battery detect levels are then used.

2-109. This method enables the HP-75 to take full advantage of the long life of alkalines without losing the advantage of the "LOW BATTERY" abort on nicads. (Nicads have a flat discharge curve with a sharp knee at the end of the battery life.)

2-110. Battery Charging

2-111. By keeping the negative input of comparator U17C at the same voltage level as the divided reference, R2C and R2D, a continuous charge current of 100 mA through the nicad battery is ensured up to a supply load current of about 50 mA. The comparator selects the appropriate gate to source voltage, VGS, of Q2 to control the current in VR1 (see figure 2-13). The VR1 and VB voltages then vary to correct the current through the battery and the sense resistor, R5, thus completing the feedback loop. The gate of Q2 is tied to the anode of VR3 through R11 to provide a maximum current limit in Q2 and VR1 when the batteries are removed. When VGS is at its maximum of 0.5V, the current in the drain of Q2 will be between 12 mA and 35 mA and the power dissipation in Q2 and VR1 will be limited. The 2.2 uf capacitor, C1, is used to stabilize the voltage at the gate of Q2 when the loop is active.

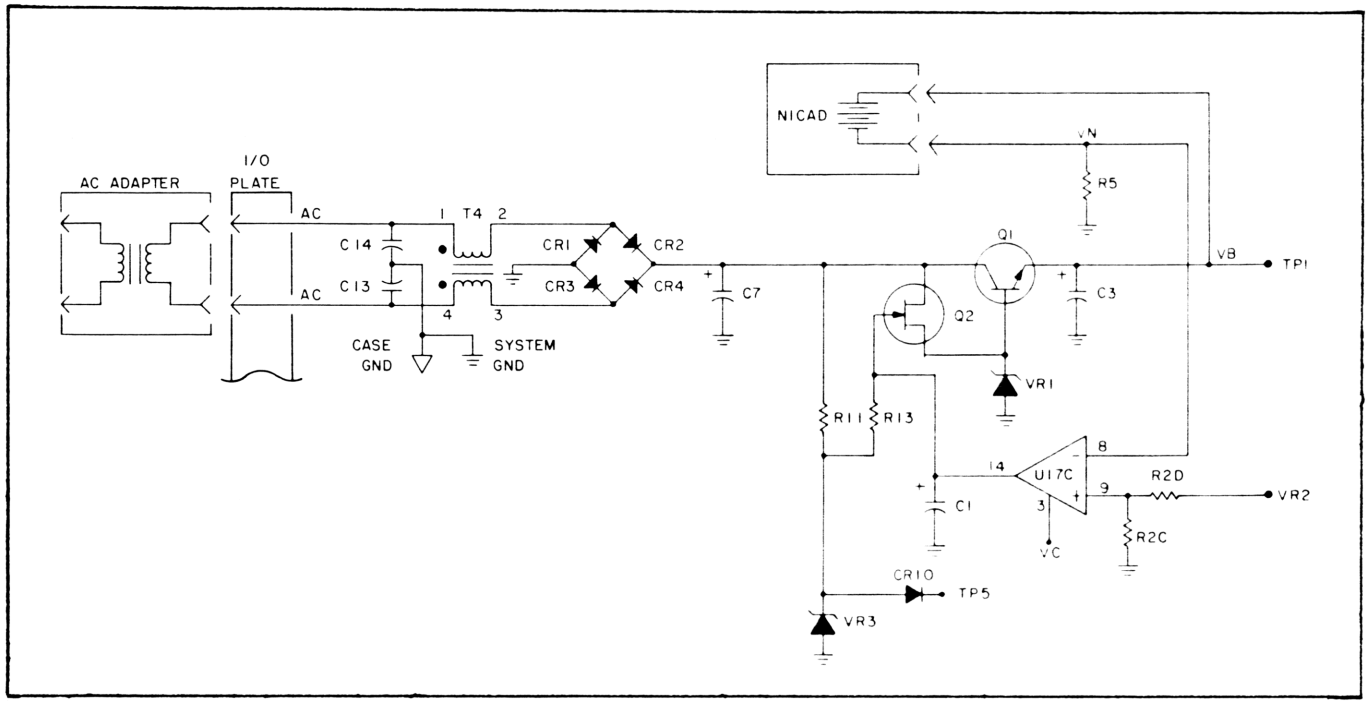


Figure 2-13. Battery Charging Circuit

2-112. The value of the capacitor, C7, was chosen to be as large as possible, and due to the space limitations inside the HP-75, a 330uf 25V capacitor was selected. Under the worst case battery charge operation of 90 Vrms/50 Hz applied to the HP 82059B AC Adapter inputs and maximum load on the switching regulator, the circuit limitation begins to become apparent. This limitation occurs when the minimum voltage across C7 (about 6V) takes Q1 and Q2 out of their linear operating regions and 120 Hz starts to pass through to VB and VC. (The HP 82059B AC Adapter has a designed-in secondary resistance which limits its output voltage under heavy current loads.)

2-113. During deep sleep, VR3 serves two purposes. First, as noted earlier, the 5.11V zener diode serves as the maximum voltage that can be applied to the gate of Q2 since comparator U17 has open collector output stages. Second, the voltage applied to the reference (VR2) and comparator U17C for deep sleep battery charging is regulated by VR3. (In the awake mode of operation, power to the battery charger circuit is provided through Q8.)

2-114. Near the end of the charge cycle, the battery voltage approaches VB's maximum voltage, 4.5V, limited by VR1. This reduces the charge current down to about 30 mA to 80 mA depending on the history of that particular battery. The battery pack is capable of 150 mA continuous overcharge current. The temperature range for battery charging is from 10 to 40 degrees C which is set by the battery pack.

2-115. AC Operation

2-116. The HP-75 can operate on ac only. In this case, since there are no batteries to charge (that is, no current in R5), the gate voltage of Q2 (see figure 2-13) is limited to its maximum by VR3, and VR1 in turn limits VB to 4.5V. All other power supply operations are the same as in battery operation, and power is still applied to the comparators and the reference, VR2, in the deep sleep mode. This is to ensure that when batteries are inserted, they will be charged at all times, even in deep sleep.

2-117. Display Reference Voltages

2-118. The HP-75 liquid crystal display requires three temperature compensated voltage references to keep the viewing cone at its factory preset angle. (See figure 2-14.) Also, since the required voltages may vary from display to display, these voltage references must be adjustable to match the room temperature voltage to the particular display installed in the unit.

2-119. The technique used here is to develop a temperature sensitive resistor divider by dividing down the reference voltage at VR2 with R27 and R20, and paralleling a 100k-ohm negative temperature coefficient thermistor, R26, with R20 at the positive input of the comparator. R9 and R12 set the gain of the network to establish the maximum voltage required for the reference voltage; RV3, RV2, and RV1 are developed by the resistor divider formed with R2F, R2G, and R2H.

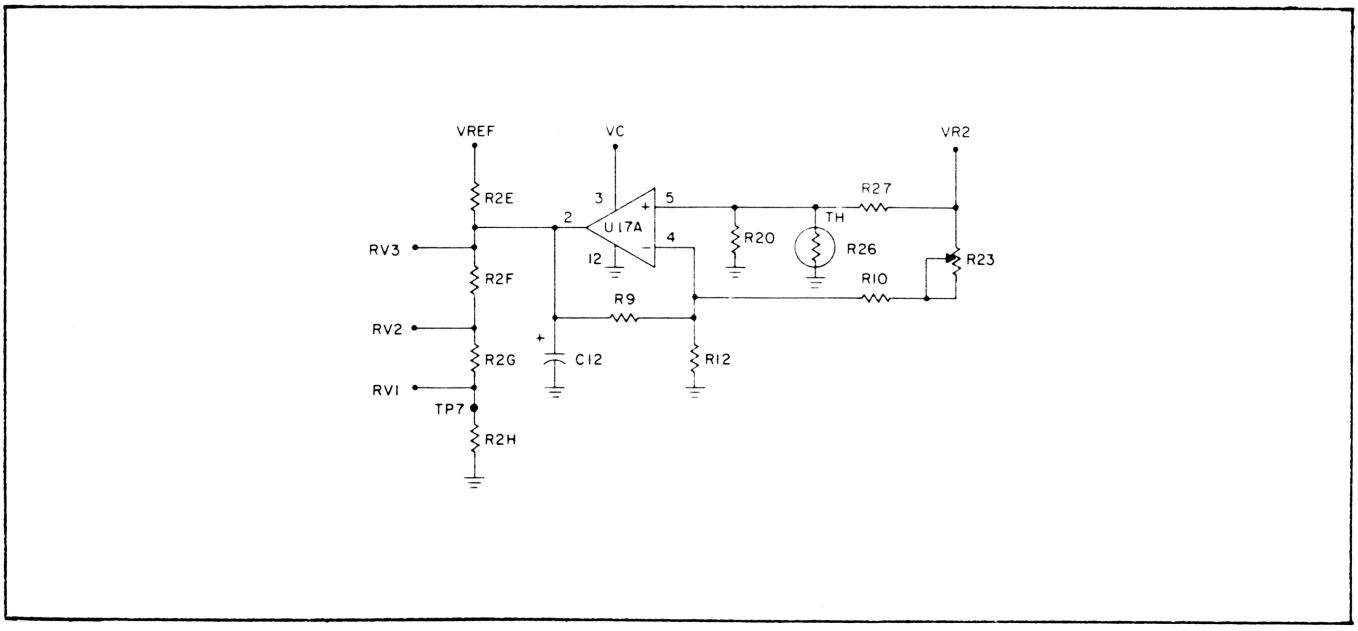


Figure 2-14. Display Reference Circuit

2-120. An adjustable temperature-independent negative voltage is added to RV3 to easily adjust for any display voltage requirements without affecting the shape or slope of the temperature compensation curve. The negative gain is set by R9 and R24 and the adjusted value of the variable resistor, R23. This adjustment actually raises and lowers the viewing cone of the display and thereby makes it easy for the factory to compensate for any display variations.

2-121. Buzz Circuit

2-122. The buzz circuit (see figure 2-15) is designed to eliminate the need for a matching transformer and reduce the power consumption to about 50 mW for the required volume level. This regenerative oscillator operates at approximately 100 kHz during the low half cycle of the applied square wave at the BUZZ input. Since this speaker can reproduce signals up to about 10 kHz, the user only hears the fundamental audio square wave.

2-123. Q4 and Q5 form a direct coupled two stage amplifier with the speaker as the load in the collector of the second stage. The feedback capacitor, C10, provides the regeneration to make this amplifier into a free-running multivibrator. R22 sets the duty cycle, while the speaker's high-frequency impedence combined with the value of C10 determines the frequency of oscillation. When the BUZZ line is pulled low, the circuit is active. Figure 2-16 shows a 1 kHz signal applied to the BUZZ line and the waveform at the base of Q4.

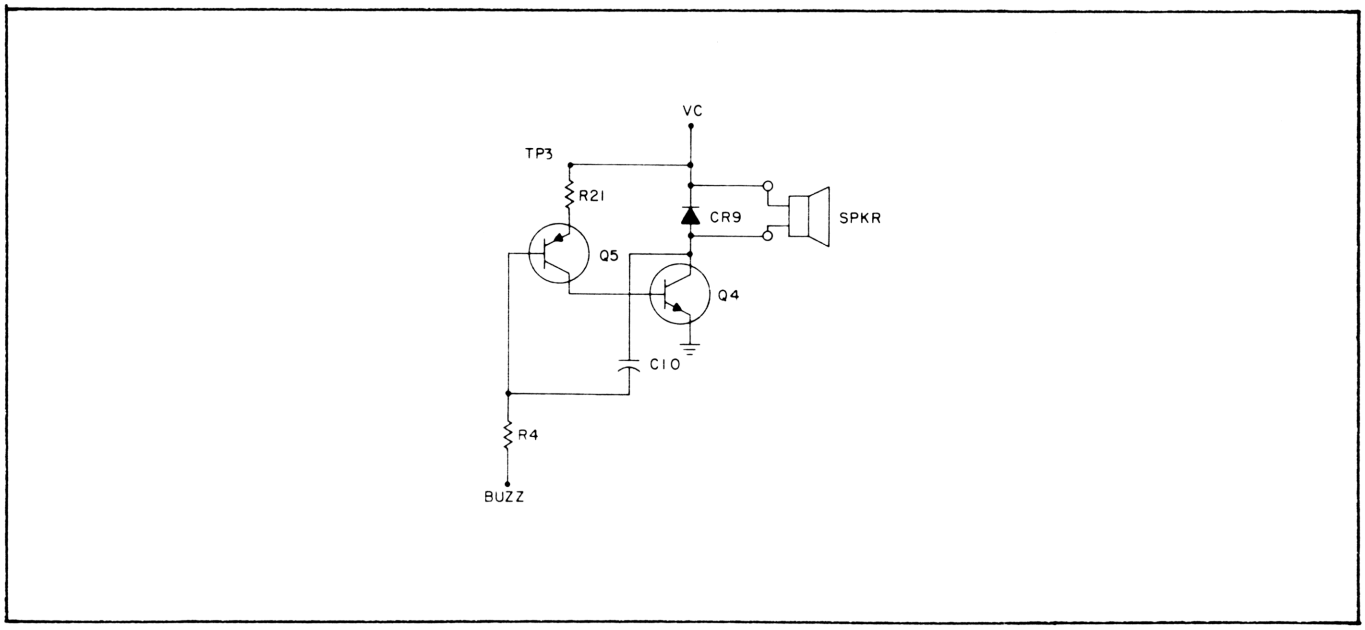


Figure 2-15. Buzz Circuit

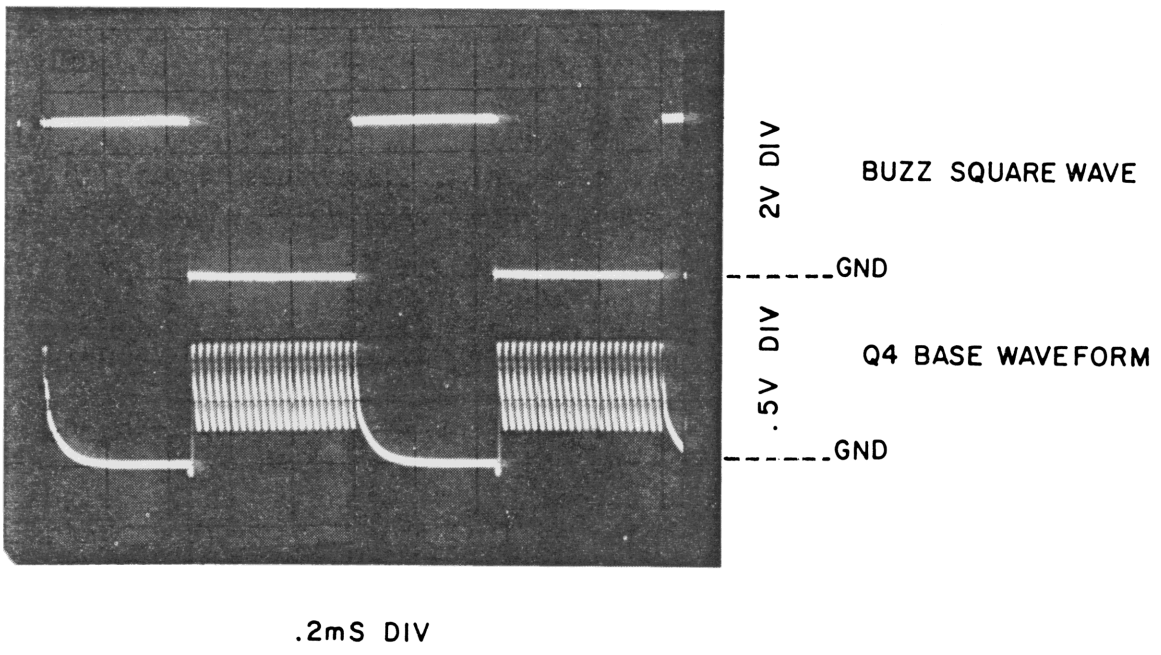


Figure 2-16. Buzz Circuit Waveform

2-124. Automatic Reset Circuit

2-125. An automatic reset on the power supply board is used to avoid any complications that might arise when VI drops below specifications (5.2V) due to IC latch-up (which is usually due to electrostatic discharge, ESD) or battery removal during operation. The resistor divider, R16 and R18, tied to VI forms the sense voltage. The comparator U17B pulls the PWO (power on) line low to reset the HP-75 system when this sense voltage drops below the reference voltage of VR2. This circuit is always active, but any true system reset (PWO pulled low) must occur when PWO is active; that is, when the system is not in the deep sleep mode (greater than 56 ms after SCL is pulled low). This, in effect, masks any reset command seen from this circuit in normal operation when going to deep sleep.

2-126. AC ESD/EMI Protection

2-127. C13, C14, and T4 form the common mode filter used to reduce ac line noise and radiated electromagnetic interference (EMI). Most importantly, this filter protects the unit from electrostatic discharge (ESD) to the ac adapter wire.

2-128. The values of C13 and C14 are small enough to not have a significant affect on the ac input voltage. T4 essentially presents no apparent inductance to ac, but for a common mode signal such as ESD or line noise, the transformer presents approximately 500 uH. This inductance along with capacitance of C13 and C14 form a low pass filter which effectively reduces noise from entering and leaving the HP-75 electronics. The ground for this filter is connected to the shield through a metal spacer.

2-129. SYSTEM TIMING

2-130. The HP-75's timing consists of three states. These are deep sleep, light sleep, and awake modes. U2, the clock/keyboard/RTC IC, generates a two-phase clock, PH1 and PH2, which is used by the CPU and peripheral ICs for data and control synchronization. All control signals (LMA, RD, WR) are valid during PH2. All data on the CPU bus is valid during PH1. PH1 and PH2 have a nominal frequency of 611 kHz during the awake mode. During light sleep the clock frequency is approximately 4.68 kHz. There are no clocks during deep sleep.

2-131. The HP-75 uses a 32.768 kHz quartz crystal for reference with the real time clock (RTC). U2 uses this frequency as a time base in a phase lock loop (PLL) clock generator. This PLL multiplies the 32.768 KHz clock by 112 to create a 3.67 MHz signal. During awake mode the 3.67 MHz clock is used in the clock generator and divided by 6 to become the 611 kHz system clocks. In light sleep, the 32.768 kHz clock is divided by 7 to generate PH1 and PH2. Whenever U2 is being read by the CPU, the 3.67 MHz clock is divided by 7 to allow the IC to have more time to get data to the processor. The timing relationships are shown in figure 2-17 and the clock control block diagram is shown in figure 2-18.

2-132. Deep Sleep With POR Low

2-133. This state is the initial state of the HP-75 before any batteries are inserted. It can also be reached by allowing the machine to discharge the internal capacitor by removing the batteries and recharger. Internal to the computer there is a power fail circuit. If the power supply drops below specification the machine will reset into this initial state. The HP-75 is also reset when the PWO line is pulled low while the machine is in light sleep or awake mode. Pressing [SHIFT] [CTL] [CLR] for five seconds will cause a reset to occur regardless of the state of the HP-75.

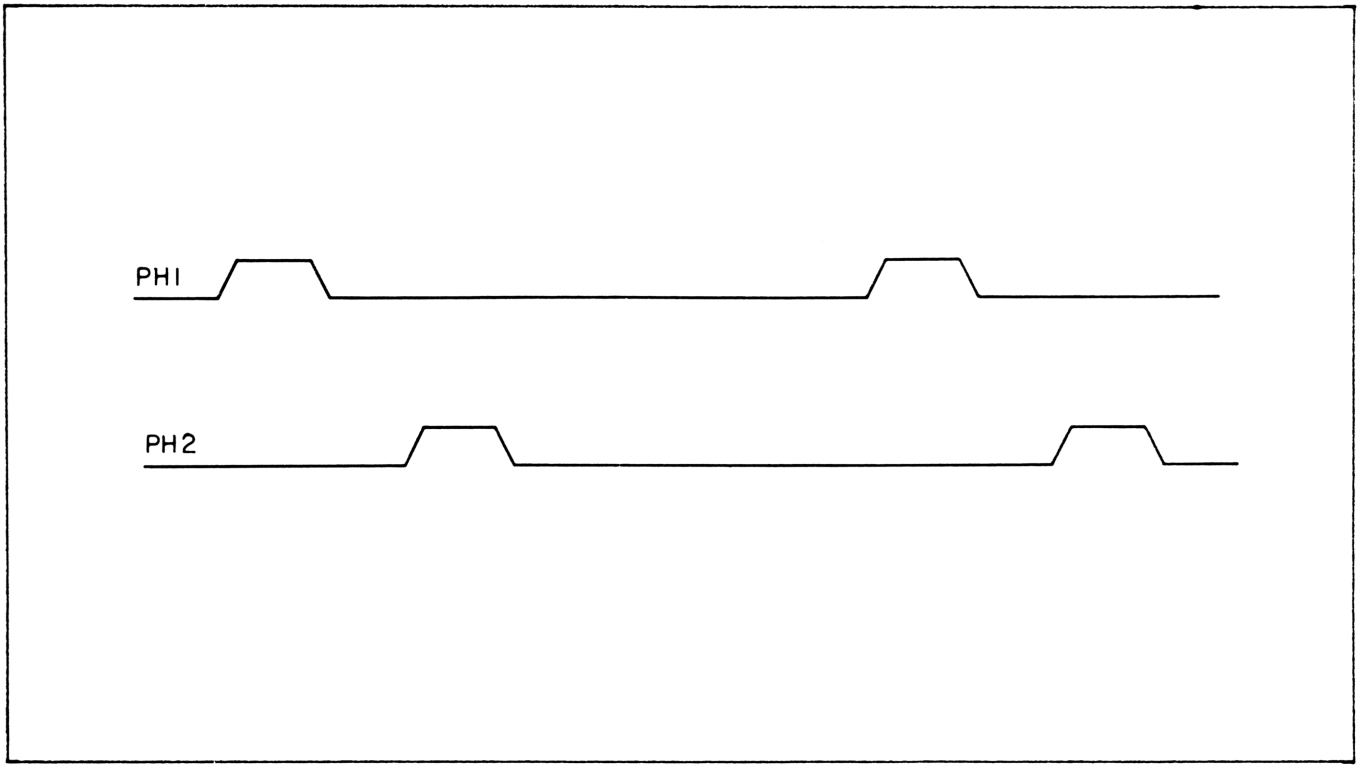


Figure 2-17. PH1 and PH2 Awake Timing

2-134. The characteristics of this state are:

- The POR flip-flop in U2IC is reset.
- No clocks are output to the system (both are at ground).
- The PWO output is low.
- The SCL output is high.
- The low-frequency oscillator is on and the real time clock (in U2) is incrementing.
- The PLL is off as is the clock generator.
- The global interupt is disabled.
- The buzzer output is high.
- Power (VC) is supplied to U2, RAM, MAR, and buffer ICs only.

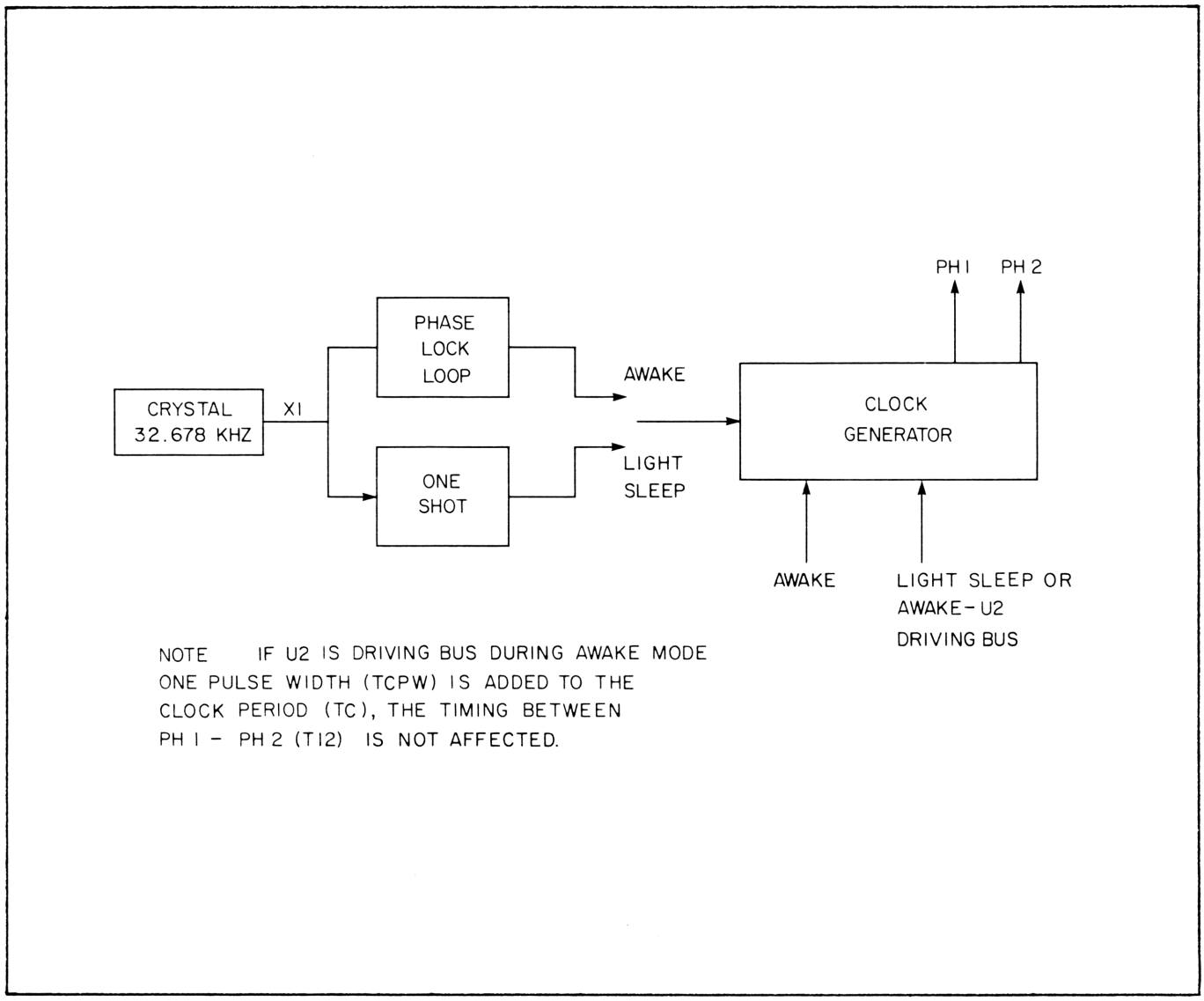


Figure 2-18. Clock Control Block Diagram

2-135. Deep Sleep With POR High

2-136. This state is the normal deep sleep state of the HP-75. During this state the contents of the RAM are saved, thus providing continuous memory. This state is reached when the CPU instructs U2 to put the system to deep sleep.

2-137. The characteristics of this state are the same as POR low with the following exceptions: the POR flip-flop is set to one and a comparator interrupt can wake up the system.

2-138. Light Sleep

2-139. This state is the idle state of the HP-75. During this state all power is supplied to the ICs in the machine. However, the clock frequency is reduced to 4.68 kHz to reduce the amount of power consumed. This state is reached when the processor instructs U2 to go into the light sleep state.

2-140. The characteristics of this state are:

- The POR flip-flop is set to one.
- The clock outputs are in the low frequency (4.68 kHz) mode.
- PWO is high.
- SCL is low.
- The clock generator is always in skip mode (divide by 7).
- The PLL is on but the HF clock output is not used, and the keyboard is active.

2-141. Awake

2-142. The awake state is the normal operating state of the HP-75 computer. During this state all programs are run and all interrupts processed. This condition is reached any time the system is instructed to wake up either by keyboard entry or comparator interrupt. Power is supplied to all ICs and circuits.

2-143. The characteristics of the awake state are:

- The POR bit reflects the previous state and should be reset before exiting the awake mode.
- During awake the clock outputs are in the high frequency state (611 kHz).
- The keyboard is active.
- PWO is high and SCL is low.
- The crystal oscilliator is on and the RTC is counting.
- The PLL is on and the clock generator isusing the 3.67 MHz clock as an input.
- Unless U2 is being read, the clock generator is in the divide by 6 mode.

2-144. CPU Control Signal Timing

2-145. The CPU controls external ROM, RAM and I/O ICs using three control signals. Each combination indicates whether address or data information is on the bus and who should be driving the bus during that cycle. The CPU controls these three lines unless a DMA has been granted to some other controller. Table 2-2 has a description for each possible combination of the three control signals. LMA, RD, and WR are valid during PH2. Control line timing is shown in figure 2-19.

Table 2-2. CPU Control Signals

LMA	RD	WR*	Bus Activity
1	1	1	NOP. No activity is occuring and the bus is floating.
1	1	0	Write. The bus data is being written into the previously addressed location on the rise of PH1.
1	0	1	Read. The contents of the previously addressed location are placed on the bus gated by PH2 and valid through PH1
1	0	0	DMA Grant. In response to the halt line going low, the CPU issues this signal and proceeds to float the control lines and bus. This allows a dma device to control the bus.
0	1	1	LMA. One byte of a two byte address is on the bus. It is to be loaded into each ICs address register during PH1.
0	1	0	Never will occur in functional working unit.
0	0	1	LMA While Reading. The contents of a previously addressed location is placed on the bus and used as one byte of a two byte address. This address is to be loaded into every ICs address register during PH1. This includes the IC that sends the address.
0	0	0	Int/Ack (interrupt acknowledge). In response to the CPU's IRL line going low, the controller issues this control signal configuration to tell the interrupting IC to place its 8 bit address on the bus.

*LMA = load memory address/RD = read/WR = write/1 = false (high logic level)/0 = true (low logic level)

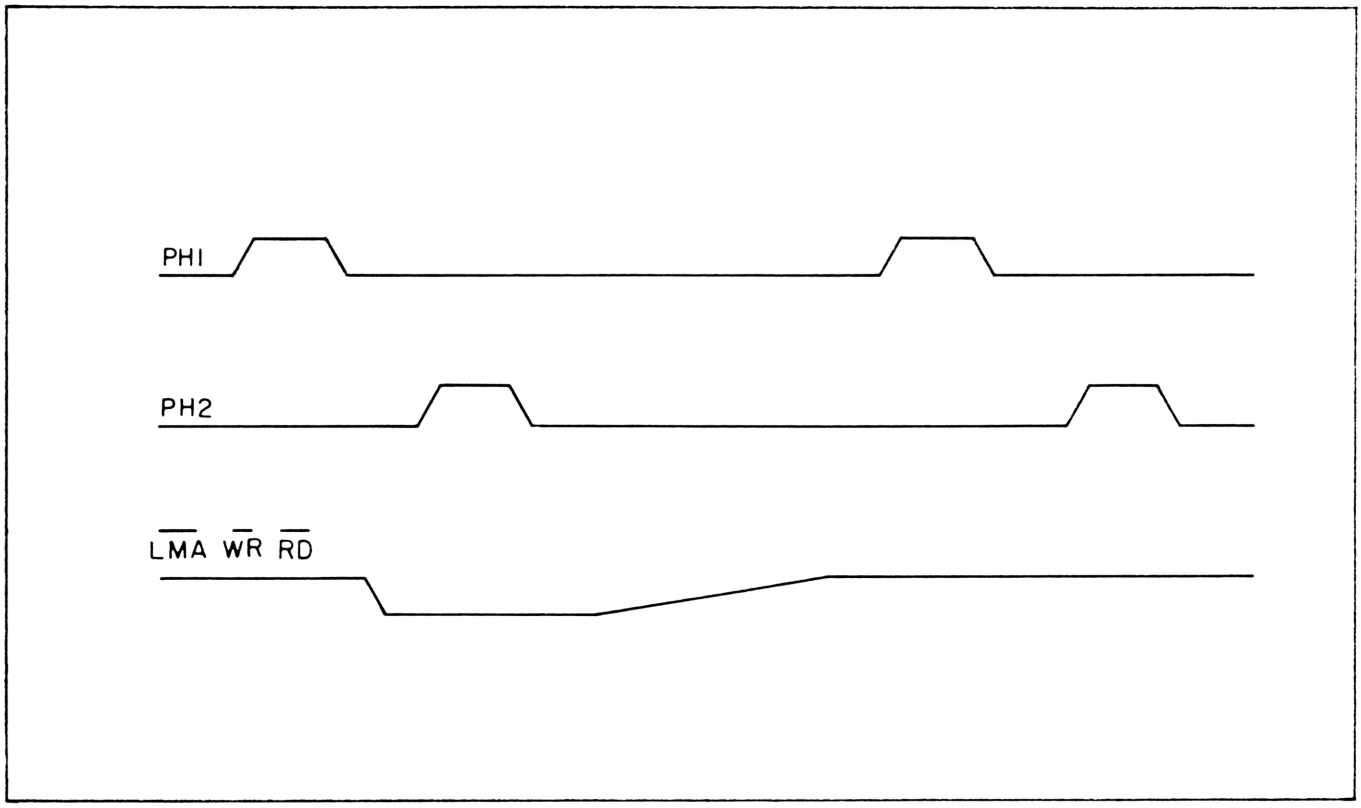


Figure 2-19. Control Line Timing

2-146. Direct Address Loading

2-147. In direct address loading all addresses are sent out by the CPU and are shipped as two bytes. Using the LMA signal as control, the two bytes are transferred in pairs. Refer to figure 2-20 for the timing information.

2-148. Within 350 ns from the time that PH1 goes high, the LMA control line goes low and will remain low during the next PH2 and then rise back to a high level within 800 ns after the fall of PH2. During PH2 the CPU begins to send the first byte of the address (lower 8 bits) which becomes valid on the data bus 600 ns after the fall of PH2. All memory and peripheral circuits will accept the address during PH1. At this time the CPU again pulls LMA low during PH1 and again is valid after 350 ns from the rise of PH1. The next byte of the address (higher 8 bits) is sent during PH2 and the control line is released to return high after PH2 goes low. Again the information on the data bus is valid within 600 ns after PH2 fall and the LMA control line returns high within 800 ns. After this sequence occurs, the external electronics have the present address and are waiting for the next control from the CPU.

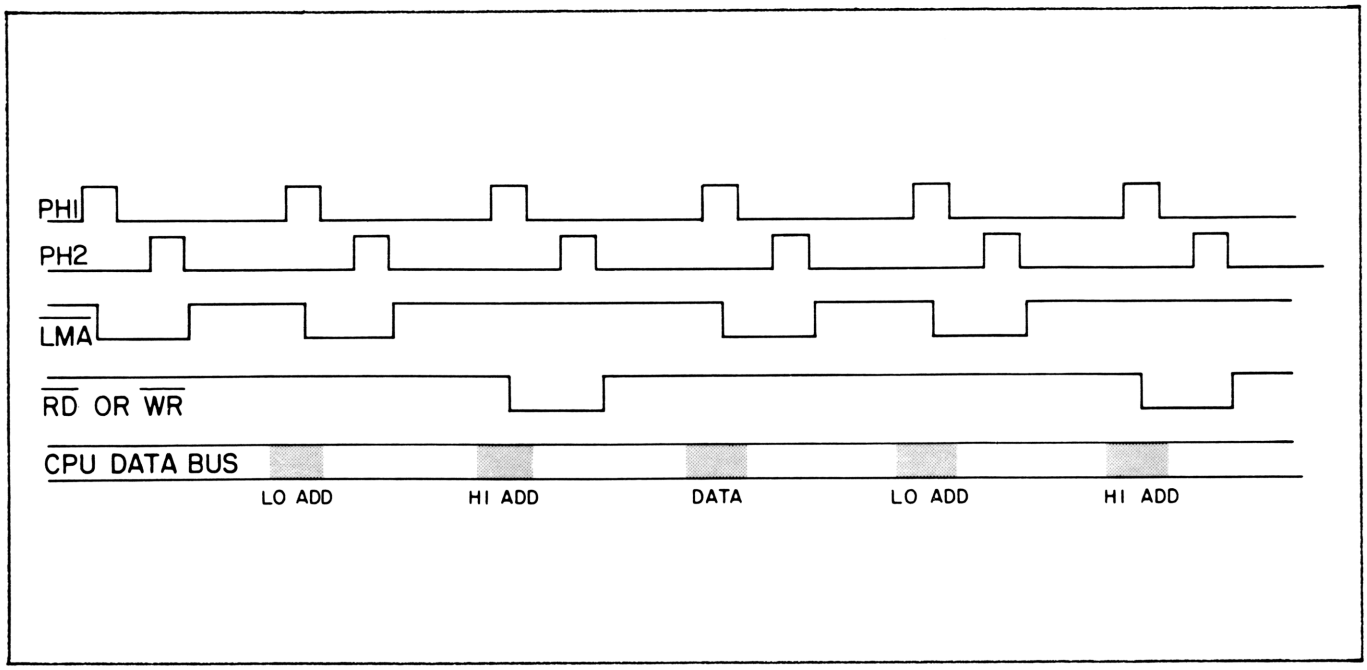


Figure 2-20. LMA Direct Address Timing

2-149. Reading

2-150. The CPU can execute a read command by pulling the RD control line low. When this happens, the RD line begins to go low during PH1 and becomes valid 350 ns after the fall of PH1. The signal remains low during the next PH2. The external circuit being addressed will begin to send data to the CPU via the data bus after PH2 rises. The data will then have to be valid 225 ns before the rise of PH1, remain valid during PH1, and stay valid for at least 40 ns. If the CPU wishes to read the next consecutive address in memory then the external MARs will increment their address registers after PH1 fall and repeat the previous cycle. Refer to figure 2-21 for timing reference.

2-151. Writing

2-152. After the CPU has output a direct address load, it may want to write information to that address. In that case, the WR control line is sent low during PH1 becoming valid within 350 ns from the rise of PH1 and remaining valid during PH2 and must return high within 800 ns after the fall of the PH2 clock. The CPU will begin to send the data on the bus during PH2 and the bus becomes valid 600 ns after PH2 falls. The data remains valid during PH1 and for at least 40 ns after the fall of PH1. The external circuits accept the data and increment their address pointers in case the CPU wishes to issue another write command. Refer to figure 2-21 for timing information.

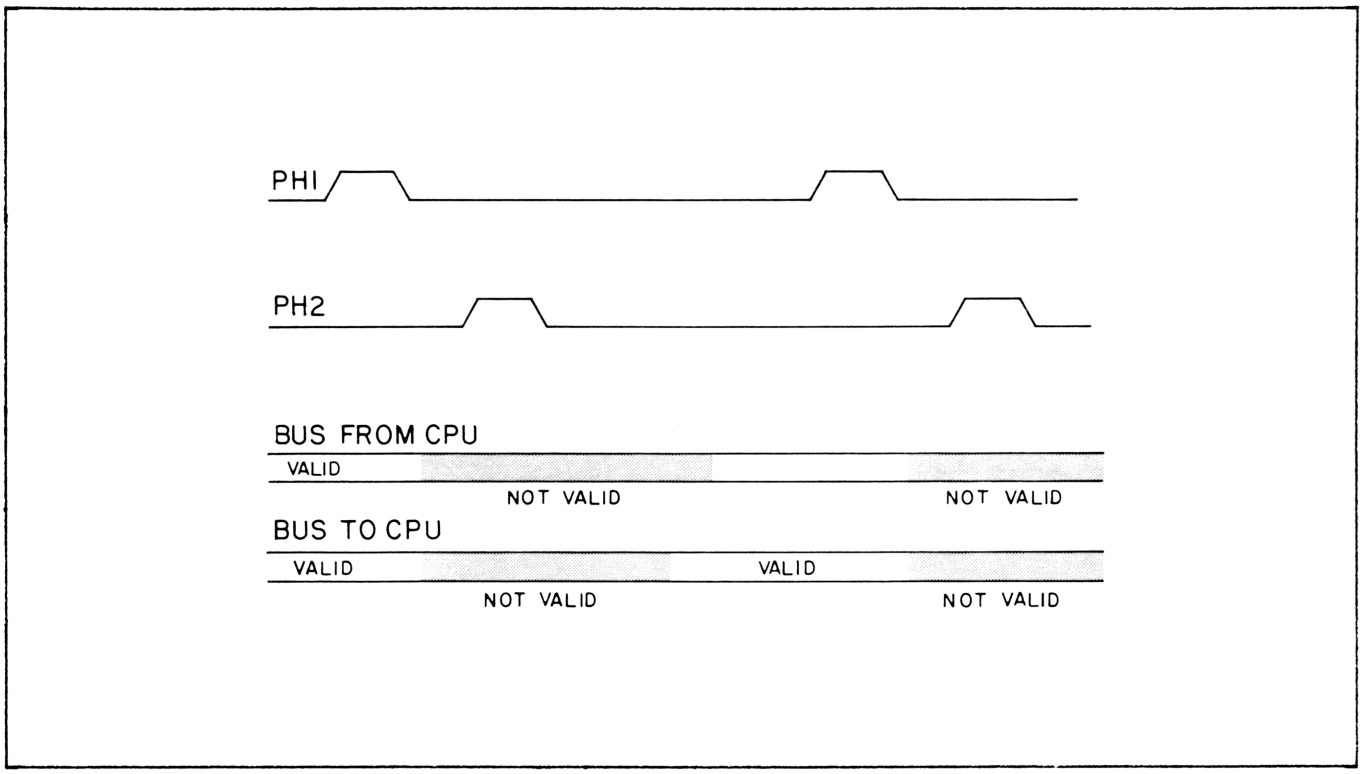


Figure 2-21. Data Read/Write Timing

2-153. Indirect Address Loading

2-154. Sometimes the CPU wants to jump to an address that is stored in two memory locations. This can be accomplished easily with the HP-75 CPU and its control lines. During PH1 both the RD and the LMA lines go low, becoming valid within 350 ns from the rising edge of PH1. This combination of control signals tells the external memory to place the currently addressed location's contents on the bus during PH2, and for all circuits to accept this data during PH1 and load it into its address register. The CPU then issues another RD and LMA combination which ocurrs as before during PH2 and the second byte of data is placed on the bus. Refer to figure 2-22 for the correct timing information.

2-155. Halt/DMA (Direct Memory Access)

2-156. The HP-75's CPU has the capability of being halted. When this action occurs, the CPU finishes the current instruction, places the program pointer on the stack and floats both the data and control buses. At this point the CPU just idles waiting for the HALT line to be released. This allows another controller to take over driving the CPU bus and control lines. This provides a crude method of direct memory access. (The HALT line is also used with the test signal and the Diagnostic ROM for signature analysis.)

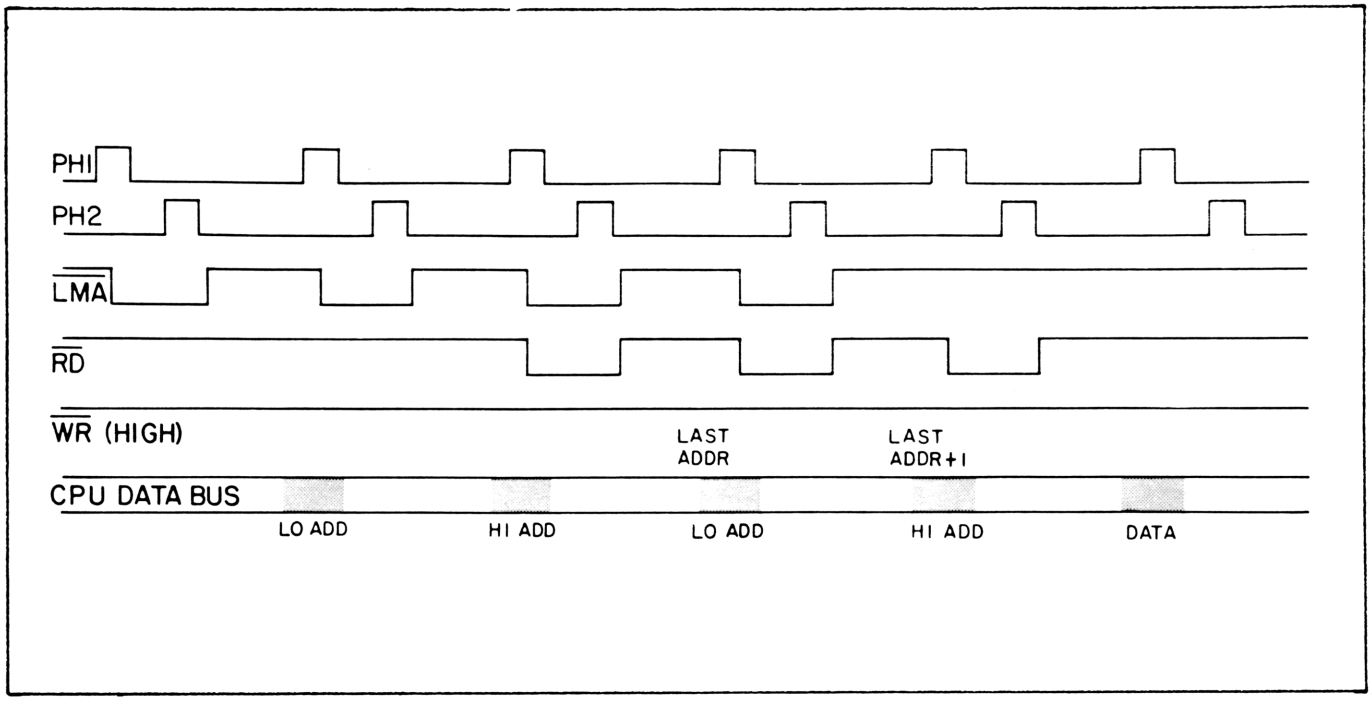


Figure 2-22. Indirect Address Timing

2-157. The HALT line should be gated with PH2 to insure proper operation. It can be pulled at any time but it is possible that the CPU might perform one additional instruction than wanted. The HALT line is brought out to the third port.

2-158. Interrupt Structure

2-159. The HP-75 computer's CPU allows for a priority interrupt structure. Since the CPU has only one line by which to detect an interrupt, all interrupting ICs IRL signals are hardwired together. The priority of when an IC can interrupt is determined through a daisy chain structure. This method is implemented with each interruptable IC having an input line PRIH and an output line PRIL. PRIH of the highest priority device is tied high. PRIL of the lowest priority device is left unhooked. The priority structure is shown in figure 2-23.

2-160. If a device has an interrupt request, it drops its PRIL at PH1. The time between PH1 and PH2 is used to determine the highest priority IC with and interrupt request. At PH2 the higher priority IC pulls the IRL line low.

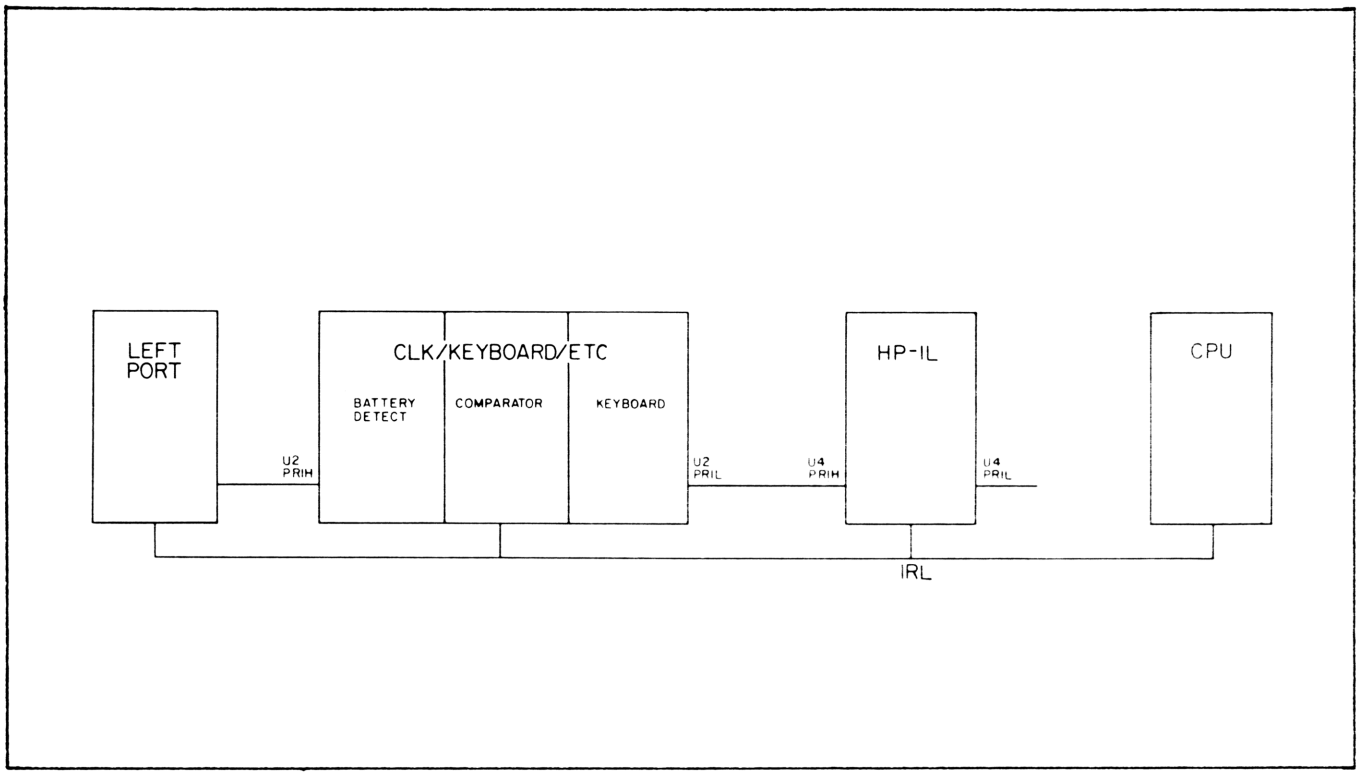


Figure 2-23. Priority Structure

2-161. After executing the current instruction, the CPU saves the return address on top of the stack and issues an acknowledge signal (LMA, WR, and RD are false) for one cycle, during this cycle the interrupting device is expected to put a pointer to the starting address of its service routine on the bus and release IRL. A second LMA with all "0"s on the bus is then output by the CPU completing the two byte address. Figure 2-24 shows the interrupt timing.

2-162. Power On Sequence

2-163. The power on (PWO) input to the CPU originates from U2. During deep sleep the PWO signal is low. Upon awaking the system, either by the [ATTN] key or comparator interrupt, SCL (U2) goes low telling the power supply to begin coming into range. U2 waits for 56 ms before generating clocks. After the PH1 and PH2 clocks have been up for 8 ms, the U2 circuit pulls the PWO line high, which signals the CPU to begin processing information.

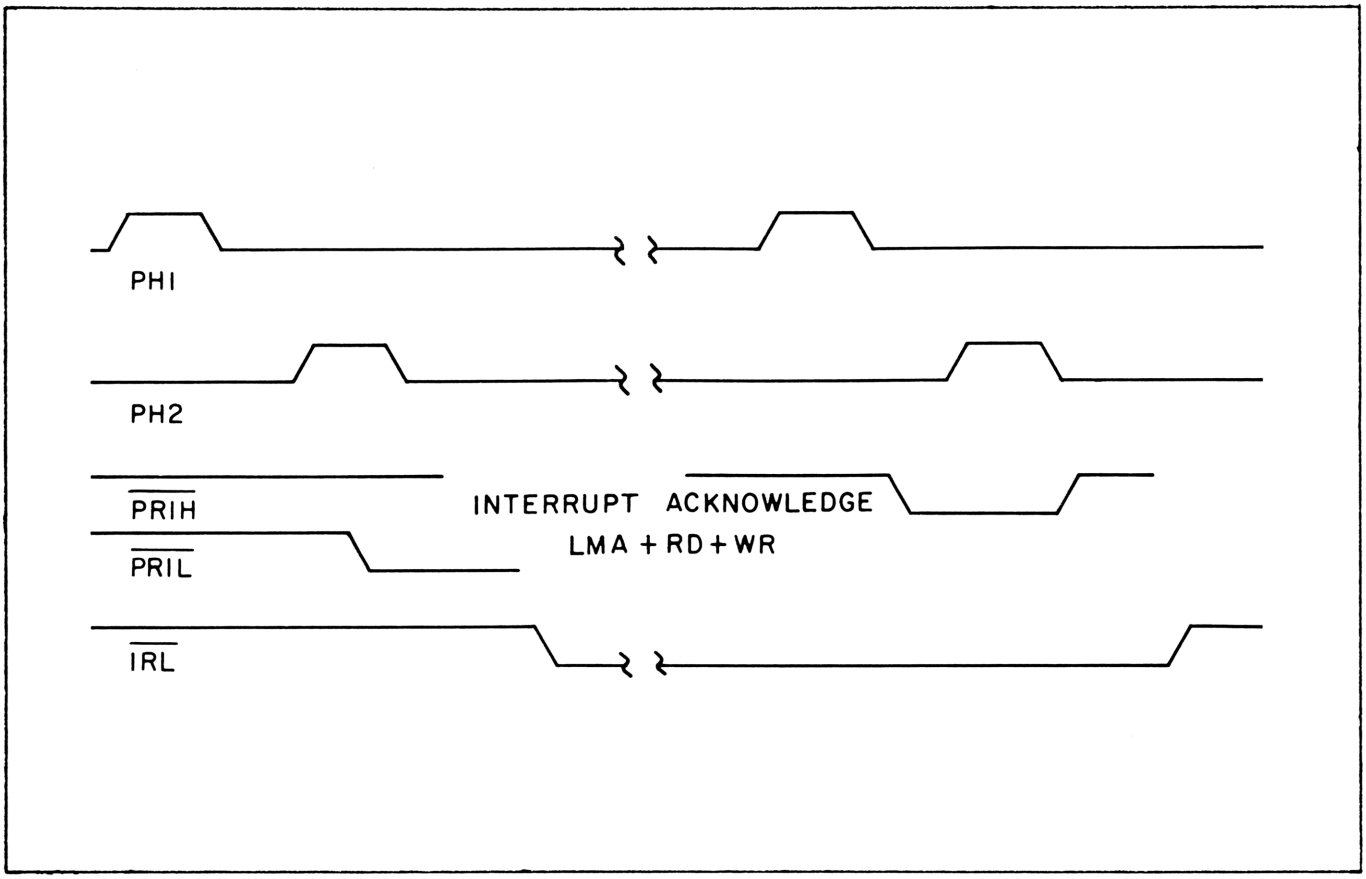


Figure 2-24. Interrupt Timing

2-164. While PWO is low, the CPU inhibits bus driving, clears its program counter, clears its state register, and waits for the signal to rise. The control lines are driven high during this period and the IF signal will be low. All internal status flags and registers are not preset by PWO and, therefore can come up in any random state. They should be initialized by the programmer before use.

2-165. It is expected that the entire system will be ready when PWO goes high. This means that other ICs must recognize the control lines. Three cycles after the PWO goes high, the CPU will issue two LMA's with all zero's on the bus, followed by two LMRD's. The result is that the contents of locations 0 and 1 are placed on the bus and loaded into each ICs address register. The CPU then issues a RD command requesting the first instruction of the power on routine. Figure 2-25 illustrates the power on sequence.

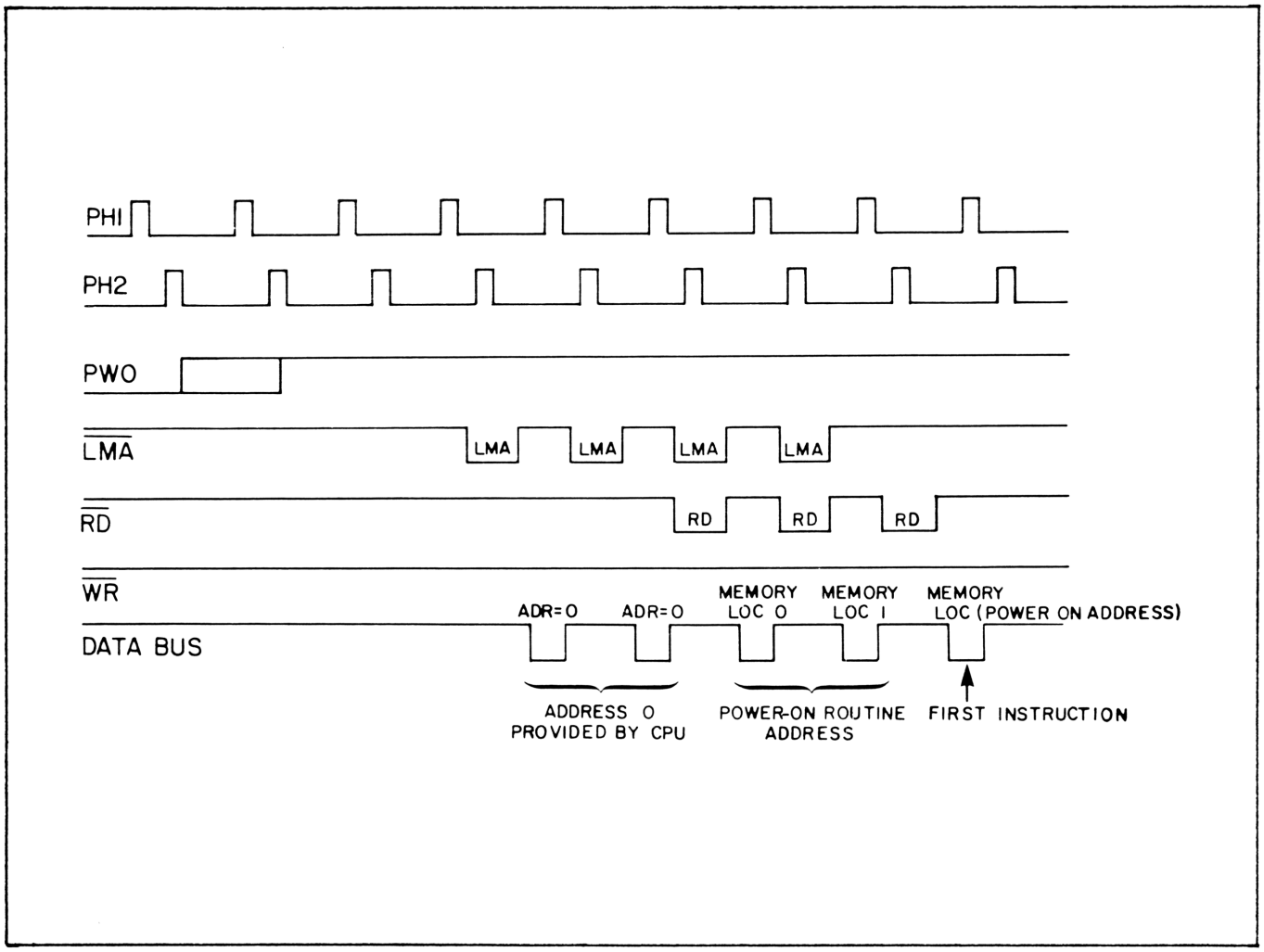


Figure 2-25. Power On Sequence

2-166. Test

2-167. The test line in the HP-75 is used for testing and troubleshooting. The signal was implemented to allow signature analysis on the bus lines. This line can be toggled through the use of I/O addresses. The two addresses used are FFAA and FF55. FFAA causes the test pads to go high and must be valid within 200 ns of the next occuring PH1. FF55 causes the test pads to go low and also must be valid 200 ns before PH1. Refer to figure 2-26 for timing information. The TEST signal from ROM U13 is brought to the third port along with the HALT line.

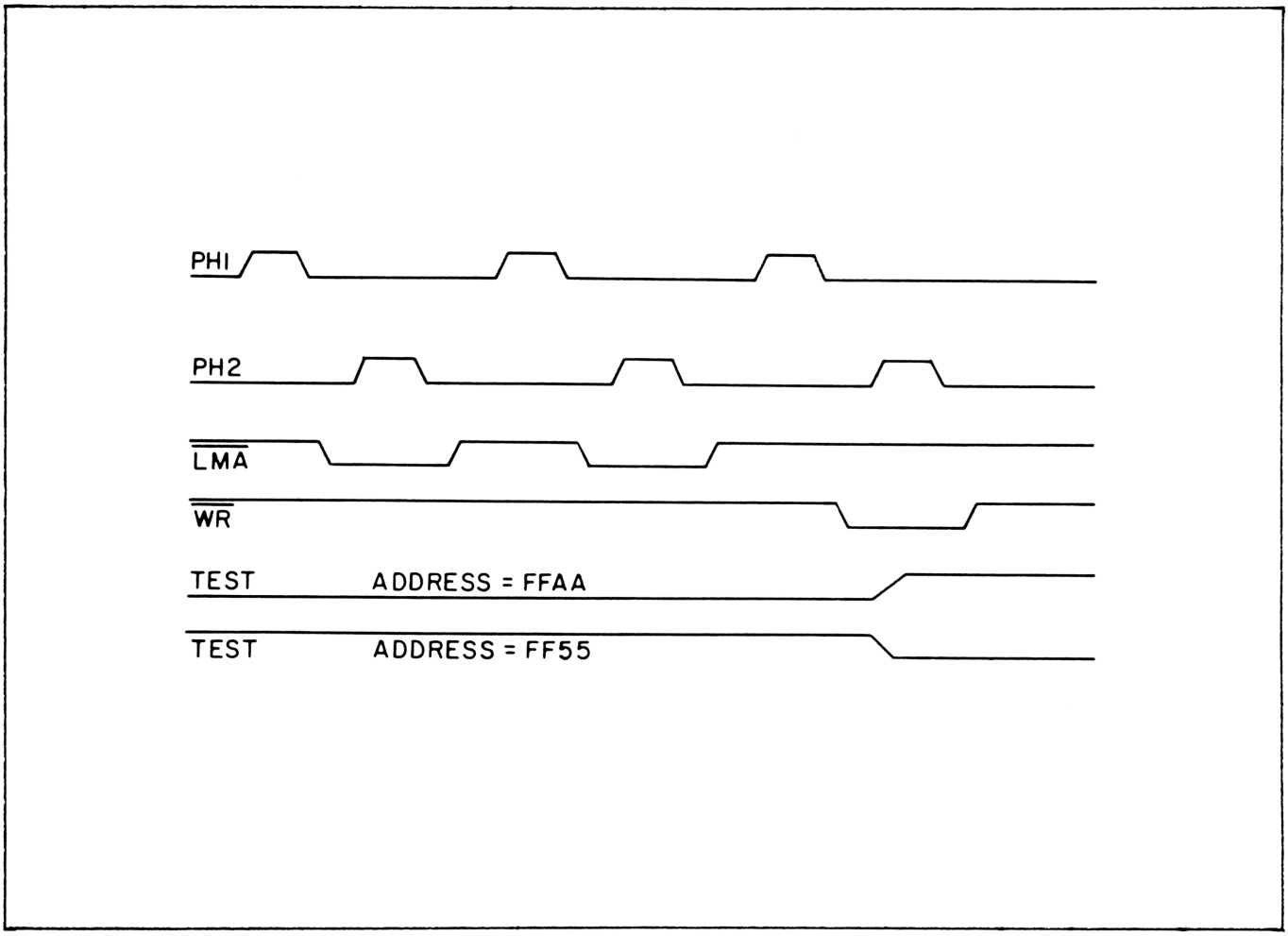


Figure 2-26. TEST Line Timing

2-168. HP-75 MEMORY ORGANIZATION

2-169. The HP-75's CPU has the capability of directly addressing 65,536 bytes of memory. This memory space is partitioned for various uses. The lower bytes are used for power on and interurrupt service routine vector addresses. The upper 256 bytes are reserved for use with I/O circuits. Through the use of the I/O capability, memory can be expanded indefinitly and the machine functions can be increased. Refer to figure 2-27 for the HP-75 memory organization structure.

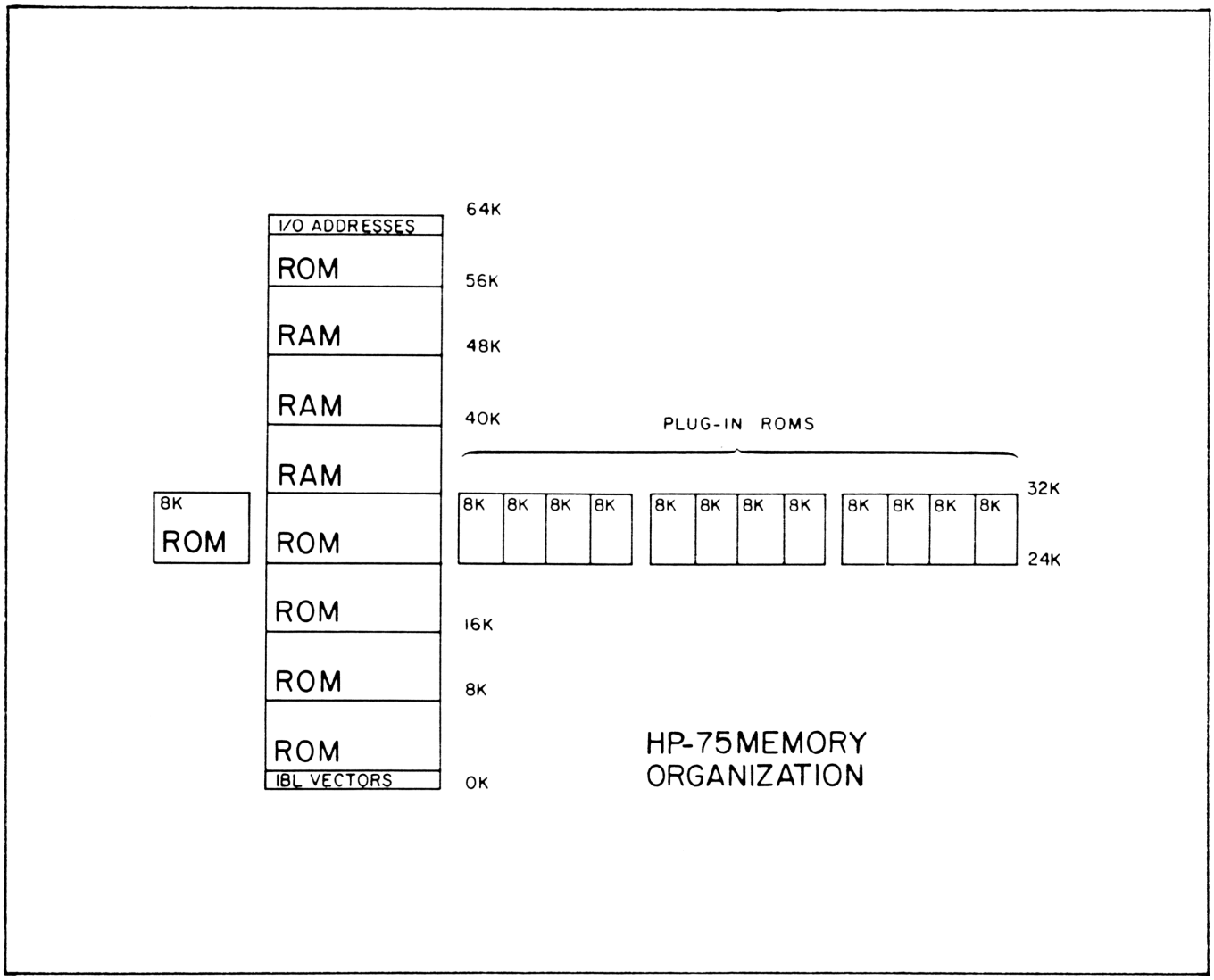


Figure 2-27. Memory Structure

2-170. ROM and ROM Plug-in Modules

2-171. The HP-75 base machine has 48K of system ROM. It occupies the 0K to 32K and the 56K to 64K memory space. 8K of the system ROM is physically mapped into the same space as another 8K at the 24K to 32K locations. This extra ROM is powered on disabled but may be swapped with the other ROM which comes on enabled. This 8K of ROM swap space enables the system to expand the amount of ROM avalable for use. Up to 144K of extra ROM may be added to the HP-75 bringing the total available ROM to 96K bytes. The ROMs are switched in and out of this space through the use of I/O addresses. First the enabled ROM is switched out and then the next ROM is turned on. The HP-75 software determines the protocol for switching ROMs in and out.

2-172. RAM and the 8K Plug-in Memory Module

2-173. Up to 24K bytes of memory space is available for RAM. The HP-75C has 16K of RAM in the base machine and is expandable to 24K with an 8K plug-in memory module. (Other RAM extensions may be added to the HP-75 through the use of the plug-in modules. These would not be directly addressed by the CPU.) The system software supports RAM increments in 2K intervals allowing for RAM configurations other than 16 or 24K.

2-174. I/O Address Space

2-175. The upper 256 (FFXX) bytes of the CPU's memory are reserved for I/O addresses. These addresses are not incremented after a read or write. The CPU issues the I/O address and then can send or read 1 to 8 bytes of data at the I/O address. Not all I/O addresses act the same. Some are used to set or read status while others are used to transfer data. It is through the use of the I/O addresses that the CPU talks to U1, U2, U4, U5, and switches the plug-in ROMs in and out. Refer to table 2-3 for a list of the I/O addresses.

Table 2-3. I/O Addresses

Hex	Octal	Access	Description
Interrupt Vector Addresses			
0 & 1	0 & 1	Read	Power on routine
2 & 3	2 & 3	Read	21mx service routine
4 & 5	4 & 5	Read	Keyboard service routine
6 & 7	6 & 7	Read	HP-IL service routine
8 & 9	10 & 11	Read	Comparator service routine
A & B	12 & 13	Read	Barcode service routine
C & D	14 & 15	Read	Power detect service routine
E & F	16 & 17	Read	Spare service routine
10 & 11	20 & 21	Read	Spare service routine
I/O Device Addresses			
FF00	177400	Write	Global interrupt enable
FF01	177401	Write	Global interrupt disable
FF02	177402	Write	Keybaord status
FF08	177410	Read/Write	Card reader status and data

Table 2-3. I/O Addresses (Continued)

Hex	Octal	Access	Description
FF10	177420	Read/Write	HP-IL status
FF11	177421	Read/Write	HP-IL control/interrupt
FF12	177422	Read/Write	HP-IL data
FF13	177423	Read/Write	HP-IL parallel poll
FF14	177424	Read/Write	HP-IL loop address
FF15	177425	Read/Write	HP-IL scratch pad
FF16	177426	Read/Write	HP-IL scratch pad
FF17	177427	Read/Write	HP-IL auxiliary
FF30	177460	Write	Enable plug-in ROM 1C
FF31	177461	Write	Disable plug-in ROM 1C
FF32	177462	Write	Enable plug-in ROM 2C
FF33	177463	Write	Disable plug-in ROM 2C
FF34	177464	Write	Enable plug-in ROM 3C
FF35	177465	Write	Disable plug-in ROM 3C
FF36	177466	Write	Enable plug-in ROM 4C
FF37	177467	Write	Disable plug-in ROM 4C
FF38	177470	Write	Enable plug-in ROM 1D
FF39	177471	Write	Disable plug-in ROM 1D
FF3A	177472	Write	Enable plug-in ROM 2D
FF3B	177473	Write	Disable plug-in ROM 2D
FF3C	177474	Write	Enable plug-in ROM 3D
FF3D	177475	Write	Disable plug-in ROM 3D
FF3E	177476	Write	Enable plug-in ROM 4D
FF3F	177477	Write	Disable plug-in ROM 4D
FF40	177500	Write	Enable plug-in ROM 1A
FF41	177501	Write	Disable plug-in ROM 1A
FF42	177502	Write	Enable plug-in ROM 2A
FF43	177503	Write	Disable plug-in ROM 2A
FF44	177504	Write	Enable plug-in ROM 3A
FF45	177505	Write	Disable plug-in ROM 3A
FF46	177506	Write	Enable system ROM 3
FF47	177507	Write	Disable system ROM 3
FF48	177510	Write	Enable plug-in ROM 1B
FF49	177511	Write	Disable plug-in ROM 1B
FF4A	177512	Write	Enable plug-in ROM 2B
FF4B	177513	Write	Disable plug-in ROM 2B
FF4C	177514	Write	Enable plug-in ROM 3B
FF4D	177515	Write	Disable plug-in ROM 3B
FF4E	177516	Write	Enable system ROM 4B
FF4F	177517	Write	Disable system ROM 4B

Table 2-3. I/O Addresses (Continued)

Hex	Octal	Access	Description
FF55	177525	Write	All IC test lines go low
FF80	177600	Read/Write	Comparator status/5 data bytes
FF81	177601	Read/Write	Real time clock status/5 data bytes
FF82	177602	Read/Write	Power detect status/DAC data
FFAA	177652	Write	All IC test lines go high
FFFC	177774	Read	LCD display controller status
FFFC	177774	Write	LCD display controller 2 data bytes

2-176. HP-75 SYSTEM SOFTWARE DESCRIPTION

2-177. The CPU receives and executes its commands from information stored in memory. This information is known as the machine software. The software must provide a flow of operation by which it can enter and exit the different hardware states of the machine. The following outlines show the basic flow of what the computer does as it wakes up from deep sleep, waits for key entry, and goes to sleep.

2-178. Power On

2-179. Upon waking up from deep sleep, the HP-75's clocks are in full awake mode (high speed). The HP-75 software performs the following sequence of events. First the software clears the LCD display and then checks to see if the Diagnostic Module is in port 3. If the Diagnostic Module is there the software transfers control of the machine to the module. If the module is not there, then the system checks to see if the POR bit of U2 is set. This bit determines whether the CPU performs a coldstart or a warmstart. If the bit is reset, the CPU performs a coldstart. If the bit is set, the CPU will restore the CPU registers and go to the warmstart procedure.

2-180. Coldstart

2-181. A coldstart is performed whenever one of the following occurs:

- Power is applied to system for first time.
- A [SHIFT]-[CTL]-[CLR], [ATTN] is performed.
- The software has determined that memory is invalid through a checksum.

2-182. On coldstart, the CPU clears the POR bit and disables interrupts. It resets the stack pointer and clears the CPU working registers. The RAM size is then computed in 2K block boundaries and zeros are written to all RAM addresses. The size and boundariesof the RAM are stored in memory. Then, in the following order, the CPU:

a. Initializes the RTC/comparator circuit.

b. Sets the card reader status.

c. Sets the beeper status.

d. Initializes the keyboard.

e. Sets up defaults for:

- o Display window.
- o Printer window.
- o Margin.
- o Line delay.

f. Initializes the HP-IL IC.

g. Sets the random number generator.

h. Sets the five-minute timeout.

i. Sets the power detect levels.

j. Enables interrupts.

k. Creates an empty file system.

2-183. After the above sequence is completed, the software allows the PI-ROMs (plug-in read-only memory) to do any required system initialization. The software then asks the user to set the time. After the time is set, the initial workfile is created. POR is then set to a "1" and time mode is entered.

2-184. Warmstart

2-185. When the POR bit is a "1" the software begins a warmstart and assumes that the HP-75 has been on before and there are user programs in memory. A warmstart is begun when the user presses [ATTN] or the time comparator signals an alarm. When warmstart begins, the software first checks to see if it was a keyboard or comparator wakeup. It then checks the RAM boundaries to see if they have changed (due to insertion or deletion of RAM module). If RAM was removed the software then does a coldstart. If RAM size is unchanged or added the software performs a checksum on the data. If the checksum is wrong then a warning is placed in the display (RAM invalid) and a coldstart procedure is begun. If the checksum is valid, the machine rearranges values in RAM if the boundary has incresased. The software then executes the following sequence of events:

a. Turns off card reader.

b. Resets keyboard.

c. Turns on HP-IL if neccesary.

d. Reinitializes interrupt intercepts.

e. Clears the LCD.

f. Sets up battery detects.

g. Enable interrupts.

h. Displays appropriate annunciators.

i. If comparator interrupts, performs the power down sequence.

j. Check for password; if wrong, performs the power down sequence.

k. Set up ROM tables.

l. Let PI-ROMs initialize if neccesary.

m. Check for files with '.' beginning and allow PI-ROM ROMs to claim them.

n. Purge '.' files that are not claimed.

o. Return to area of software where told to go to Sleep.

2-186. Waiting for a Key

2-187. When the machine is awake it can be in one of the following three software states:

- Time mode.
- Appointment mode.
- Edit mode.
  - Text.
  - Basic.

2-188. When the HP-75 is not running a program or displaying the time, it is expecting a key entry by the user. In order to save power after about 4 seconds of no key activity, the machine enters a light sleep state. The internal PH1 and PH2 clocks frequencies are reduced to 4.67 KHz from 611 KHz. The system then draws less current from the batteries, thereby prolonging the battery life. After about 5 minutes of no keyboard activity the machine enters the power down sequence. The following sequence must be completed before the machine goes into the light sleep state.

a. PI-ROMs are given a chance to do anything they need to do.

b. Begins 4-second countdown to light sleep time-out.

c. Services any pending non-keyboard interrupts.

d. Checks for low power--if low power, performs the power down sequence.

e. Checks for key entry.

- If there is a key entry, the system:
  - (a) Wakes up the machine to full awake.
  - (b) Processes key entry.
  - (c) Returns to step 1.
- If there is no key entry, the system continues with step 6.

f. Checks to see if 4 seconds have elapsed for light sleep time-out.

- o If 4 seconds has elapsed then begins deep sleep time-out and . continues with step 7.
- o If 4 seconds has not elapsed then the system returns to step 3.

g. Checks to see if five minutes have elapsed for deep sleep time-out.

- o If 5 minutes have elapsed, then continue with step 8.
- o If 5 minutes have not elapsed, then return to step 3.

h. Checks to see if the user has disabled deep sleep time-out.

- o If the user has not disabled deep sleep time-out, then the system performs the power down sequence.
- o If the user has disabled deep sleep time-out, then return to step 3.

2-189. Power Down

2-190. The power down mode of the HP-75 is used to perform the necessary housekeeping functions before going to deep sleep. The deep sleep state is characterized by a blank display with power applied to the RAM and comparator circuits. This allows for continuous memory when the machine is not being used. The power down sequence is encountered when one of the following conditions occures:

- o BYE is encountered in a program.
- o [SHIFT]-[ATTN] is executed.
- o [B]-[Y]-[E]-[RTN] is typed into the machine.
- o There has been no key entry for at least 5 minutes.
- o The battery detect has determined that the batteries are too low for proper operation to continue.

2-191. When BYE is encountered in a program, the HP-75 halts the program and performs the power down sequence. This allows appointments to wake up the machine since it is no longer running a program.

2-192. When the power down mode is called from other software the following sequence takes place.

a. HP-IL unlisten message is sent to HP-IL devices.

b. LCD is cleared.

c. The first two display annunciators are cleared.

d. If HP-IL oscillator is on, it is turned off.

e. If low battery is detected, BATT annunciator is turned on.

f. Comparator is given a chance to service itself.

g. System checks for any pending timers.

h. If timers need service, services them.

i. Processes [EDIT] key.

j. Processes appointments.

k. Restarts power down sequence.

l. Gives PI-ROMs a chance to do perform any needed operations.

m. Interrupts are disabled.

n. Sets beginning address on stack for warm start initialization.

o. Saves CPU working registers in RAM.

p. Computes RAM checksum.

q. Saves checksum for use in warmstart.

r. Goes into deep sleep.

SECTION
III

DISASSEMBLY AND REASSEMBLY

3-1. INTRODUCTION

3-2. This section describes--both in words and in pictures--how to access, remove, and replace the major assemblies of an HP-75. These assemblies are shown in figure 7-1, which shows the HP-75 in an exploded view.

3-3. Each disassembly procedure builds on the previous procedures. For example, removal of the logic board is discussed in procedure 3-11, but you must do all preceeding disassembly procedures first. This is likewise true for the assembly procedures.

3-4. REMOVING AND TIGHTENING SCREWS

3-5. The main tools you will need to remove and replace the major HP-75 assemblies are a #1 Posidriv screwdriver and nest to set the unit in. All screws in the HP-75 are Posidriv--not Phillips. Although a Phillips will work, it can easily strip the screw heads.

3-6. Due to the nature of the plastic used in the HP-75, the threads can easily be stripped if you overtighten the screws. If you strip the threads, you will have to replace the part. Try to engage the screws in the original threads to minimize the chance of stripping the threads.

3-7. Table 3-1 lists the tools recomended for disassembly and assembly.

Table 3-1. Recommended Tools

HP Part Number	Discription
00075-60918	Diagnostic fixture
00075-60907	Topcase nest
8710-0899	Posidrive screwdriver, #1

CAUTION

The ICs in the HP-75 can be very easily damaged by electrostatic discharge (ESD) if adequate precautions are not taken. Observe these precautions:

- The surface of the repair bench must be grounded.
- Any tool or fixture that is used in the disassembly, reassembly, or troubleshooting of the computer must be grounded to the surface of the repair bench.
- All assemblies must be kept within their antistatic containers during storage and while being carried to the repair bench.
- While handling assemblies, repair personnel must wear a wrist strap grounded to the surface of the repair bench.
- Use an air ionizer to drain static charge from the repair bench area.

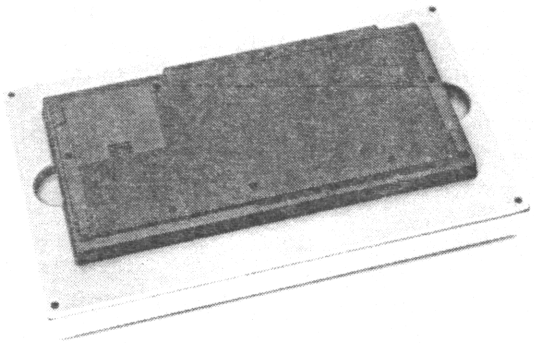
CAUTION

Parts in the HP-75 can be easily contaminated with grease or dirt while you are handling them. To prevent this from happening, wear finger cots during disassembly and reassembly. Failure to do so can result in improper operation of the computer.

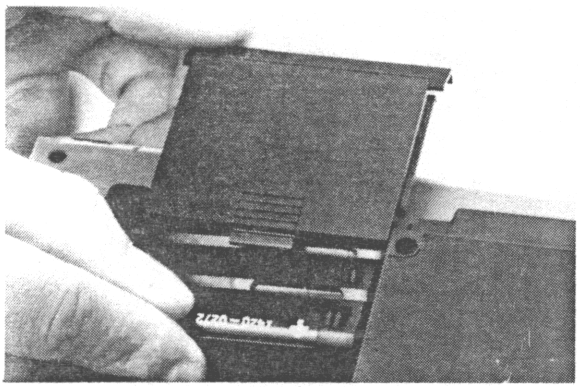
3-8. REMOVING THE BACK CASE

a. Ensure that the computer is turned off by pressing the [SHIFT] and [ATTN] keys at the same time.

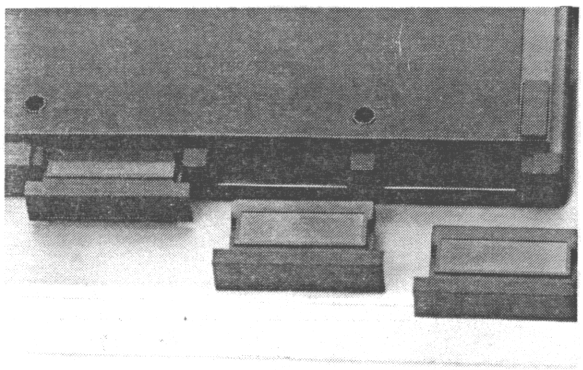
b. Place the computer in the nest as shown, press down and outward on the battery compartment door until it slides out.



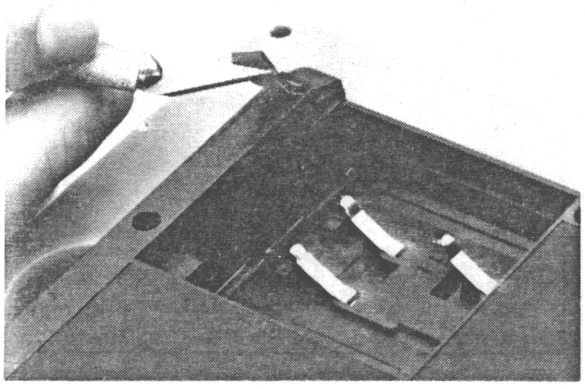
c. Remove the battery. Also remove the plug-in RAM module if one is present.



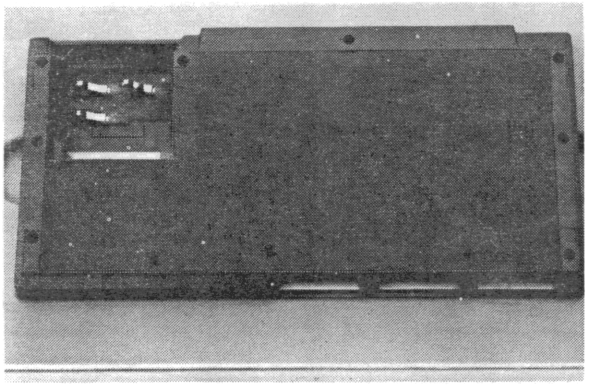
f. Pull the three ROM port covers out of the ROM ports in the front left side of the computer.



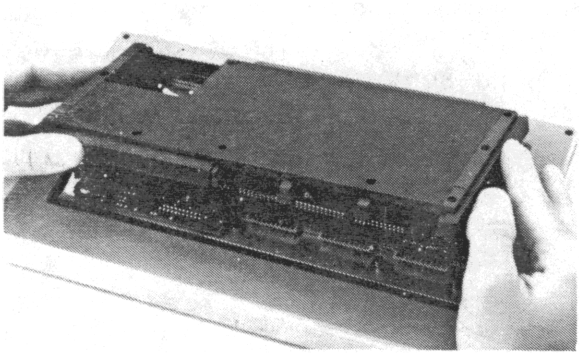
e. Remove and discard the four feet. Use a sharp knife to lift one corner, then peel off the foot.



f. Using a #1 Posidriv screwdriver, remove the 11 screws from the bottom case.



g. Pull the case apart. Gently pull up simultaneously on both sides of the bottom case.

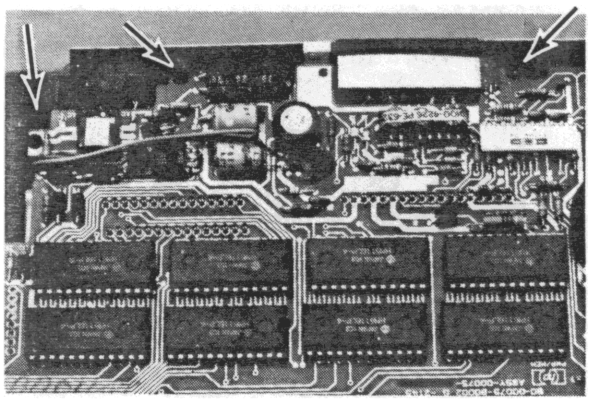


3-9. REMOVING THE POWER SUPPLY/RAM PCA

After separating the case (procedure 3-8):

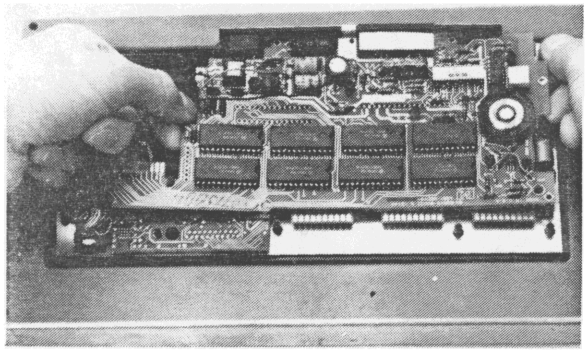
a. The PCA facing you is the power supply/RAM PCA.

b. Remove the three screws that hold the power supply/RAM PCA.



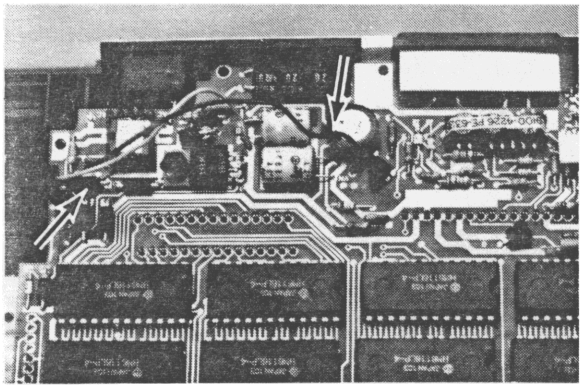
> CAUTION
>
> Do not put anything between the PC boards to pry the boards apart. This may damage the circuit traces on the PC boards.

c. Slowly begin to loosen the power supply/RAM PCA by pulling it up at different points close to the connecting pins.



d. If the power supply/RAM PCA is to be replaced perform step e. If the power supply/RAM board is not being replaced then skip to procedure 3-10.

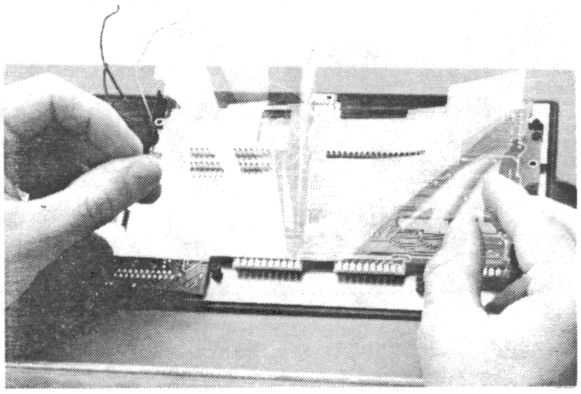
e. Unsolder the black, red, and blue wires connecting the battery compartment to the power supply/RAM PCA.



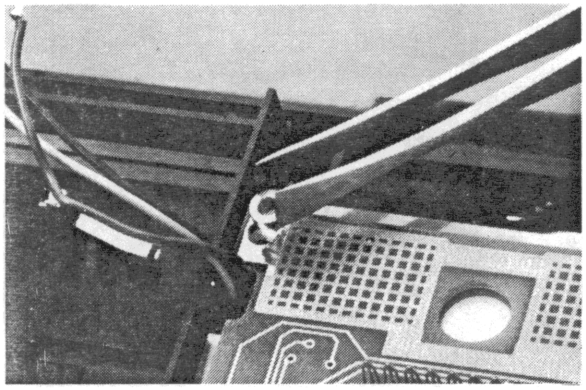
3-10. REMOVING THE LOGIC PCA AND THE DISPLAY ASSEMBLY

After separating the case and removing the power supply/RAM PCA (procedures 3-8 and 3-9):

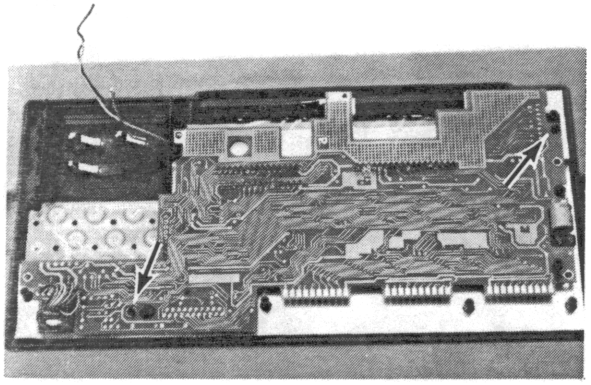
a. Remove the two mylar barrier sheets that are on top of the logic PCA.



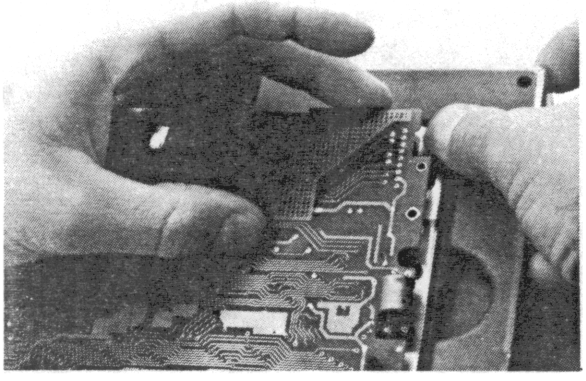
b. Remove the brass stand off.



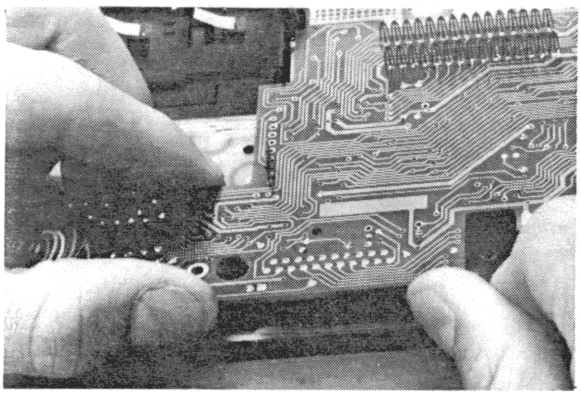
c. Remove the two screws that are holding the logic PCA.



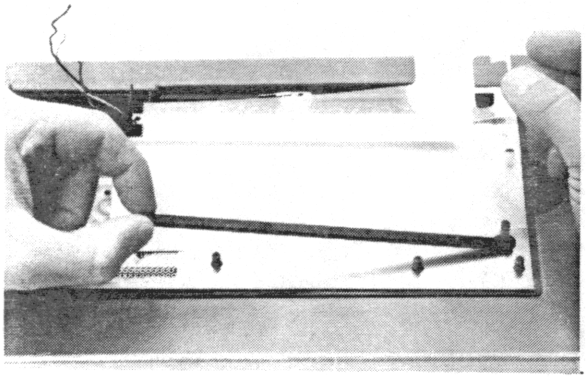
d. While pressing down on the display assembly, loosen the connector pins in the upper-right hand corner between the logic PCA and the display.



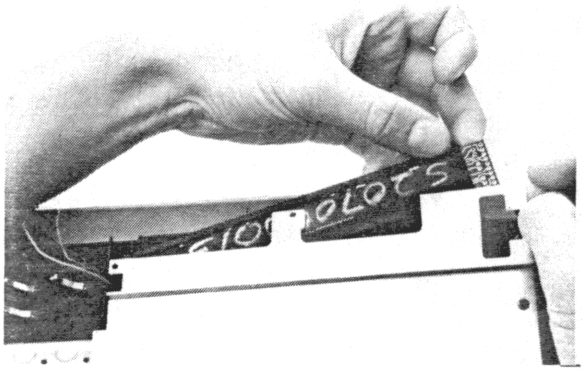
e. Loosen the connector pins in the lower left corner between the logic PCA and the keyboard PCA. Remove the logic PCA.



f. Remove the spacer strip in the lower center of the keyboard PCA, then remove the ground plane insulator.

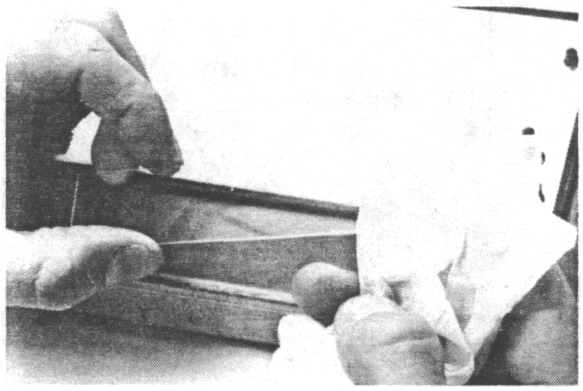


g. Remove the display assembly and the cover window while gently lifting up on the ground plane.



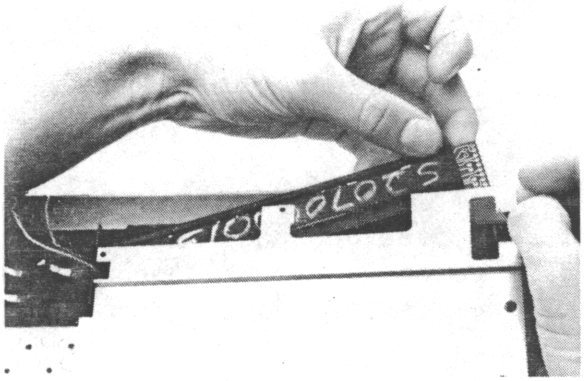
3-11. ASSEMBLING THE LOGIC AND DISPLAY ASSEMBLIES

a. Lay the top case in the nest so the keys are face down and the battery compartment is in the lower-right hand corner.



b. Carefully clean the plastic window with alcohol and a lint-free wipe.

c. Insert the plastic window in the top case with the dull finish side down.

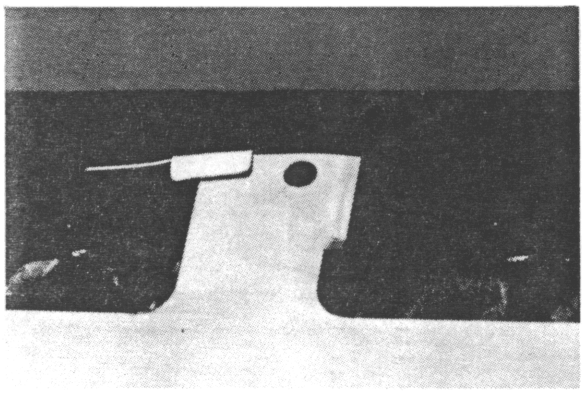


d. Clean the display side of the display assembly with alcohol.

e. Lay the display assembly in the top case with the pin connector holes on the right and press the PCA into the slot.

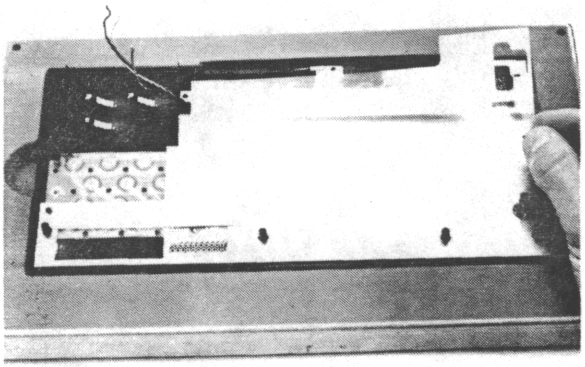
f. Be sure the ground plane is laying flat and properly in place.

g. Be sure the top case overlay tab is on top of the grounding tab of the ground plane.

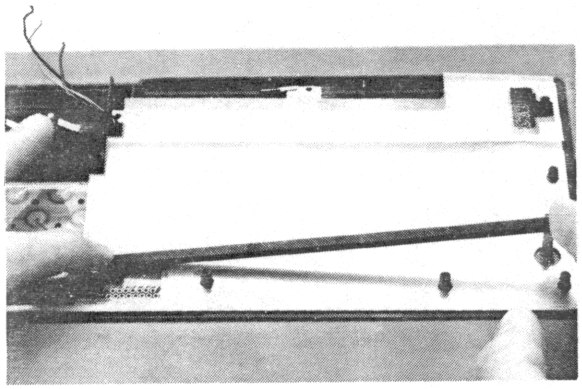


h. Examine the ground plane insulator, which covers the ground plane, for any holes or tears. If there are holes or tears, replace it with a new one.

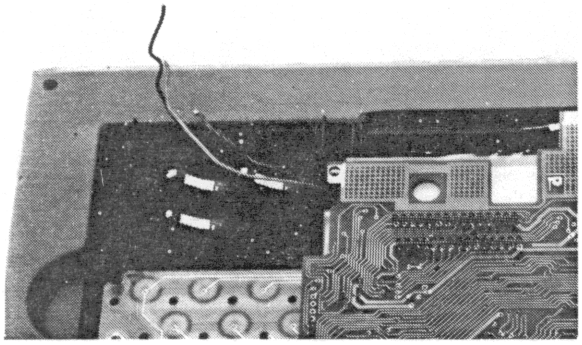
i. Lay the ground plane insulator on top of the ground plane.



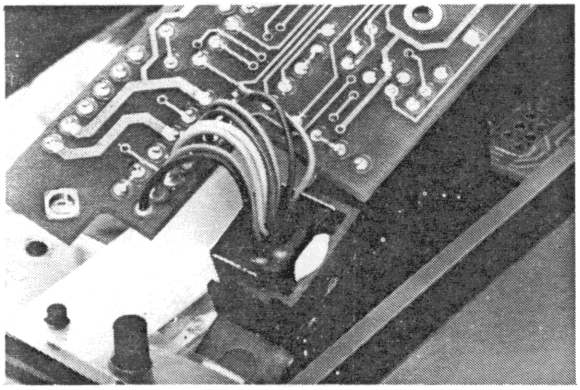
j. Install the spacer strip as shown.



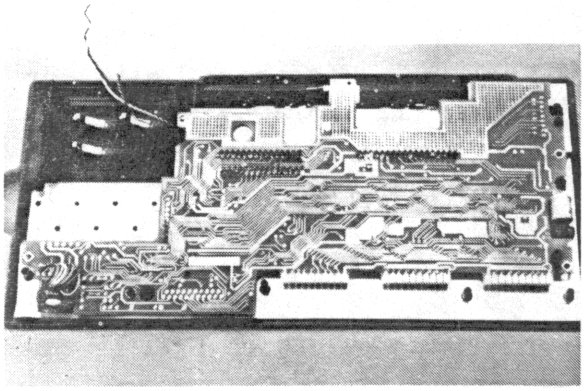
k. Hold the logic PCA with the component side down, and the ROM port connectors away from you. Note the position of the three wires near the battery compartment.



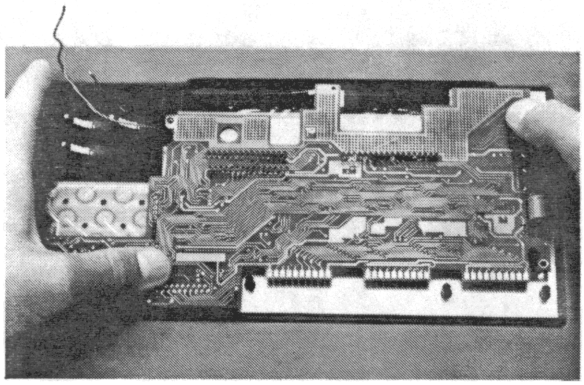
l. Insert the lip of the card reader into the slot being sure the other end sets on the locating boss.



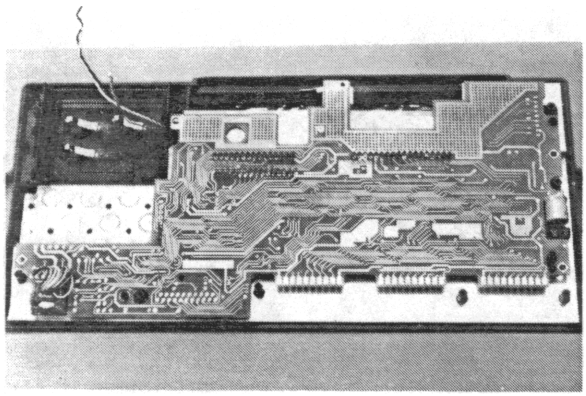
m. Lay the logic PCA on the top case aligning the screw holes and the connector pins.



n. Slowly press the logic PCA into place, making sure the connector pins all seat into their proper holes.

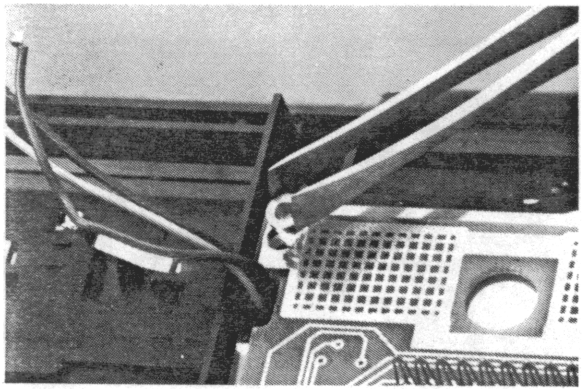


o. Insert the two screws into the logic PCA.



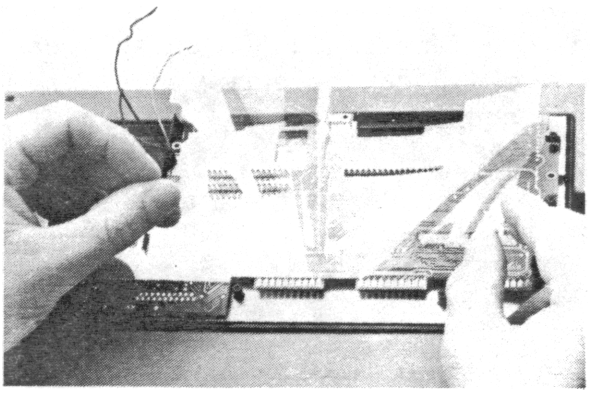
3-12. INSTALLING THE POWER SUPPLY/RAM PCA

a. Install the brass stand off on top of the logic PCA.

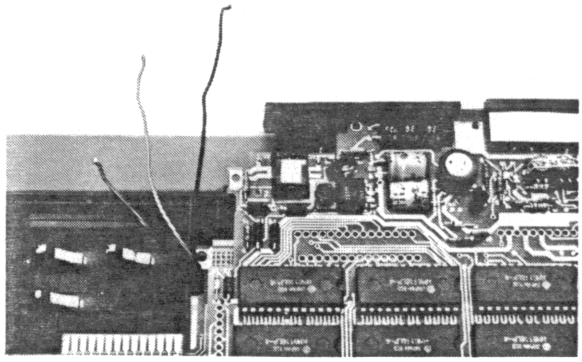


b. Examine the two mylar barrier sheets for holes or tears. If they are damaged, replace them.

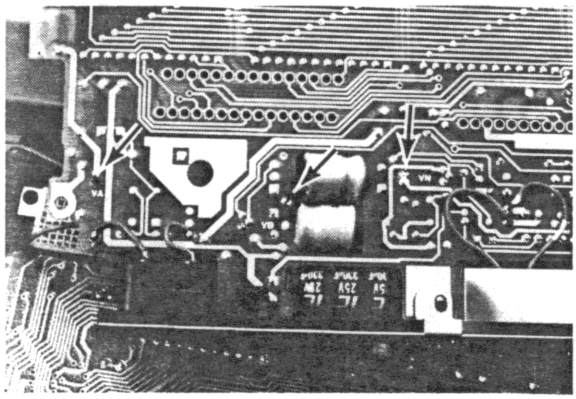
c. Install the two mylar barrier sheets on top of the logic PCA



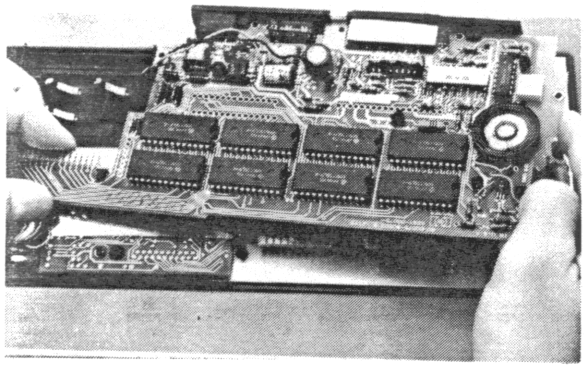
d. Carefully note the position of the wires shown. They will need to be soldered into the corresponding holes.



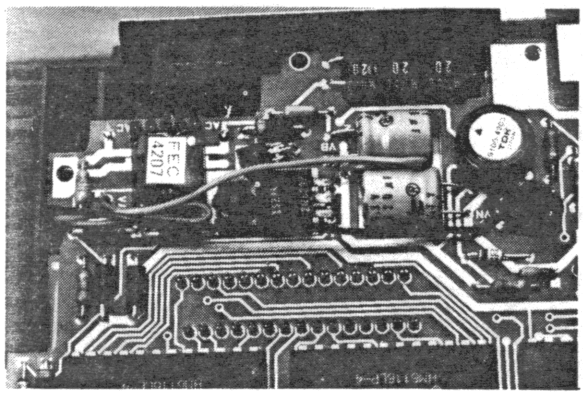
e. Laying the power supply/RAM PCA across the unit as shown, solder the blue, red, and black wires into the corresponding holes.



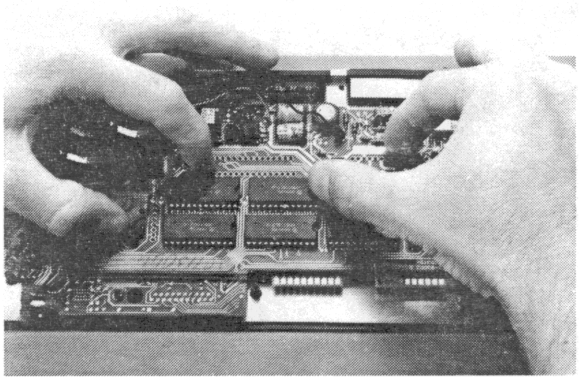
f. Swing the power supply/RAM PCA into position over the logic PCA.



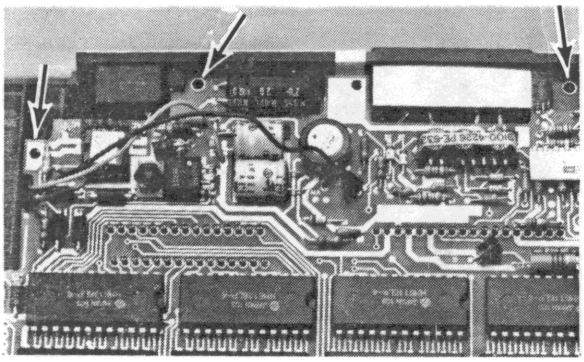
g. At the battery compartment, pull the blue, red, and black wires into the relief slot. Set the I/O assembly into its slot and align the power supply/RAM PCA over the connector pins.



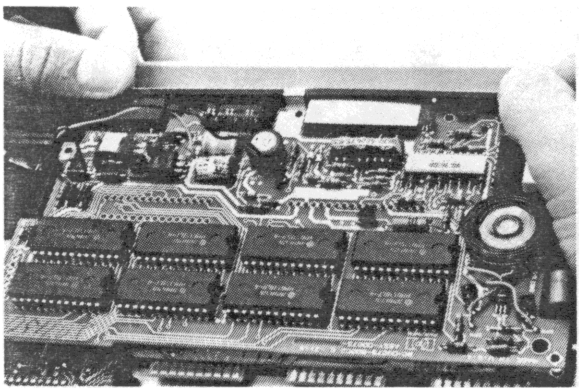
h. In the locations shown, gently press the power supply/RAM PCA onto the connector pins.



i. Insert the three screws into the power supply/RAM board, while making sure the I/O assembly is properly seated.

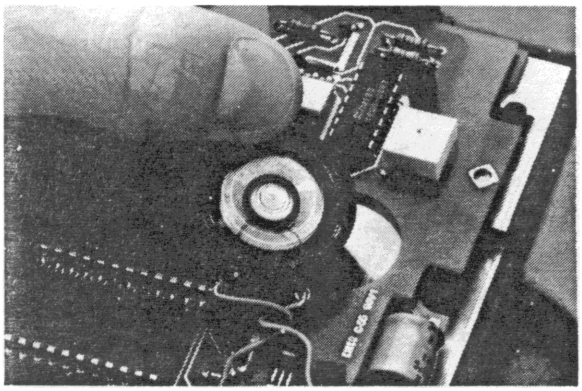


j. Bend the blue, red, and black wires over the power supply/RAM PCA as shown.



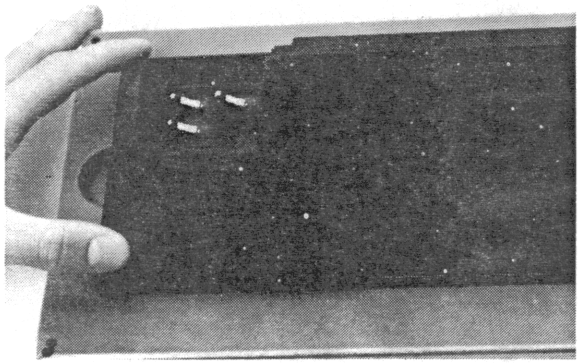
3-13. INSTALLING THE BACK CASE

a. Set the speaker in its recess in the power supply/RAM PCA.

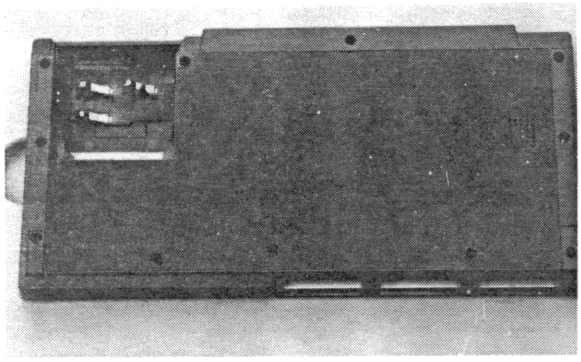


b. Set the back case on the unit and align it with the top case.

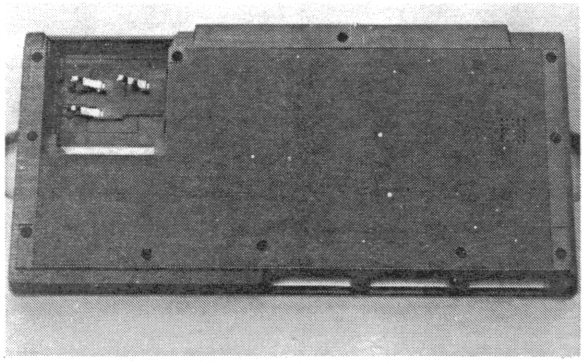
c. Gently press the back case into place. Make sure the speaker is aligned in its socket in the back case.



d. Install the 11 screws.

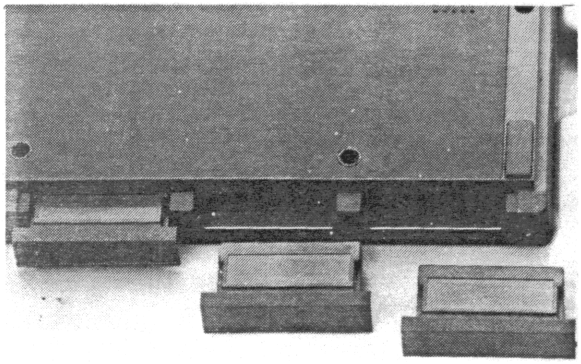


e. Install four new feet.

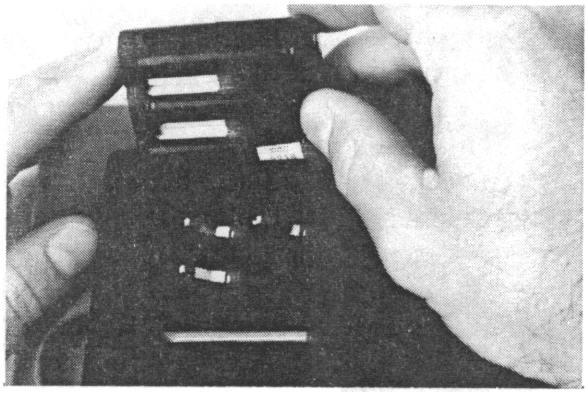


f. Insert the three ROM port covers into the ROM ports.

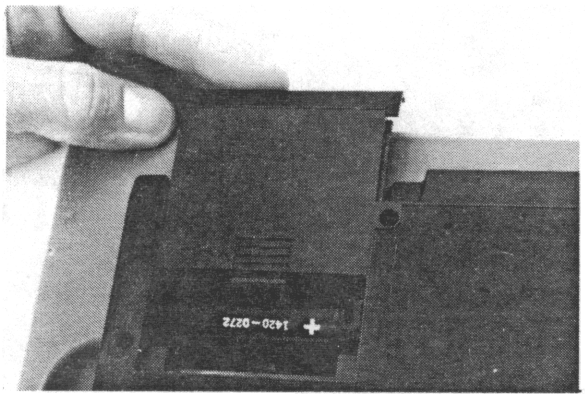
g. Install the plug-in RAM module if you removed one earlier.



h. Install the battery.



i. Install the battery cover.



SECTION
IV

Diagnostic ROM

4-1. INTRODUCTION

4-2. This section is a reference section that describes the diagnostic ROM and the way it tests the HP-75. The diagnostic ROM is used as part of the testing procedures in section 5. However, section 5 uses only the multiple test feature of ROM. Depending on what testing you need to do, you may find some of the other features of the ROM usesful. For example, you may need to do a burn-in on a unit that came in for repair. In that situation the auto test feature should be used.

4-3. This section will describe the features of the ROM. You should read this section to familiarize yourself with the ROM before actually using it in any testing procedure.

4-4. DESCRIPTION OF THE DIAGNOSTIC ROM

4-5. The diagnostic ROM is a preprogrammed ROM (read-only memory) designed to be inserted into the right ROM port (port 3) of the HP-75. Its program is designed to take control of the CPU and exercise the various ICs and buses, thereby detecting most hardware malfunctions. The diagnostic ROM cannot determine if the software is operating properly except where certain software responses, in connection with a test, are expected but not received.

4-6. The diagnostic ROM assumes a working kernel of hardware consisting of a portion of the CPU, the system bus, system clocks, part of system ROM 0, and the diagnostic ROM itself. If any part of this kernel is not working, then the computer will probably not turn on--the display should remain blank (but junk could be in the display) and no audible frequencies should emitted from the speaker.

4-7. The diagnostic ROM tests pieces of hardware outside of the initial kernel. As these pieces are found to be OK, the diagnostic ROM adds these new pieces to the working kernel and uses the expanded working kernel to test additional pieces of hardware. The working kernel thus grows until all pieces of the computer have been tested.

4-8. When a test is completed on a good piece of hardware, the diagnostic ROM displays "OK" and emits a high-pitched beep. If the piece is not good, "BAD" is displayed and a low-pitched beep is emitted. Thus, if the display is not working when the diagnostic ROM is first turned on, you can tell if the diagnostic ROM is working by listening for the beeps.

4-9. The diagnostic ROM reassigns the keyboard when it comes on. Before using the diagnostic ROM place the diagnostic ROM overlay on top of the keyboard. If you do not have an overlay refer to table 4-1 at the end of this section for a list of the key reassignments.

4-10. Once a test has been run individually, during the multiple test, or during the auto test and found to be bad, the diagnostic ROM will maintain a "BAD" in its status table for that test even if the test runs "OK" later. the status table can be cleared by pressing the reset key or by turning the HP-75 off and then on. In either case the CPU and RAM tests will be automatically run when the ROM takes over the system again.

4-11. TROUBLESHOOTING WITH THE DIAGNOSTIC ROM

4-12. To properly use the diagnostic ROM you will need a polarity reversible HP-IL cable, a magnetic card, and a diagnostic ROM service check sheet.

> CAUTION
>
> The HP-75 must be turned off before you insert the diagnostic ROM. If the HP-75 is not turned off when you insert the ROM, the ROM, the HP-75, or both could be severely damaged.

4-13. When using the diagnostic ROM, be sure you do the following:

a. Make sure the computer is off by pressing [SHIFT]/[CTL]/[ATTN] keys at the same time and hold them down for one second before inserting the ROM.

b. Insert the diagnostic ROM into ROM port three (the one nearest the card reader) in the front of the computer.

c. Press [ATTN] to turn on the computer. When the computer comes on the ROM will automatically take control of the CPU. The diagnostic ROM automatically runs the CPU and the RAM test when it comes on. If both tests are OK, then it will ask you to select a test. Refer to paragraphs 4-32 and 4-35 for an explanation of the CPU and RAM tests.

d. The test you will be using to troubleshoot the computer in section 5 is the multiple test. In addition to this test, you can run the auto test or select individual tests for special testing procedures.

e. After you have completed the diagnostic ROM tests, press the [SHIFT] and [ATTN] keys to turn the computer off, then remove the ROM.

4-14. DIAGNOSTIC ROM GROUP TESTS

4-15. There are two groups of tests that can be run from the diagnostic ROM. These tests can be run normally with the computer awake or they can be run while the computer is in light sleep by using the light sleep toggle. The two groups of tests are:

- The multiple test.
- The auto test.

4-16. Each group is made up of various individual tests that are run in a specified order for maximum error checking. The descriptions of the individual tests that make up each group are found in paragraph 4-30.

4-17. Multiple Test

4-18. This is the test that is used in section 5 to troubleshoot the HP-75.

4-19. The multiple test automatically runs most of the available diagnostic tests. Certain tests require operator input. When the computer runs one of these tests, it will stop, emit a medium tone beep and display a message indicating the type of input it is looking for.

4-20. To interrupt the testing cycle, press [ATTN] and the computer will complete the current test and return to a state of waiting for another test to be selected.

4-21. The following tests are run during the multiple test:

- o ROM checksum.
- o Keyboard.
- o Clock.
- o MAR.
- o Deep sleep.
- o Battery level detect.
- o LCD driver.
- o LCD controller.
- o HP-IL.

4-22. As these tests are run, messages are displayed. The first message is the current test being run. Then the results of the test are given as either "OK" or "BAD". As each test is being run, you should remember the results of both the tests and the subtests.

4-23. Most tests are made up of several subtests. The status of each subtest is reported as it is run.

4-24. After the multiple test is completed, you can call up the mulitple report, which will review the status of each test. The multiple report does not report on the status of any subtest.

4-25. You may delay a test and hold the current display by pressing the space bar key. This is advisable while using the check sheet so you don't miss any status reports.

4-26. Auto Test

4-27. The auto test is designed to exercise the computer with no operator input. This test repeatedly cycles through the tests in its directory. These tests are:

- o CPU.
- o ROM checksum.
- o Clock.
- o MAR.
- o Deep sleep.
- o Battery level detect.
- o LCD driver.
- o LCD controller.
- o HP-IL (only a partial test is performed).
- o Non-destructive RAM.

4-28. As these tests are run, the test name and then its status is displayed. After all the tests have been run an auto report is displayed. These messages are displayed very quickly and are very difficult to read. The cycle is then repeated continuously until you interupt the cycle by pressing the [ATTN] key. The results of the auto test can be displayed by initiating the auto report.

4-29. You may delay the reporting of the test results either during the testing cycle or during the auto test report by pressing and holding the space bar key.

4-30. INDIVIDUAL TESTS

4-31. This section lists each test and describes what it does. Many of these tests are run as part of one or both of the group tests. Additionally, the tests can be run separately when initiated from the keyboard.

4-32. CPU Test

4-33. The CPU test attempts to run the entire CPU instruction set. If some part of the instruction set does not operate, the display will show "CPU BAD x", where x is a code letter A through Q. The code letter indicates the type of CPU error. Refer to table 5-3, Diagnostic ROM Error Messages for an explanation of what to do for one of these error messages.

4-34. The CPU test is automatically run when the computer, with the diagnostic ROM installed, is first turned on. This test is also run when the reset key is pressed, during auto test, and when initiated from the keyboard.

4-35. Destructive RAM Test

4-36. The destructive RAM test loads each RAM with different patterns of 1's and 0's. This test then checks for cross coupling between the bits in adjacent RAM locations. The test proceeds from the lowest order RAM to the highest order RAM. The highest order working RAM that is found is assumed to be the upper boundry of the RAM space. In this way, the diagnostic ROM determines the amount of RAM available in the computer.

4-37. If all the RAM in the assumed RAM space is working correctly, a high-pitched beep will sound and the display will read "nnK of RAM", where nn is the number of Kbytes. If an error is detected a low-pitch beep will sound and the display will read "RAM x BAD", where x is the letter designation of the bad RAM. (Refer to the power supply/RAM schematic, figure 8-2, for the letter disignation reference.) Then the display will show "nnK of RAM", where nn is the number of Kbytes the diagnostic ROM was able to detect.

4-38. This test is automatically run when the ROM is first turned on and when the reset key is pressed. There is no way to initiate this test from the keyboard.

4-39. ROM Test

4-40. The ROM test does a checksum on each of the ROMs. The 1's and 0's in each ROM are added in binary and checked against the reference sum stored in the diagnostic ROM. The diagnostic ROM can check the six system ROMs and all plug-in ROMs including itself.

4-41. The results of a good system ROM test are reported with a high pitch beep and a display of "ROM x OK" , where x is 0, 1, 2, 3, 4, or P4B for the six system ROMs. A bad test result has a low pitched beep and a display of "BAD" instead of "OK". The plug-in ROMs are similarly reported as "ROM Pnx OK" or "ROM Pnx BAD", where P stands for plug-in, n is the slot number (1, 2, or 3), and x is the switchable bank (A, B, C, or D) within the slot.

4-42. This test is run as part of both the multiple and auto tests. Additionally, this test can be initiated from the keyboard.

4-43. Keyboard Test

4-44. The keyboard test requires the operator to press the keys in the order specified by the message in the display.

4-45. The first message will be "PLEASE PRESS KEYS IN SEQUENCE". The keys should then be pressed in order starting in the upper left hand corner with the [TIME] key. The [ATTN] key is skipped, because the system would not wake up if the [ATTN] key was not working. Also, the [ATTN] key is used to interrupt the tests. Press one key at a time going from left to right, first doing the top row and proceeding to the bottom row. The last key to be pressed should be the space bar. If a key is missed or doesn't provide a proper signal, the computer will beep and display "EXPECTED x", where x is the key it expected. The x will be the number or letter appearing on the key, execpt for the special function keys. The special function keys will display a word or symbol representing the key. The space bar displays several spaces within quote marks (" ").

4-46. If several bad keys are found or if a whole row appears to be bad, you can abort the key sequence test by pressing the [ATTN] key. The next subtest of the keyboard test will then begin.

4-47. After each key is pressed in sequence, the computer will proceed to the modifier key test. Different messages will be displayed indicating varous key combinations which should be pressed. The computer will display in order the following messages: "PRESS CONTROL & ANY KEY", "PRESS LEFT SHIFT & ANY KEY", "PRESS RIGHT SHIFT & ANY KEY", "PRESS CONTROL & SHIFT & ANY KEY". Next the computer will prompt for the "TWO KEY TEST". A key should be pressed, while holding it down the key next to it should be pressed, and then the first key should be released. Then press another key and while holding it down press the key next to it. If you see the four keys codes appear in the display in the order the four keys were pressed then the test passes. The test passes or fails depending on what is seen in the display. The ROM has no way of detecting the results of this test.

4-48. Pressing a fifth key begins the keyboard interrupt test. Press another key and hold it down. The computer will display "KEYBOARD INTERRUPT TEST*". Continue holding down the key and the computer will display "KEYBOARD MULTIRUPT TEST*" and then the display will shift to "KEYBOARD MULTIRUPT DONE*". After the last message you can release the key.

4-49. The result of the key sequence test is OK if "PLEASE CONTINUE" is displayed while the keys are being pressed. If a key is not working the computer will display "EXPECTED x" as described in paragraph 4-45. The computer will allow three tries before displaying "x KEY BAD*" and emitting a low beep. "PLEASE CONTINUE" will then appear in the display again. All the remaining tests are OK if the display announces the next subtest. After the computer displays "KEYBOARD MULTIRUPT DONE*", the results of the total test will be displayed as "KEYBOARD OK*" and a high-pitched beep will sound, or "KEYBOARD BAD*" and a low-pitched beep will sound.

4-50. This test is run as part of the multiple test or when initiated from the keyboard.

4-51. Clock Test

4-52. The clock test is comprised of three subtests, which are the real-time clock, the global disable, and the comparator tests.

4-53. The real-time clock test checks the clock to see if it runs correctly in both normal and test mode. The global interrupt disable test disables the global interrupt and then checks for an interrupt. The comparator test checks to see if the comparator is able to interrupt the system.

4-54. As each test is run, it is announced in the display. If the test is good an "OK" is displayed and a high-pitched beep is emitted. If the test is bad, a "BAD" is displayed and a low-pitched beep is emitted.

4-55. This test is run as part of both the multiple and the auto tests. It can also be initiated from the keyboard.

4-56. Deep Sleep Test

4-57. The deep sleep test checks to see if the computer properly turns off (goes into deep sleep). When the computer turns off, the system clock stops. If the system clock continues to run then deep sleep does not work properly.

4-58. The computer will display "DEEP SLEEP TEST", after which it will turn off. The operator then presses the [ATTN] key to turn the computer back on. The computer immediately turns off again for 20 seconds while waiting for a comparator interrupt to wake up the system again. This 20-second delay can be eliminated by pressing the [ATTN] key again. This test is also used for checking RAM in deep sleep.

4-59. The results are reported for a good test as "DEEP SLEEP OK*" when the system turns on again and a high-pitched beep is emitted. If the test is not good, then "DEEP SLEEP BAD*" is displayed and a low pitched-beep is emitted. After either the OK or BAD message is displayed, the ammount of RAM that was OK will be reported as "nnK OF RAM". Any bad RAM ICs that are bad will be reported as "RAM x BAD". If the system clocks turn off properly, then the ROM will display "DEEP SLEEP OK*" even if some RAM is determined to be bad.

4-60. The deep sleep test is run as part of the multiple test and when initiated from the keyboard. An abbreviated version of this test is run during auto test.

4-61. Battery Level Detect Test

4-62. The battery level detect test checks to see if an interrupt is generated when the voltage level is lower than the reference level set by the CPU and detected by U2. This level is set artificially high and low by the diagnostic ROM to check for this interrupt.

4-63. The computer will display "POWER SUPPLY DETECT TEST". If the test is good, the computer will display "POWER SUPPLY DETECT OK*" and emit a high-pitched beep. If the test is not OK, the computer will display "POWER SUPPLY DETECT BAD*" and emit a low-pitched beep.

4-64. This test is run as part of the multiple and auto tests, or when initiated from the keyboard.

4-65. LCD Driver Test

4-66. The LCD driver test is a subjective test. This test passes or fails depending on what the operator sees. This test exercises the circuitry which turns on and off the various segments of the LCD. The patterns are listed in order of appearence in figure 4-1.

4-67. The computer will display "LCD DRIVER TEST*". Then the display patterns will appear. The computer will indicate the test is finished by displaying "LCD DRIVER TEST DONE*".

4-68. This test is run as part of the multiple and auto tests, or when initiated from the keyboard.

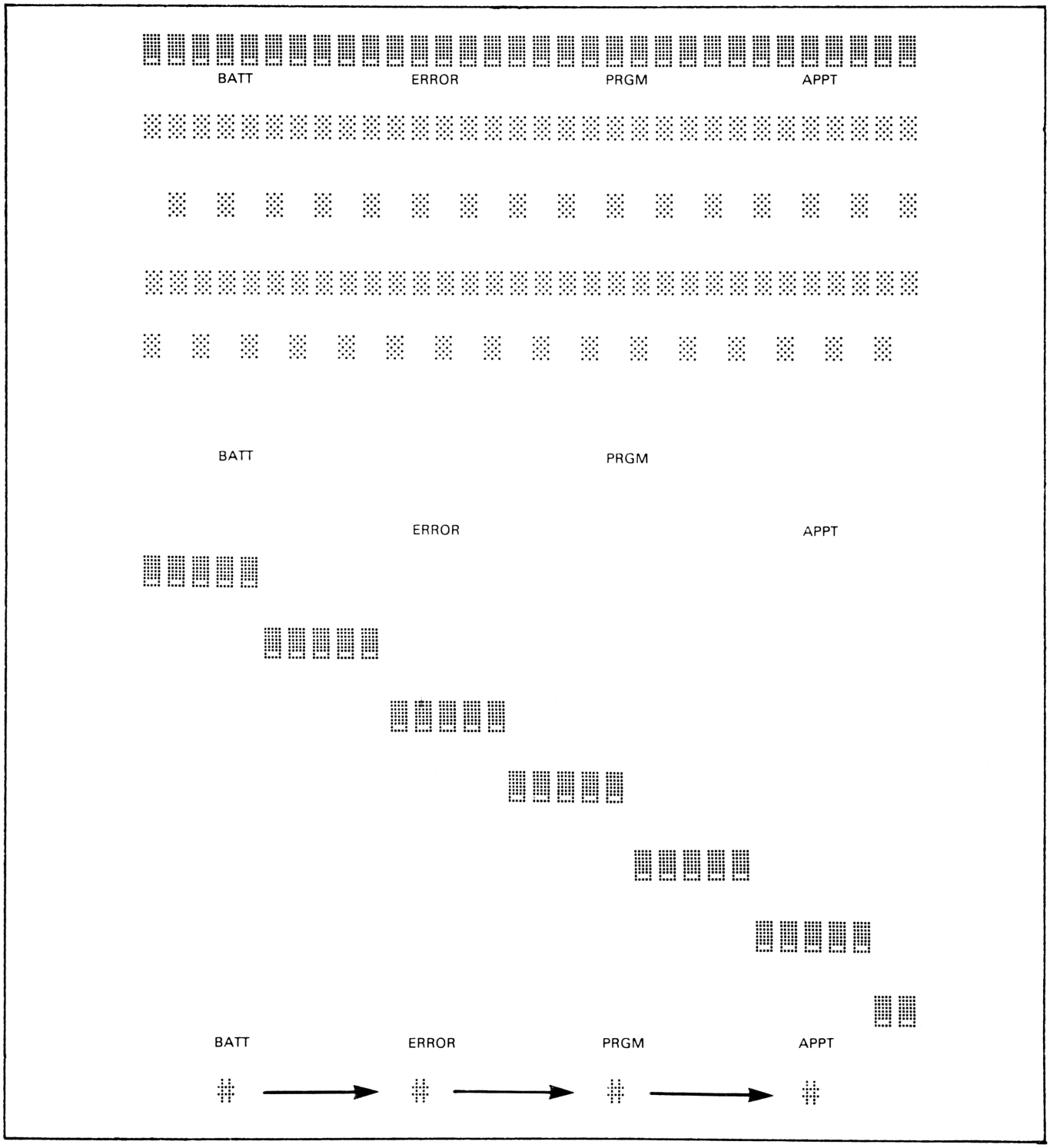


Figure 4-1. LCD Driver Characters

4-69. LCD Controller Test

4-70. The LCD Controller test is a subjective test. This test passes or fails depending on what the operator sees. This test shows the entire character set 32 characters at a time. These characters are shown in the order they are displayed in figure 4-2.

4-71. The computer displays "LCD CONTROLLER TEST*". Then the characters are displayed. The computer will indicate the test is finished by displaying "LCD CONTROLLER TEST DONE*".

4-72. This test is run as part of the multiple and auto tests, or when initiated from the keyboard.

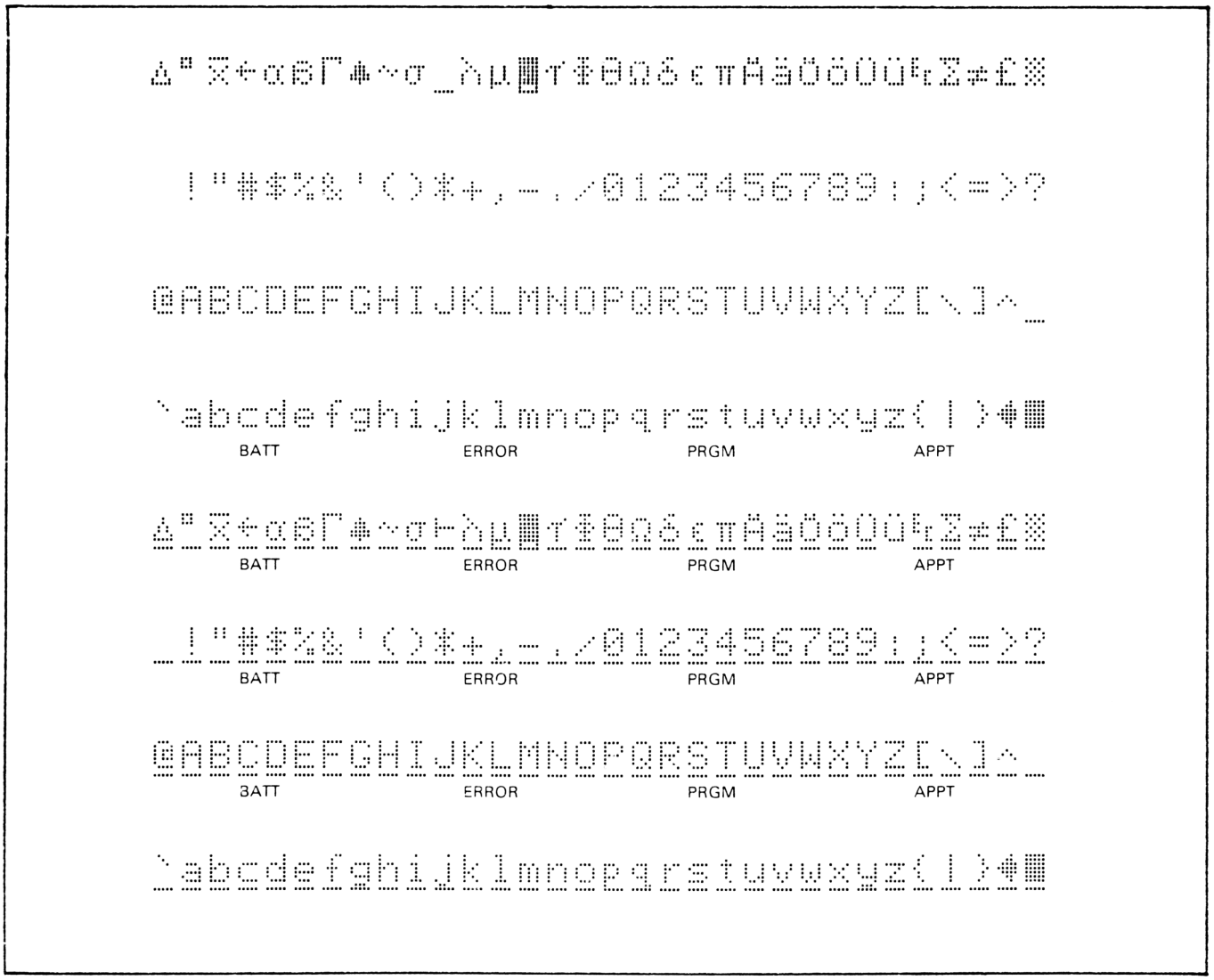


Figure 4-2. LCD Controller Characters

4-73. HP-IL Test

4-74. The HP-IL test requires operator to perform certain functions using an HP-IL cable. The test tries to exercise the various capabilities of HP-IL. HP-IL messages are sent around the loop, checked for accuracy, and checked for proper response.

4-75. The computer will display "HP-IL TEST*". Then the computer will ask "DO YOU HAVE A HP-IL CABLE? (Y/N)". Press [Y] for yes or [N] for no. It doesn't matter if the Y and N are upper or lower case letters. Do not press the [RTN] key after the [Y] or [N] or after any of your key responses in the HP-IL test. If you do have a cable and you press [Y] the computer will display "BRIDGE PORTS WITH THE CABLE". You should plug in both ends ofthe cable in their mating ports in the back of the computer so that one continuous loop is formed. After you have established the loop, press any key to begin this subtest.

4-76. Next the computer will display "PLEASE UNPLUG HP-IL CABLE". After the cable is unplugged and you have pressed a key to signal the computer that the cable is unplugged, another HP-IL message will be sent. This message, of course, should not be received.

4-77. The computer will next ask "CAN YOU REVERSE POLARITY?". If you have a cable with a reverse switch on it or a cable that has been cut and spliced back together reversed, then by pressing the [Y] key. If you cannot reverse HP-IL polarity then press the [N] key. If you pressed the [Y] key, the computer will then respond "THEN PLEASE DO SO". When you have reversed the polarity and plugged both ends of the cable back into their mating ports, press any key to begin the test.

4-78. The results of each subtest are OK unless an HP-IL error message is displayed. If an error is detected, the error messages will be displayed immediately and the test will be interrupted. The computer will display "HP-IL ERROR <error message>". The specific meaning of each error message is not important. The error messages are listed in table 5-3, Diagnostic ROM Error Messages.

4-79. If an error is detected at any step of the test the computer will ask "DO YOU WANT TO CONTINUE?". If you wish to abort the remainder of the test press the [N] key. If you wish to continue then press the [Y] key.

4-80. After the test has been completed the computer will display either "HP-IL OK*" and emit a high-pitched beep, or will display "HP-IL BAD*" and emit a low-pitched beep.

4-81. This test is run as part of the multiple test or when initiated from the keyboard. If you wish to run this test as part of the auto test, then plug in a nonreversed-polarity cable. The auto test will run only those parts of the test that use the nonreversed-polarity cable and require no operator input.

4-82. MAR Test

4-83. The MAR (memory address register) test checks the MAR IC for its ability to successfully address the RAM. Test patterns are sent out to known RAM addresses, then read back and checked for correctness.

4-84. The computer displays "MAR TEST*". If the test is good, the computer will display "MAR OK*" and emit a high-pitched beep. If the test fails, then the display will read "MAR BAD*" and emit a low-pitched beep.

4-85. This test is run as part of the multiple and auto tests, or when initiated from the keyboard.

4-86. Beep Test

4-87. The beep test checks the beeper by emitting a high-pitched beep. Even though the beeper should have been sounding throughout the testing procedures a separate test is available to verify a failure if the beep has not been heard.

4-88. The key marked BP/TST is the beep test key. The key marked BEEP turns the beeper on and off. If the beeper bothers you, you may turn it off by pressing the BEEP key once. Pressing it again will cause the beeper to begin functioning again.

4-89. The beep test passes or fails depending on what the operator hears or does not hear.

4-90. Non-Destructive RAM Test

4-91. The non-destructive RAM test checks RAM without destroying the current contents of RAM. This test checks RAM eignt bytes at a time. The contents of the eight bytes are stored in one of the CPU registers during the time those eight bytes are being tested.

4-92. The computer displays "NON-DESTRUCTIVE RAM TEST*" at the start of the test. The results for a good test are reported by the computer displaying "nnK OF RAM". Where nn is the number of Kbytes that the diagnostic ROM found in the computer. This test is very similar to the destructive RAM test.

4-93. This test is run as part of auto test or when initiated from the keyboard.

4-94. Light Sleep Tests

4-95. Since the computer is in light sleep except when it is running a program, receiving keyboard input, or performing I/O operations, it is important to know if the computer is operating properly while it is the light sleep state. This test is toggled. When set or enabled, diagnostic ROM will run those tests listed below while the HP-75 is in light sleep. These tests will be run in light sleep mode even if they are run as part of the multiple or auto test. Pressing any key during a light sleep test will awaken the computer and cause the messages in the display to be displayed very quickly. So do not press any key during light sleep tests except the [ATTN] key to abort the current test.

4-96. The following tests are run in light sleep whenever the light sleep tests are enabled:

- CPU.
- ROM checksum.
- MAR.
- Deep sleep.
- LCD driver.
- LCD controller.

4-97. It is easy to recognize that the computer is running in light sleep. The display messages will appear to scroll onto the display one character at a time. If the messages appear to flash onto the display normally, then light sleep is not working properly.

Table 4-1. Key Reassignments

Primary Key	Alternate Key*	Test Performed or Function
[ATTN]		Turns unit on
[SHIFT]-[ATTN]		Turns unit off
[CLR]	[BACK]	Reset
[W]	[1]	Multiple test
[E]	[2]	Auto test
[R]	[3]	ROM test
[T]	[4]	Keyboard test
[Y]	[5]	Real time clock, global disable, and comparator test
[U]	[6]	MAR test
[I]	[7]	Deep sleep test
[O]	[8]	Battery level detect
[P]	[9]	LCD driver test
[*]	[0]	LCD controller test
[TAB]	[*]	HP-IL test
[Z]	[LOCK]	Card reader toggle
[X]	[A]	Light sleep toggle
[C]	[S]	Beep toggle
[V]	[D]	Beep test
[B]	[F]	CPU test
[N]	[G]	Non-destructive RAM test
[M]	[H]	Multiple test report
[,]	[J]	Auto test report
	[K]	Return test
[/]	[L]	Diagnostic ROM revision
[RUN]	[;]	Skip auto test
	[SHIFT]-[=]	Card reader read/write
	[SPACE]	Pause test and display

*If a whole row of primary keys are not functional then the alternate key will probably be functional. This allows you to run the diagnostic ROM tests even if the keyboard is not fully functioning.

SECTION
V

Troubleshooting and Testing

5-1. INTRODUCTION

5-2. This section contains the procedures you should follow to isolate the cause of a problem in an HP-75C Portable Computer. It also gives the procedure to verify that a unit is good. Tools that facilitate service are listed in table 5-1.

> CAUTION
>
> Ensure that adequate precautions are taken regarding electrostastic protection. Work at a bench setup that is electrostatically protected. Otherwise , components may be damaged.

Table 5-1. Recommended Tools

HP PART/MODEL NUMBER	DESCRIPTION
00075-60918	Diagnostic fixture
00075-60905	Display intensity adjustment fixture
00075-60906	Ammeter adapter
00075-60903	Diagnostic ROM
7121-4125	Diagnostic ROM overlay
00075-60915	'TEST' and 'VERIFY' programs (card)
00075-60916	Cleaning card
8710-0899	Posidriv screwdriver, #1

5-3. This section contains three troubleshooting tables. The first is table 5-2, Repair Procedures. This table contains the procedures necessary to repair the HP-75C. This table is the main structure of the repair process. Table 5-3, Operational Verification, is used to verify that the repaired unit is fully operational and ready to be returned to the customer. Table 5-4, Diagnostic ROM Error Messages, describes the procedure to use when an error has occured while using the diagnostic ROM.

5-4. When troubleshooting the HP-75C, start with table 5-2, Repair Procedures. Sequentially follow the steps and actions in this table. If an error occurs while using the diagnostic ROM, you will branch to table 5-4, Diagnostic ROM Error Messages. Look for the specific error message that was displayed by the HP-75 and perform the action indicated. After you have completed that action, return to the step in table 5-2 from which you branched and repeat the step. Then proceed through the remainder of the table. For example, if the MAR test failed while running the multiple test under section C, step 3 in table 5-2, branch to TEST: MAR in table 5-4. After you have replaced the logic PCA, return to step 3 under section C in table 5-2 and rerun the multiple test. After the multiple test has finished, complete the remainder of table 5-2.

5-5. If a board must be replaced, replace it with a new board and perform the failed test again. If the procedure shows that the problem could be in more than one assembly, replace the assemblies in the order specified under the priority column. After the first priority assembly has been replaced, perform the step again where the failure occurred. If the unit fails the test again, put the first priority assembly that was just replaced back into the unit and replace the second priority assembly. Follow this general outline until the unit passes the test. Note that in some situations you may need to replace two or more assemblies, so sometimes you may need to replace two assemblies at a time. Replace two assemblies at a time only after you have tried replacing the indicated assemblies one at a time.

5-6. Some steps will tell you to check all of the solder connections on various ICs. In doing so, gently try lifting the leads one at a time. If a lead can be lifted, solder the lead to the trace with a narrow tipped soldering iron. Be careful not to desolder the surrounding leads. After you have resoldered the lifted lead, do not clean the PCA. If more than five leads are lifted on one PCA, replace that PCA. After any soldering, return to and repeat the step where the failure occurred.

5-7. INITIAL PREPARATION

5-8. Perform the following steps before attempting to troubleshoot the HP-75:

a. Visually inspect the unit for physical damage. Replace any assemblies that are physically damaged.

b. Determine the customer's concern, if possible. Frequently the customer includes a message with the unit describing the problem.

- o If the problem relates to the rechargable battery pack or recharger, test them according to the procedures in section 6.
- o For other problems with the unit, perform the test and repair procedures beginning with table 5-2, Repair Procedures.

Table 5-2. Repair Procedures

STEP	ACTION
A. LEAKAGE CURRENT TEST	
1. Remove the battery.	
2. Remove the Memory Module, if one is present in the unit.	
3. Remove any plug-in modules.	
4. Install the ammeter adapter in the battery compartment.	
5. Press and hold [SHIFT] [CTL][CLEAR] for two seconds.	
6. Measure the current.	If the current is less than 200 microamps, the power supply/RAM PCA is good. If the current is greater than 200 microamps, replace the power supply/RAM PCA. Repeat steps 5 and 6.
7. Remove the ammeter adapter.	
B. POWER SUPPLY TEST	
For the following tests, if the display comes on or the unit beeps, the unit has turned on.	
1. Insert the diagnostic ROM into port 3.	

Table 5-2. Repair Procedures (Continued)

STEP	ACTION
2. Install a known good battery.	
3. Do not connect the recharger.	
4. Press [ATTN].	If the unit does not turn on, replace the power supply/RAM PCA. Then repeat this section starting with step 1.
5. Press [SHIFT][ATTN].	
6. Connect the recharger to the unit.	
7. Press [ATTN].	If the unit does not turn on, replaced the power supply/RAM PCA. The repeat this section starting with step 1.
8. Press [SHIFT][ATTN].	
9. Remove the battery.	
10. Press [ATTN].	If the unit does not turn on, replace the power supply/RAM PCA. Then repeat this section starting with step 1.
11. Press [SHIFT][ATTN].	

Table 5-2. Repair Procedures (Continued)

STEP	ACTION
C. DIAGNOSTIC ROM TESTS If the unit fails any step in this section, place the unit on the diagnostic fixture and repeat the test before replacing any assemblies. After the unit is on the diagnostic fixture, if the unit fails any test, refer to the section for that test in table 5-4, Diagnostic ROM Error Messages. As soon as a diagnostic error occurres, interrupt the test and refer to table 5-4. Replace the indicated assembly and return to step 1 of this section and repeat the steps.	
1. Press [SHIFT][ATTN].	
2. Install the battery and connect the recharger.	
3. Insert the diagnostic ROM into port 3.	
4. Press [ATTN]. The CPU and RAM tests automatically run.	If the unit fails either test, refer to table 5-4, Diagnostic ROM Error Messages.
5. Press key [1] or [W] to run the Multiple test.	If the unit fails any test, refer to table 5-4, Diagnostic ROM Error Messages, under the test that failed. Then return here and rerun the Multiple test.
6. Press [SHIFT][ATTN].	
7. Remove the diagnostic ROM.	

Table 5-2. Repair Procedures (Continued)

STEP	ACTION
D. OPERATING SYSTEM CHECK If the unit fails any of the next three tests, first replace the logic PCA and then perform the three tests again. If the unit again fails any of these tests, reinstall the logic PCA that was just replace and then replace the power supply/RAM PCA and perform the three tests again. If the unit fails again, then replace the logic PCA so that a new logic PCA and a new power supply/RAM PCA are in the unit.	
1. Press [ATTN].	Only "SET Mo/Dy/Year Hr:Mn:Sc AM" should be in the display. The cursor should be over the first M. If anything else is in the display, the unit has failed this test.
2. Press [ATTN].	Only "SAT 01/01/0000 12:00:01 AM" should be in the display. The cursor should be two spaces to the right of the AM and the clock should be counting. If anything else is in the display, the unit has failed this test.
3. Press [EDIT].	Only the prompt '>' and the curser should be in the display. If anything else is in the display, the unit has failed this test.
E. CARD READER TEST Use the program "Test" that is on a magnetic card for the following steps. A listing of the program is in table 5-5. For information on the use of the card reader, refer to section 8 of the owner's manual.	
1. Type "copy card to 'test' card" then press [RTN]. Follow the instructions in the display. Use the card labeled "Test".	If the HP-75 has trouble reading the card, clean the head and the card and try again. If after 10 tries the HP-75 still has problems reading the card, replace the logic PCA and repeat this step.

Table 5-2. Repair Procedures (Continued)

STEP	ACTION
2. Type "edit 'test'" then press [RTN].	
3. Press [RUN].	The following should be displayed in order: "CARD READER TEST" "PLEASE WAIT" "1 track(s) needed" "Copy to card: Align & [RTN]"
4. Align a blank card in the card reader slot and press [RTN].	"Pull card..." should be displayed. If anything else is displayed, replace the logic PCA.
5. Pull the card.	"Verify card: Align & [RTN]" should be displayed. If anything else is in the display, replace the logic PCA.
6. Align the card, press [RTN], and pull the card.	If the card was verified, then the following will be displayed: "1 track(s) needed" "Copy to card: Align & [RTN]" If the verify fails, clean the card and the card reader and try to verify the card again. If the verify fails for 10 tries, replace the logic PCA.
7. When the "Test" program has been successfully completed, "Finished" will be displayed.	

Table 5-2. Repair Procedures (Continued)

STEP	ACTION
8. If the logic PCA was replaced during the card reader test, return to step 1 and repeat this test.	

Table 5-3. Operational Verification

STEP	ACTION
1. Press and hold [SHIFT] [CTL][CLR] for two seconds.	
2. Insert the diagnostic ROM in port 3.	
3. Press [ATTN].	"SELECT TEST" should be displayed after the CPU and RAM tests.
4. If no trouble has been found with the unit from the time testing first began in table 5-2 until this step, then proceed with step 6.	
5. Press key [1] or [W] to run the Multiple test. Then proceed with step 8.	If any diagnostic test fails, return to table 5-2, Repair Procedure, and perform the steps under section C, Diagnostic ROM Tests.
6. Press key [A] or [X] to put the HP-75 into Light Sleep Test mode.	
7. Press key [2] or [E] to run the Auto test. Allow the unit to run for at least one cycle.	If any test fails, return to table 5-2, Repair Procedures, under section C, Diagnostic ROM Tests.
8. Press [SHIFT][ATTN].	
9. Remove the diagnostic ROM.	
10. Remove the unit from the diagnostic fixture.	

Table 5-3. Operational Verification (Continued)

STEP	ACTION
11. Place the unit in the display adjustment fixture with the unit assembled, but with the battery out and the back case off.	
12. Plug the recharger into the unit and turn the unit on.	
13. Fill the display with "1"s by pressing and holding the [1] key.	
14. While looking through the operator's window, press the button that turns on the light.	
15. Adjust R23 with a small screw driver until the middle segment of the bottom row of dots of each character darkens slightly.	
16. Assemble the case.	
17. Reinstall the memory module if the unit came in with one.	
18. Reinstall the battery.	

Table 5-3. Operational Verification (Continued)

STEP	ACTION
19. Type "copy card to 'verify'" then press [RTN].	
20. Type "run 'verify'".	If "OK!!!" is displayed, the unit is good. If "BAD" is displayed, return to table 5-2, Repair Procedures, and repeat the entire set of procedures. Then return to step 1 of this table to verify the operation of the unit.
21. Press and hold [SHIFT] [CTL] [CLR] for two seconds.	
22. Reinstall any plug-in modules that came in with the unit.	

Table 5-4. Diagnostic ROM Error Messages

ERROR CODE	COMMENTS	Assembly Replacement Priority*		
		PWR/RAM (A1)	LOGIC (A2)	DISPLAY (A3)
TEST: CPU				
CPU BAD 'x'	If x is A thru M or O thru T, then check all solder connections on A2U3, A2U4, and A2U2.	2	1	0
	If x is N, then check all solder connections on A2U6, A2U7, and on all RAM ICs.	2	1	0
TEST: RAM				
RAM 'x' BAD	If 'x' is any letter from A thru H, check solder connections on the system RAM on the power supply/RAM PCA.	1	2	0
	If 'x' is any letter from I thru L, replace the memory module.	0	0	0
	If 'xxK of RAM' is displayed and the test will not proceed further, check to see if a key is stuck down. If the keyboard is OK, then check all solder connections on A2U2.	0	1	0

Table 5-4. Diagnostic ROM Error Messages (Continued)

ERROR CODE	COMMENTS	Assembly Replacement Priority*		
		PWR/RAM (A1)	LOGIC (A2)	DISPLAY (A3)
TEST: ROM				
ROM 'x' BAD	Check all solder connections using the following table:			
	if x is 0, A2U8	0	1	0
	if x is 1, A2U9	0	1	0
	if x is 2, A2U10	0	1	0
	if x is 3, A2U11	0	1	0
	if x is 4, A2U12	0	1	0
	if x is P4B, A2U13	0	1	0
	If x is P1A, P1B, P2A, P2B, P3A, or P3B, then remove and replace the plug-in ROM.	0	0	0
TEST: KEYBOARD				
xxxx KEY BAD	First replace the top case. Check all solder connections on A2U2, A2U3, and A2U4.	0	2	0
KEYBOARD BAD	First replace the top case. Check all solder connections on A2U2, A2U3, and A2U4.	0	2	0

Table 5-4. Diagnostic ROM Error Messages (Continued)

ERROR CODE	COMMENTS	Assembly Replacement Priority* PWR/RAM (A1)	LOGIC (A2)	DISPLAY (A3)
TWO KEY ROLLOVER BAD	Check all solder connections on A2U2, A2U3, and A2U4.	0	1	0
KEYBOARD INTERUPT BAD	Check all solder connections on A2U2, A2U3, and A2U4.	0	1	0
KEYBOARD MULTIRUPT BAD	Check all solder connections on A2U2, A2U3, and A2U4.	0	1	0
TEST: REAL-TIME-CLOCK/COMPARITOR				
RTC BAD	Check all solder connections on A2U2.	0	1	0
GLOBAL DISABLE BAD	Check all solder connections on A2U2.	0	1	0
COMPARITOR BAD	Check all solder connections on A2U2.	0	1	0
TEST: MAR				
MAR BAD	Check all solder connections U6 and U7.	0	1	0

Table 5-4. Diagnostic ROM Error Messages (Continued)

ERROR CODE	COMMENTS	Assembly Replacement Priority*		
		PWR/RAM (A1)	LOGIC (A2)	DISPLAY (A3)
TEST: DEEP SLEEP				
RAM 'x' BAD	If 'x' is any letter from A thru H, check all solder connections on all system RAM.	1	2	0
	If 'x' is any letter from I thru L, replace the memory module.	0	2	0
Unit does not turn on again	Check all solder connections on A2U2, A2U3, and A2U4.	0	1	0
TEST: BATTERY LEVEL DETECT				
BATTERY LEVEL DETECT BAD	Check all solder connections on A2U2, A2U3, and A2U4.	0	1	0
TEST: LCD DRIVER				
Columns missing in the display	Check all solder connections on A2U1.	0	2	1
Bad display	Check all solder connections on A2U1.	0	2	1
Poor viewing	Adjust display during operational verification in table 5-3, steps 11 through 18.	0	0	0

Table 5-4. Diagnostic ROM Error Messages (Continued)

ERROR CODE	COMMENTS	Assembly Replacement Priority*		
		PWR/RAM (A1)	LOGIC (A2)	DISPLAY (A3)
TEST: LCD CONTROLLER				
Wrong characters	Check all solder connections on A2U1.	0	1	2
Missing row or lines	Check all solder connections on A2U1.	0	1	2
Bad display	Check all solder connections on A2U1.	0	1	2
No under-lining	Check all solder connections on A2U1.	0	1	2
TEST: HP-IL				
HP-IL ERROR: -POWER ON -REGISTER -DATA FRAME -END FRAME -IDY FRAME -RDY FRAME -CMD FRAME -IFCR FRAME -GLOB DIS -POWER OFF -OVAR BIT -FRNS BIT -SRQR BIT	Check all solder connections on A2U18 and A2U4.	1	2	0

Table 5-4. Diagnostic ROM Error Messages (Continued)

ERROR CODE	COMMENTS	Assembly Replacement Priority* PWR/RAM (A1)	LOGIC (A2)	DISPLAY (A3)
TEST: BEEP				
No beep	Inspect the speaker and its wires. If the speaker is damaged, replace it.	1	2	0
Wrong frequency	Inspect the speaker and its wires. If the speaker is damaged, replace it.	1	2	0
Erratic sound	Inspect the speaker and its wires. If the speaker is damaged, replace it.	1	2	0
TEST: NON-DESTRUCTIVE RAM				
(Same as RAM test, page 5-16.)				
TEST: DIAGNOSTIC ROM VERSION				
Wrong version	Replace with current version	0	0	0

*The numbers under the assembly replacement priority mean the following:

0 = Do not replace.
1 = Replace first.
2 = Replace second.

Table 5-5. "Test" Program Listing

```
10 ! TEST

20 DELAY 1

30 DISP 'CARDREADER TEST'@ DELAY1@ DISP'PLEASE WAIT'

40 ASSIGN #1 TO 'TEST1' @ FOR I=1 TO 41 @ PRINT #1; '********' @ NEXT I @
    PRINT #1; ''

50 ASSIGN #2 TO 'TEST2' @ FOR I=1 TO 41 @ PRINT #2; 'zzzzzzzz' @ NEXT I @
   PRINT #2; ''

60 COPY 'TEST1' TO CARD

70 COPY 'TEST2' TO CARD

80 DISP 'Finished'

90 END
```

Table 5-6. "Verify" Program Listing

```
10 ! VERIFY
20 X=RND*10+1 @ Y=RND*10+1
30 X=ABS(X)
40 X=ANGLE(X,Y)
50 X=ACOS(X)
60 X=FP(X)
70 X=ASIN(X)
80 X=FP(X)
90 X=ATN(X)
100 X=COS(X)
110 X=COT(X)
120 X=CSC(X)
130 X=DEG(X)
140 X=EXP(X)
150 X=FLOOR(X)
160 X=INT(X)
170 X=LOG(X)
180 X=IP(X)
190 X=LOG10(X)
200 X=MAX(X,Y)
210 X=MOD(X,Y)
220 X=RAD(X)
230 X=RMD(X,Y)
240 X=SEC(X)
250 X=SIN(X)
260 X=SQR(X)
270 X=TAN(X)
280 IF X=1.30601000859 THEN DISP 'OK!!!' ELSE DISP 'Bad'
290 END
```

SECTION
VI

Accessories

6-1. INTRODUCTION

6-2. This section identifies electrical accessories that are available for the HP-75 Portable Computer. Defective accessories should be replaced rather than repaired since the cost of a new unit is usually less than the cost of repair.

6-3. HP 82001B BATTERY PACK

6-4. The HP 82001B Battery Pack is shown in figure 6-1. This is the same battery pack used in the HP-35, HP-45, HP-65, and HP-80.

6-5. The serial number located on the battery pack indicates the week that the pack was initially charged. The format is described below:

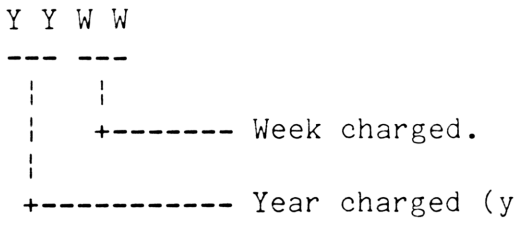


Figure 6-1. HP 82001B Battery Pack

6-6. To determine if the battery pack is bad or merely needs charging, perform the procedure in table 6-1.

Table 6-1. Battery Troubleshooting

STEP	SPECIFICATION	ACTION
1. Attach an 18-ohm, 2W resistor to the terminals of the voltmeter.		
2. Measure the voltage of the battery pack.	greater than or equal to 3.6V	If in range, then battery is good. If below range but greater than or equal to 3.3V, charge the battery for 30 minutes and repeat this step. If between 3.0V and 3.3V, charge the battery for 8 hours and stop here. If less than 3.0V, proceed to step 3.
3. Charge the battery for 5 minutes.		
4. Remove the resistor from the voltmeter.		
5. Measure the voltage of the battery pack.	greater than or equal to 3.6V	If in range, charge the battery for 8 hours and stop here. If below range, replace the battery.

6-7. RECHARGERS

6-8. Various ac rechargers (table 6-2 and figure 6-2) are available for use with the HP-75 Portable Computer. These rechargers are the same as those used on HP 82161A, HP 82162A, and other HP-IL peripherals.

Table 6-2. Rechargers

MODEL NUMBER	VOLTAGE*	IDENTIFICATION
HP 82059B	110	US
HP 82066B	220	Europe
HP 82067B	220	UK desktop
HP 82067B Opt 001	220	UK with RSA plug
HP 82068B	220	Australia
HP 82069B	110	Europe

* Indicates nominal voltage; acceptable ranges are 210 to 250 Vac and 90 to 120 Vac.

6-9. The serial number located on the recharger indicates the month that the unit was manufactured. The format is described below:

```
Y Y M M
--- ---
 ¦   ¦
 ¦   +------- Month manufactured.
 ¦
 +----------- Year manufactured (years since 1960).
```

6-10. To determine whether the recharger is functioning properly, perform the procedure in table 6-3.

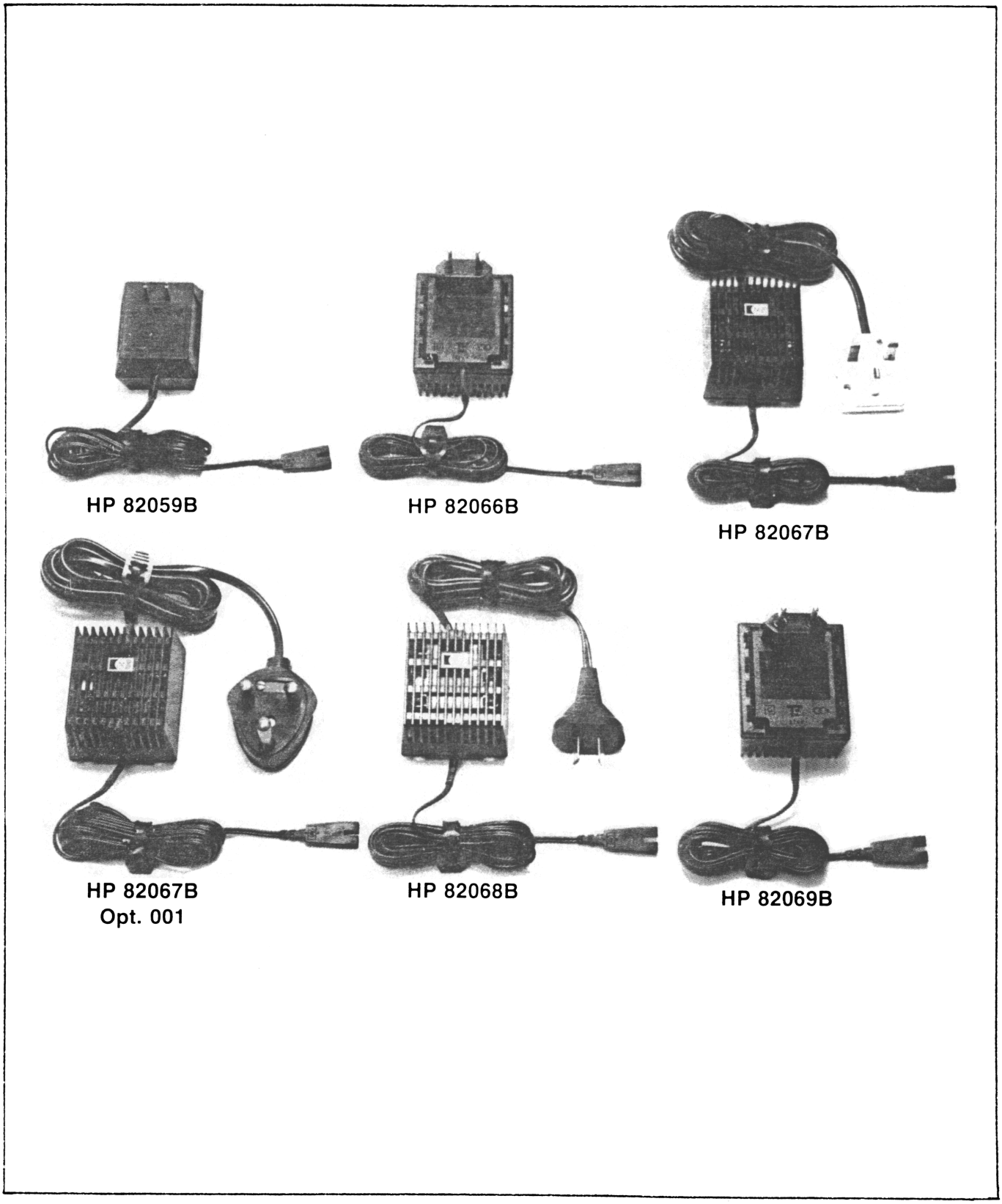


Figure 6-2. Rechargers

Table 6-3. Recharger Troubleshooting

STEP	SPECIFICATION	ACTION
1. Plug the recharger into an outlet of the proper voltage. Refer to table 6-2.		
2. Measure the output voltage with an ac voltmeter.	9.9 to 13.3 Vac for an input voltage of 110 Vac or 220 Vac*	If in range, proceed to step 3. If out of range, replace the recharger and stop testing here.
3. Connect a 12-ohm, 5%, 5W resistor to the terminals of the voltmeter.		
4. Measure the output voltage.	5.3 to 7.3 Vac for an input voltage of 110 Vac or 220 Vac+	If in range, proceed to step 5. If out of range, replace the recharger and stop testing here.
5. While measuring the voltage, wiggle and pull the wire at the transformer and at the connector.	greater than or equal to 5.3 Vac	If in range, the recharger is good. If drops below range, replace the recharger.

* More generally, VOUT should equal (VIN / 110) x 11.6 Vac $\pm$ 1.7V or (VIN / 220) x 11.6 Vac $\pm$ 1.7 V. (VIN is the ac voltage of the power outlet.)

\+ More generally, VOUT should equal (VIN / 110) x 6.3 Vac $\pm$ 1.0V or (VIN / 220) x 6.3 Vac $\pm$ 1.0 V. (VIN is the ac voltage of the power outlet.)

SECTION
VII

Replaceable Parts

7-1. INTRODUCTION

7-2. This section lists the replaceable parts and assemblies of the HP-75 Portable Computer. The reorder part number of the complete HP-75 unit is 00075-69902.

7-3. Parts descriptions, HP part numbers, quantities, and reference designations (where applicable) for the HP-75 are listed in table 7-1. (The computer is illustrated in figure 7-1.)

7-4. ORDERING INFORMATION

7-5. To order replacement parts or assemblies, address your order or inquiry to Corporate Parts Center or Parts Center Europe. Specify the following information for each part ordered:

a. Product model and serial number.

b. HP part number.

c. Part description.

d. Complete reference designation (if applicable).

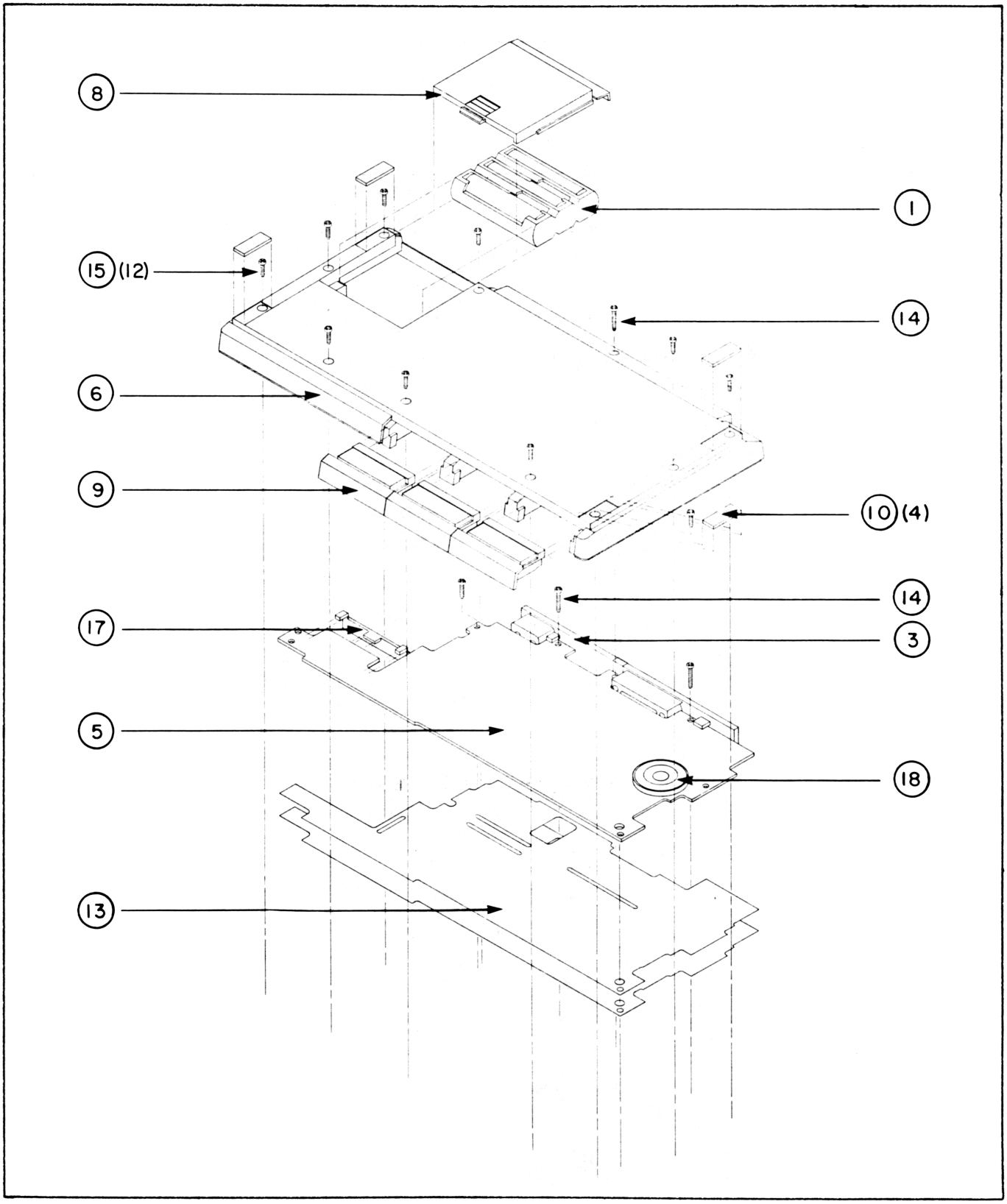


Figure 7-1. HP-75 Portable Computer Exploded View

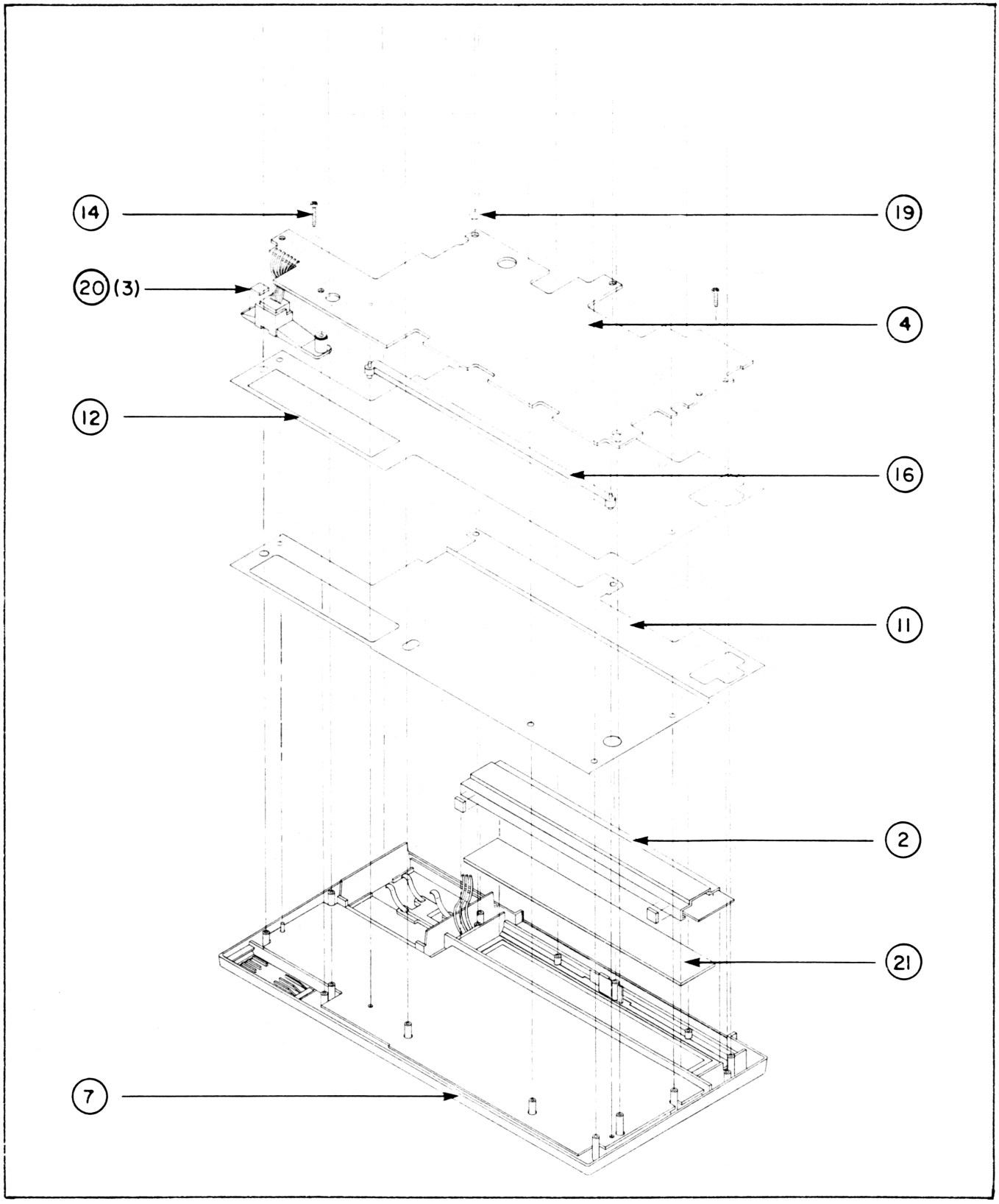


Figure 7-1. HP-75 Portable Computer Exploded View (Continued)

Table 7-1. HP-75 Portable Computer Replaceable Parts

INDEX NUMBER, FIGURE 7-1	HP PART NUMBER	DESCRIPTION	QUANTITY
	82700-69901	ASSEMBLY, 8K RAM	1
1	82001-60001	ASSEMBLY, battery pack	1
2	00075-69007	ASSEMBLY, display, exchange	1
3	00075-60910	ASSEMBLY, I/O plate	1
4	00075-69044	ASSEMBLY, 16K logic PCA, exchange	1
5	00075-69043	ASSEMBLY, 16K power supply/RAM PCA, exchange	1
6	00075-60912	CASE, bottom, service	1
7	00075-60909	CASE, 16K top, service	1
8	00075-60908	DOOR, battery, service	1
9	00075-60911	DUMMY ROM, service	3
10	0403-0432	FOOT	4
11	1600-1284	GROUND PLANE	1
12	0330-0357	INSULATOR, ground plane	1
13	4114-0992	INSULATOR, plastic sheet	2
	0510-0160	NUT, hex, double-chamfer	1
14	0624-0306	SCREW, self-tapping 2-28	4
15	0624-0503	SCREW, tapping	12
	2200-0728	SCREW, machine 4-40	1
16	00075-40012	SPACE STRIP	1
17	00075-40015	SPACER, RAM	1
18	9164-0133	SPEAKER, 1.125"	1
19	0380-1542	STANDOFF	1
20	0460-1791	TAPE, foam	3
21	1000-0620	WINDOW	1

SECTION
VIII

Reference Diagrams

8-1. This section includes reference diagrams for the HP-75 Portable computer.

8-2. The component location diagrams for the Power Supply/RAM PCA and Logic PCA are shown in figures 8-1 and 8-3 respectively. (Replaceable parts are listed in section VII.)

8-3. The schematic diagrams for the Power Supply/RAM PCA, Logic PCA, and Display PCA are shown in figures 8-2, 8-4, and 8-6 respectively.

8-4. The signal lines to all ICs and connectors are shown in figure 8-5.

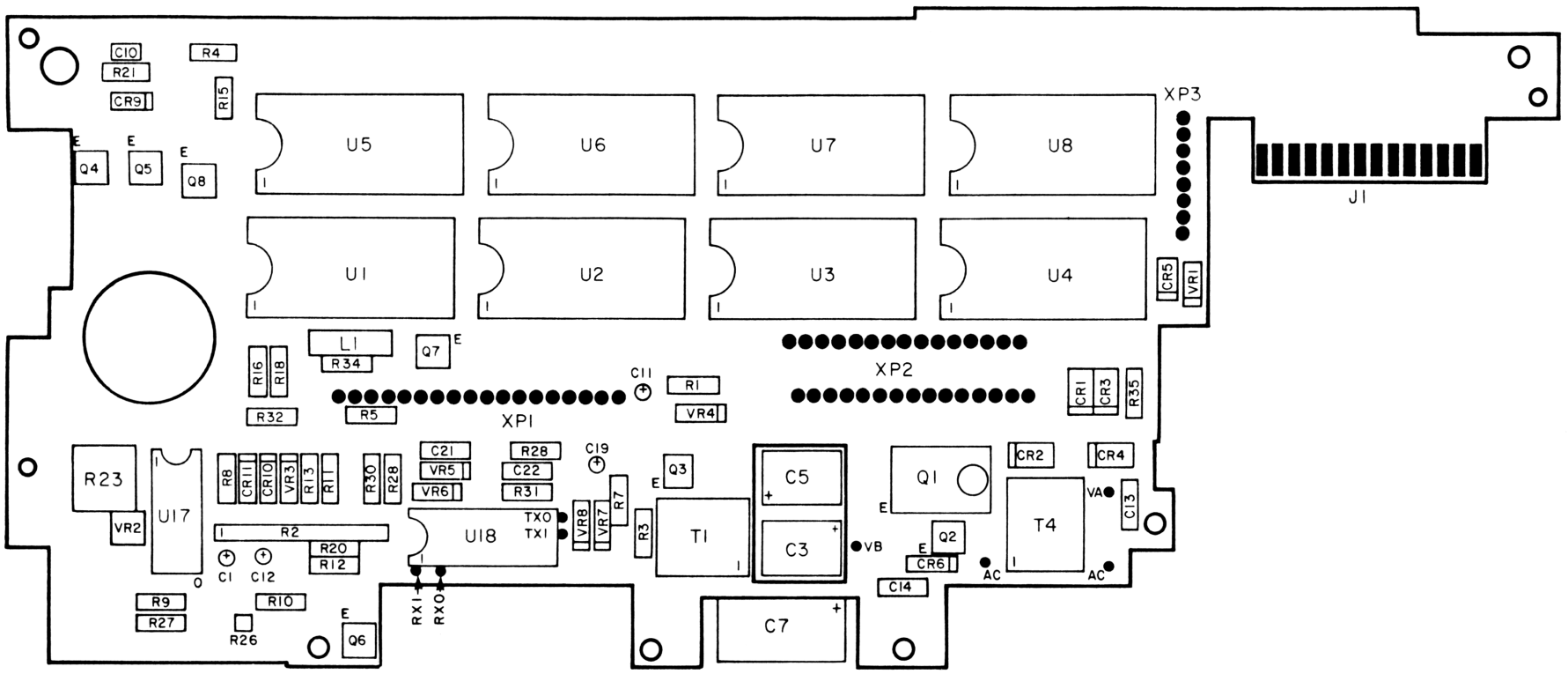


Figure 8-1. Power Supply/RAM PCA Component Location Diagram

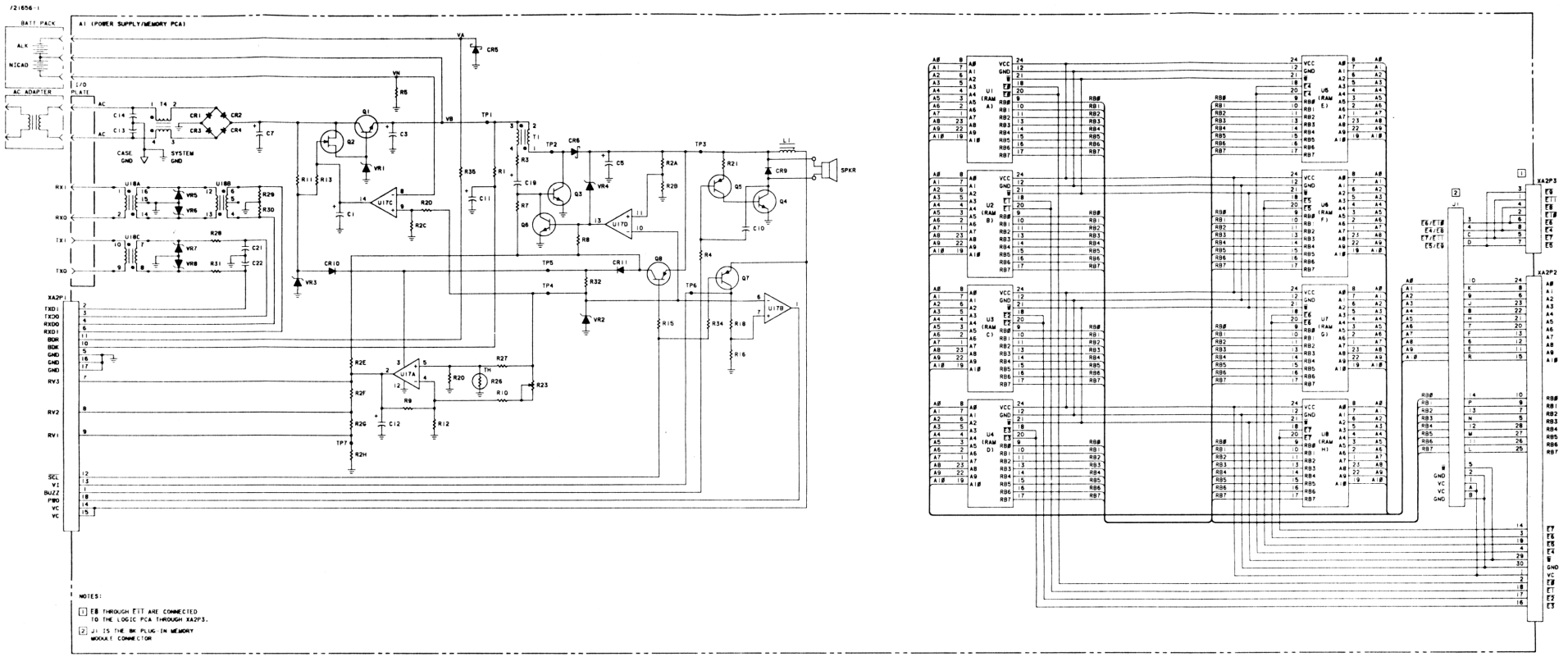


Figure 8-2.
Power Supply/RAM PCA Schematic

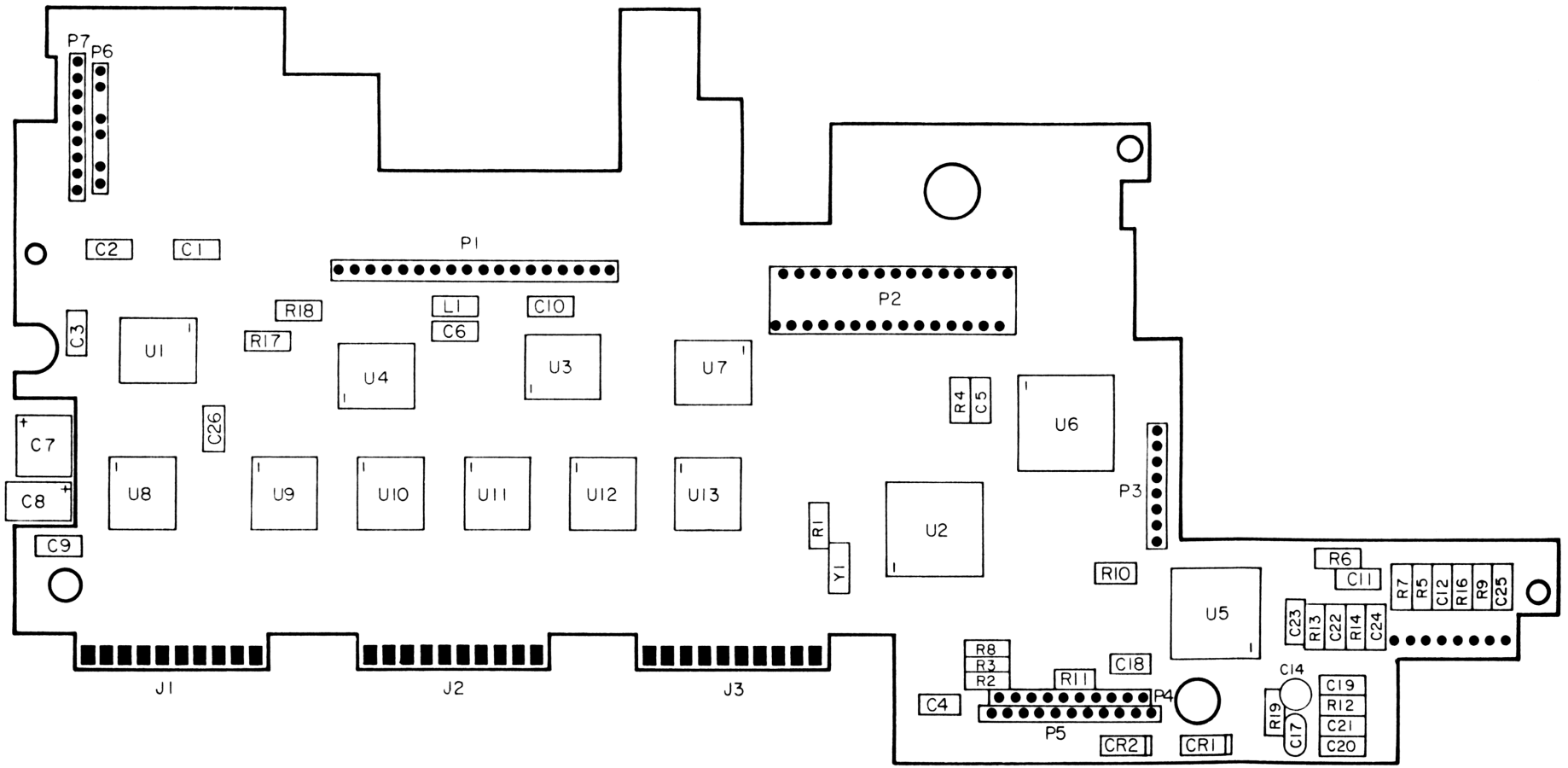


Figure 8-3. Logic PCA Component Location Diagram

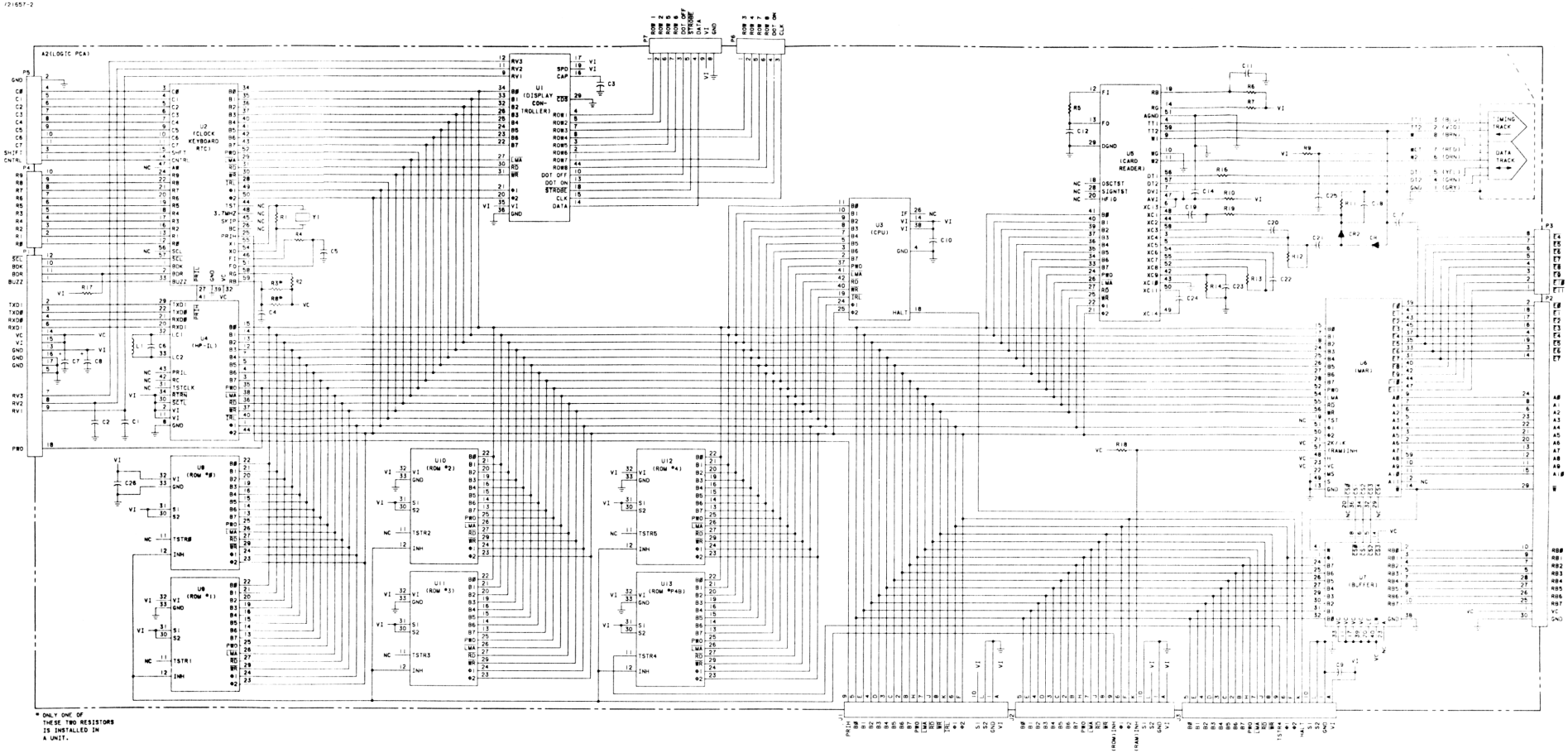
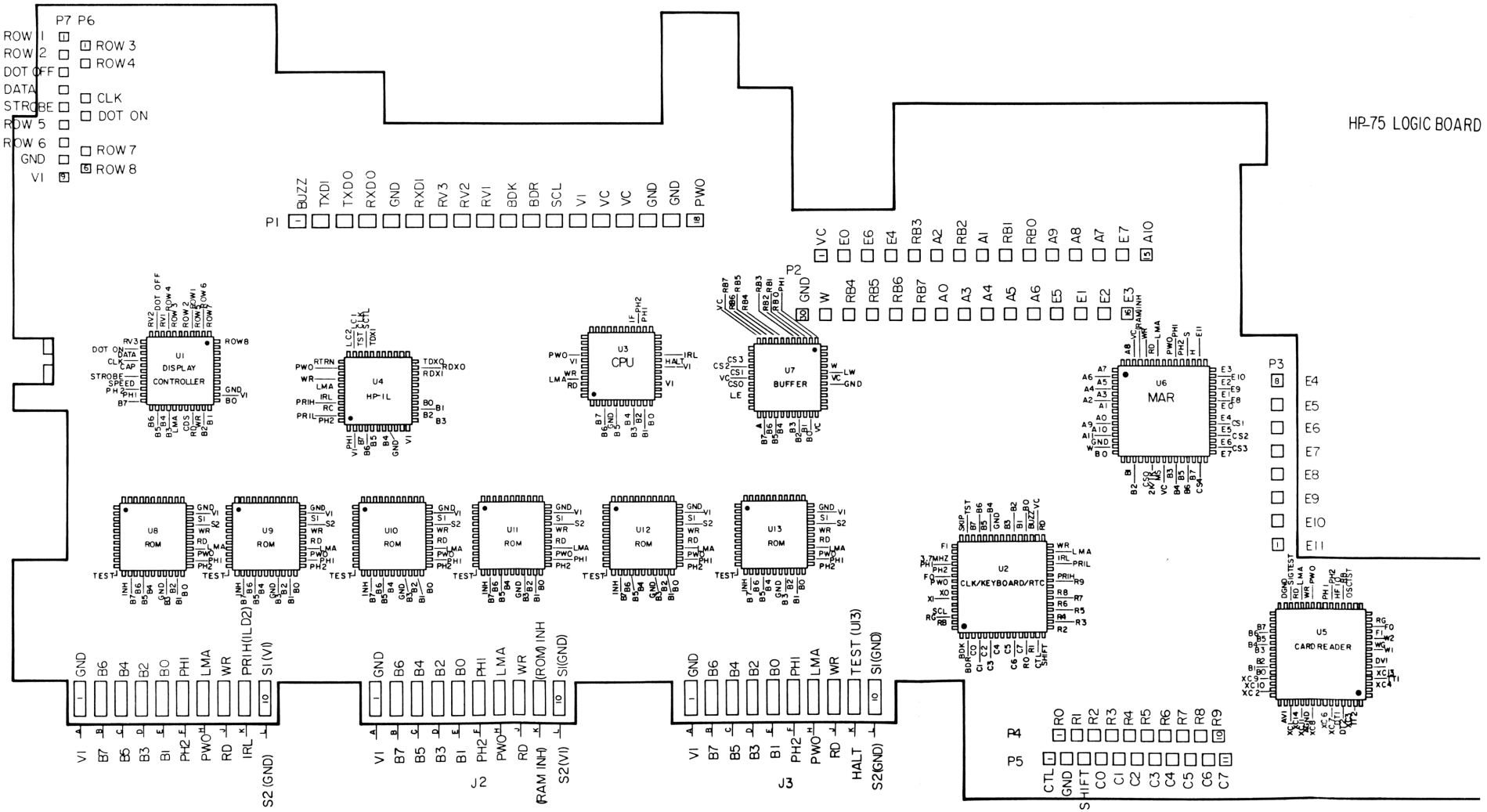


Figure 8-4.
Logic PCA Schematic


HP-75 LOGIC BOARD
P7 P6
ROW 1
ROW 2
DOT OFF
DATA
STROBE
ROW 5
ROW 6
GND
VI
ROW 3
ROW 4
CLK
DOT ON
ROW 7
ROW 8
P1
BUZZ
TXDI
TXDO
RXDO
GND
RXDI
RV3
RV2
RV1
BDK
BDR
SCL
VI
VC
VC
GND
GND
PWO
P2
P3
P4
P5
U1 DISPLAY CONTROLLER
U2 CLK/KEYBOARD/RTC
U3 CPU
U4 HP-IL
U5 CARD READER
U6 MAR
U7 BUFFER
U8 ROM
U9 ROM
U10 ROM
U11 ROM
U12 ROM
U13 ROM
J2
J3
S2 (GND)
S2(VI)
(RAM INH)
(ROM) INH
HALT
TEST (UI3)
S2(GND)
SHIFT

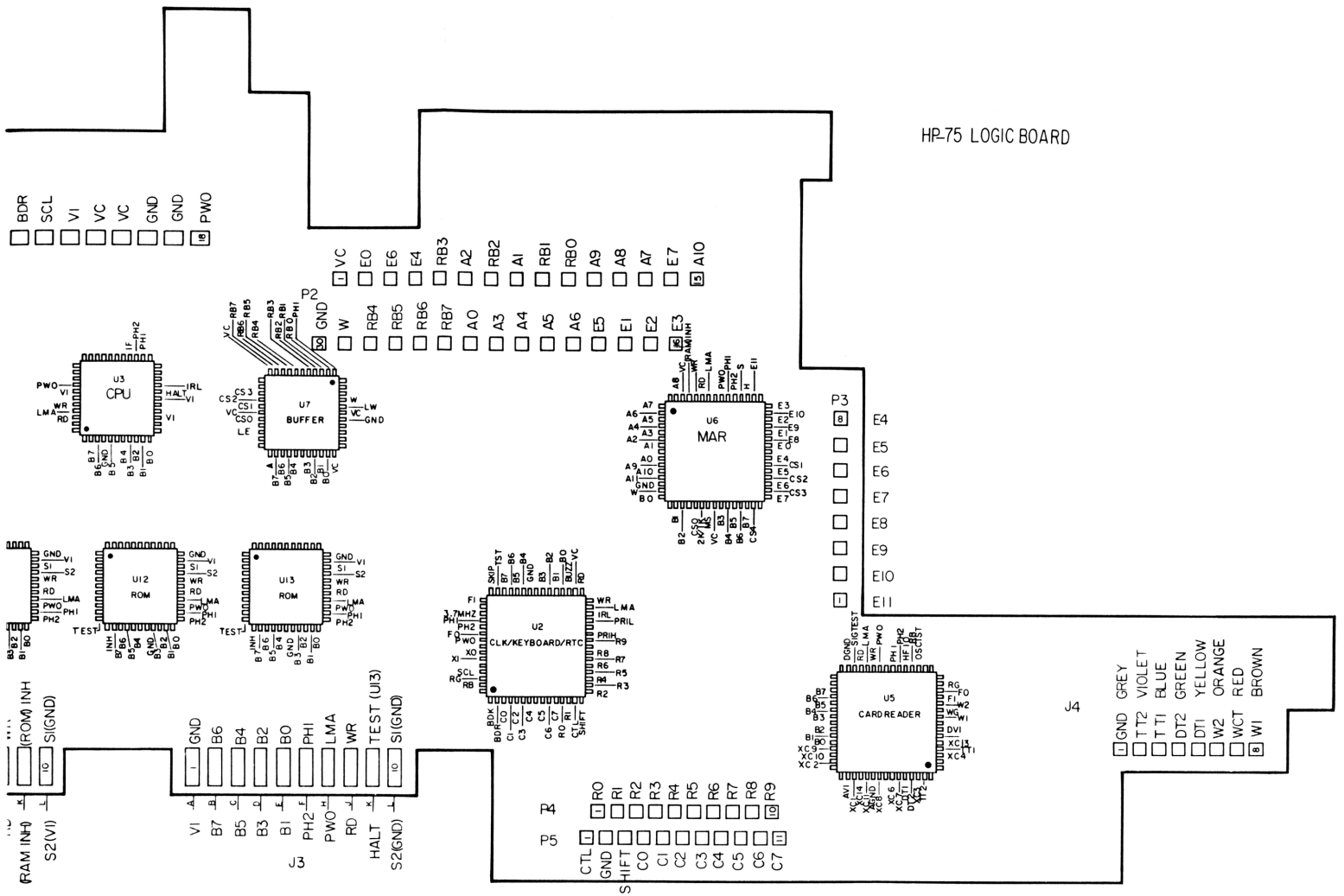


Figure 8-5.
Logic PCA Signal Lines

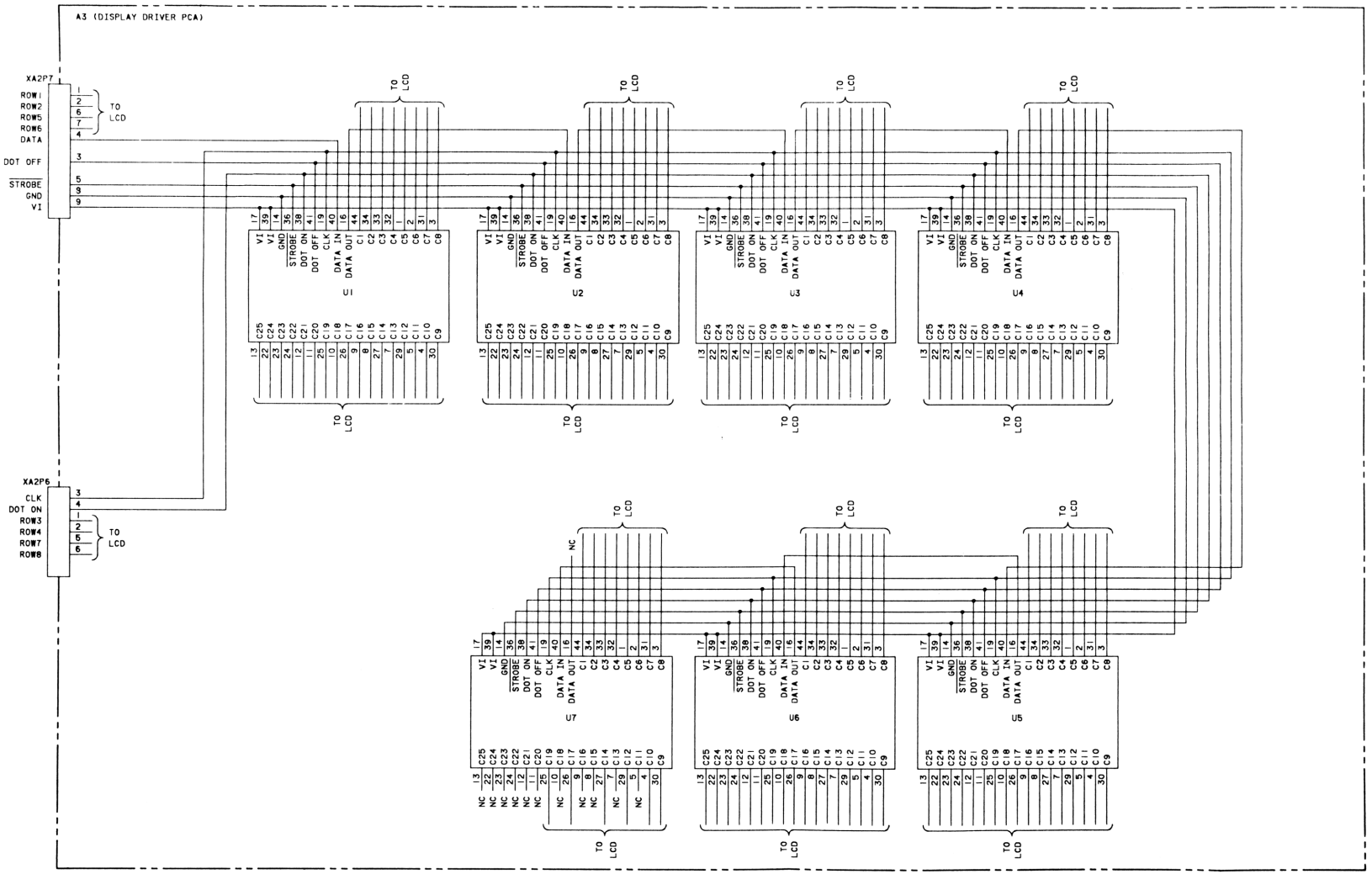


Figure 8-6.
Display PCA Schematic

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00075-90052

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