HP 82713A

Plug-In Module Simulator

SERVICE MANUAL

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General Information

1-1. INTRODUCTION

1-2. This service manual contains information to help you troubleshoot and repair the 82713A Plug-in Module Simulator (PMS).

1-3. This section describes the PMS and outlines how to use this manual.

1-4. The remainder of this manual is divided into 6 sections:

- A description of the 82713A and how it operates (section II).
- Assembly/disassembly procedures (section III).
- A description of the software diagnostics (section IV).
- Troubleshooting procedures (section V).
- List of replaceable parts (section VI).
- Reference diagrams (section VII).

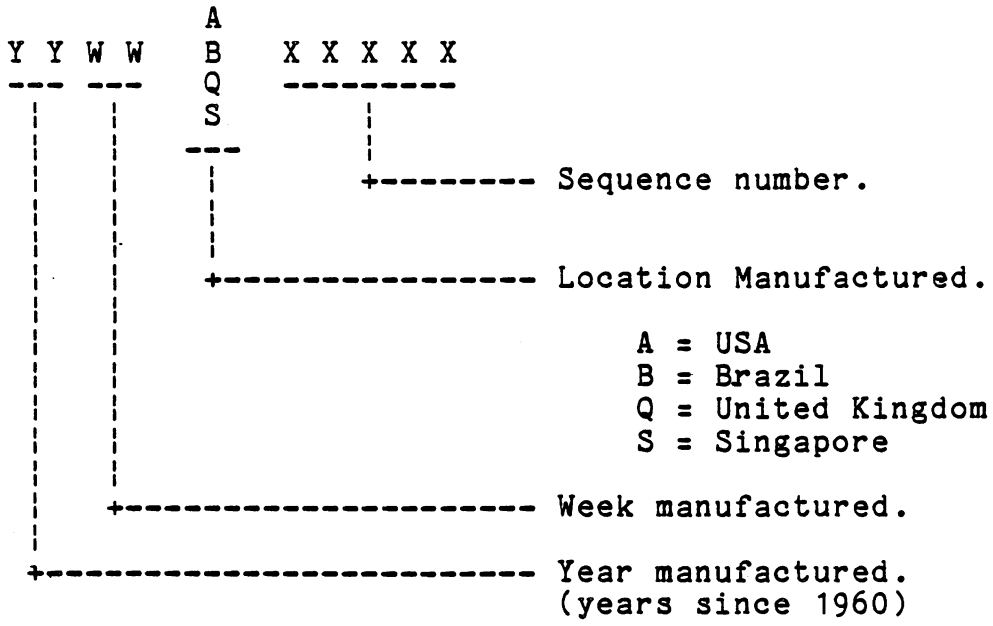
1-5. Before using this manual in actual repair, read through sections I and II to become familiar with the PMS and it's operation. Then read sections through V to become familiar with the repair procedures.

Table 1-1. Specifications

Environmental Limits o Operating Temperature: -20 to 55 degrees C (-4 to 131 degrees F) o Storage Temperature: -40 to 75 dgrees C (-40 to 167 degrees F) o Operating Humidity: 95 percent at 40 degrees C o Storage Humidity: 90 percent at 65 degrees C
Power o Typical: 25mW (both banks cleared)

1-6. IDENTIFICATION

1-7. The serial number of the module is used for identification and determination of the warranty status. It is located at the center of the bottom case. Its format is shown below:



SECTION
II

Theory of Operation

2-1. FUNCTIONAL DESCRIPTION

2-2. The HP 82713A Plug-in Module Simulator is designed to be a functional equivalent of a plug-in ROM for the HP-75. The PMS however, adds the feature of being able to be written to.

2-3. The PMS consists of 5 primary circuits:

- o Buffer Circuit
- o MAR (Memory Address Register)
- o I/O Decode Logic
- o RAM (Random Access Memory)
- o Power Supply

2-4. The PMS is organized into 2 major assemblies:

- o Logic PCA (Printed Circuit Assembly)
- o Connector/Cable Assembly

2-5. The Logic PCA contains the following:

- o 2 8K-Byte banks of RAM
- o Power Supply
- o Address/Latch Counter
- o Timing Logic
- o Control Logic
- o Bank Enable Logic
- o Enable Clock Logic
- o Write Enable Logic
- o RAM Select Logic

2-6. The Connector/Cable Assembly contains the following:

- o Bidirectional Buffer
- o Unidirectional Buffer
- o EMI (Electro-Magnetic Interference) circuit
- o Cable

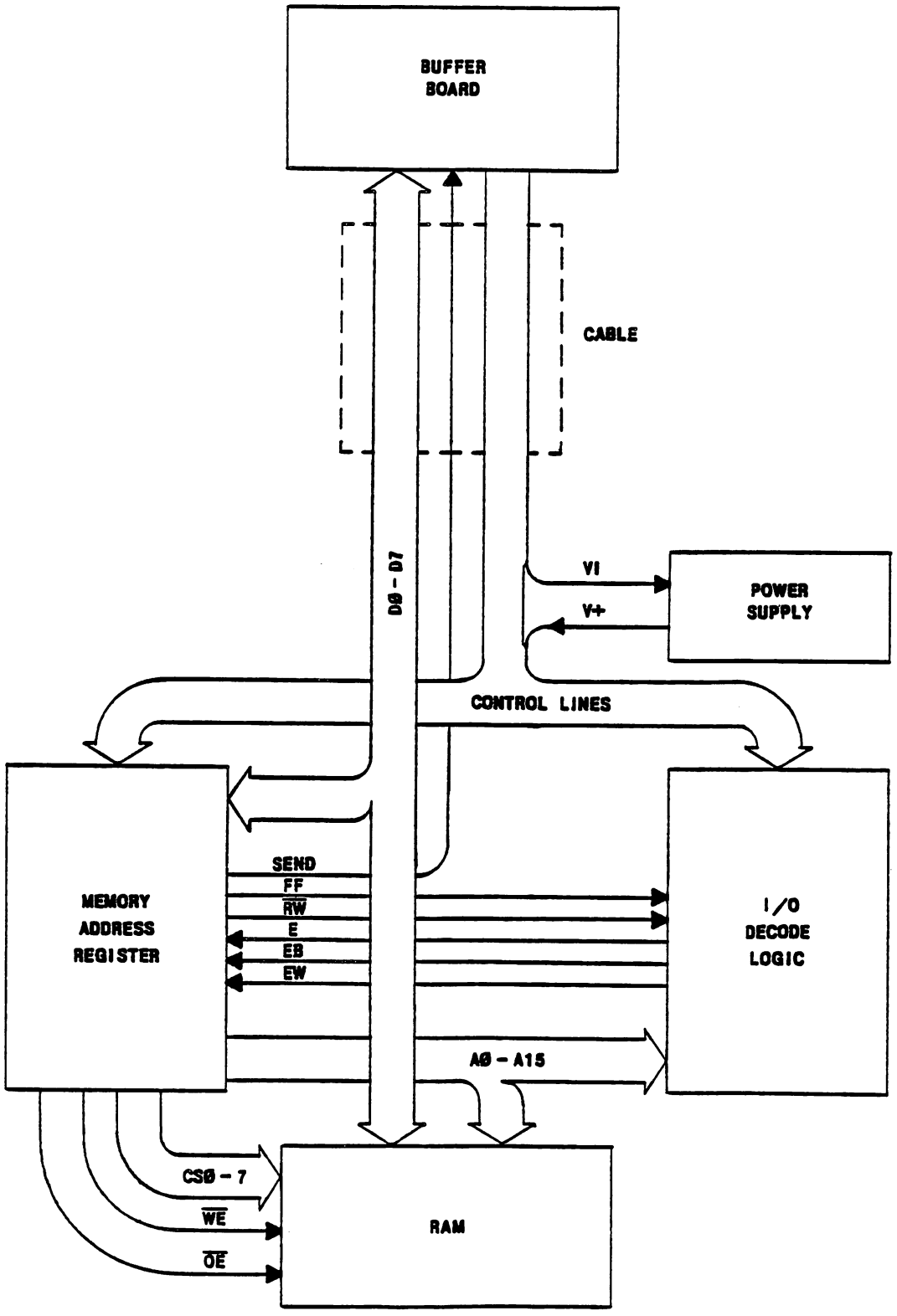


Figure 2-1. HP 82713A System Block Diagram

2-7. RAM

2-8. The PMS contains 16K-Bytes of RAM organized in two banks of 8K-Bytes each. Each bank is independant of each other. Each is addressed seperately and controlled seperately. This allows the user to store files to, edit files, run files, or catalog each bank individually.

2-9. Each bank consists of four 2K-byte RAM chips. Each is addressed via an 11 bit address bus. Data is transferred to and from the RAM via an 8 bit data bus. Write Enable, Read Enable, and Chip Select lines are used to control the RAM.

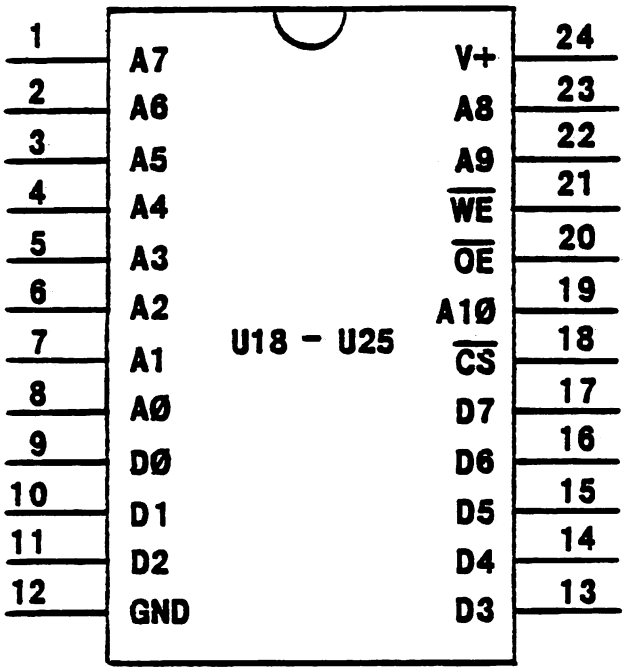


Figure 2-2. RAM

2-10. MAR

2-11. The Memory Address Register (MAR) consists of four circuits:

- o Address/Latch Counter
- o Control Logic
- o Timing Logic
- o RAM Select Logic

2-12. The MAR decodes address information from the HP-75 bus. The HP-75 sends out a 16 bit address whenever it wants to access the PMS. The MAR takes the 16 bits and generates the neccesary internal addressing select, and read/write information.

2-13. The Address/Latch Counter supplies a latched 16 bit address to the RAM and the I/O Decode Logic. This circuit recieves a 16 bit address from the HP-75 bus in 2 sequential bytes. The address is then latched into 4 counter chips (U5-U8). The outputs of U5-U8 are directly connected to the internal address bus. The address loaded into U5-U8 is then used by the RAM and I/O Decode Logic. The I/O Decode Logic uses 13 address bits (A0-A7, A11-A15) and the FF line in its Write, Clock, and Bank Enable circuits. The RAM uses 11 address bits (A0-A10) to address each of the four chips in both banks.

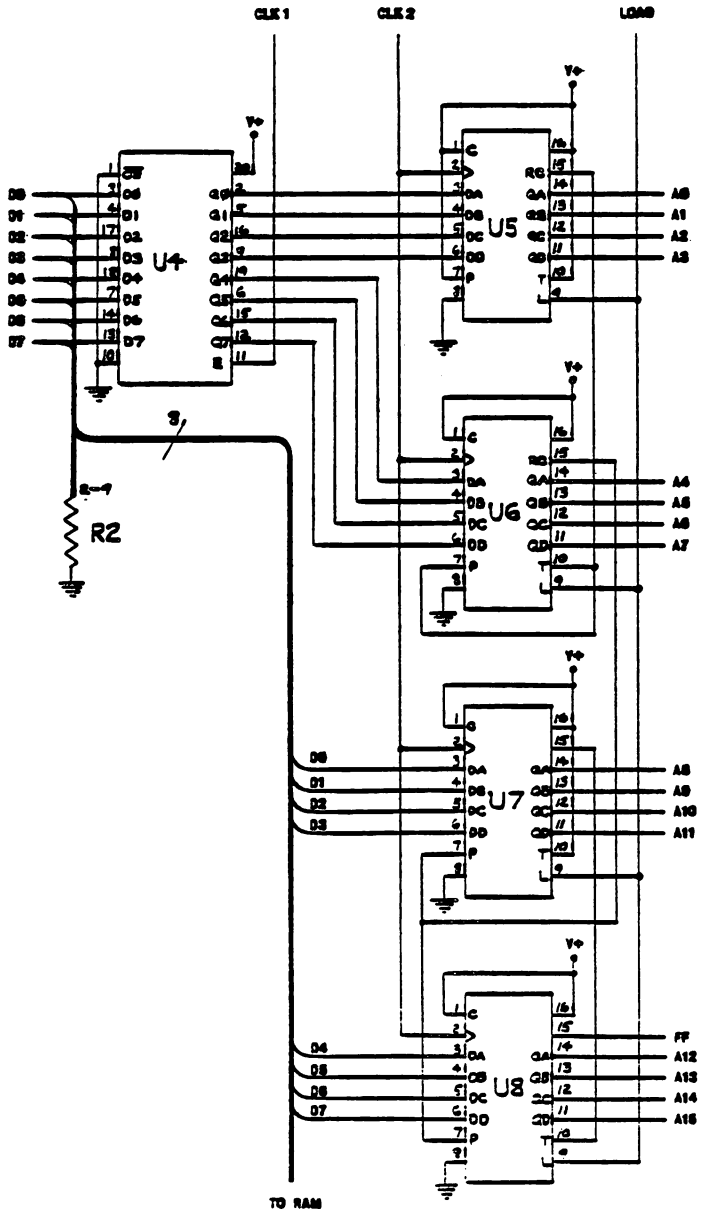


Figure 2-3. Address Latch Counter

2-14. The Control Logic demultiplexes and increments the 16 bit address from the HP-75 bus. When the HP-75 sends out an address, it is sent out in 2 seperate bytes. The first byte (least significant byte) is latched into a buffer (U4) when the LMA line from the 75 is pulsed. When the LMA line is pulsed a second time, the first byte in U4 and the second byte now on the HP-75 bus, are loaded into the counters (U5-U8).

2-15. The Control Logic circuit also increments U5-U8. This occurs when a read or write occurs on the HP-75 bus in the absence of an LMA pulse.

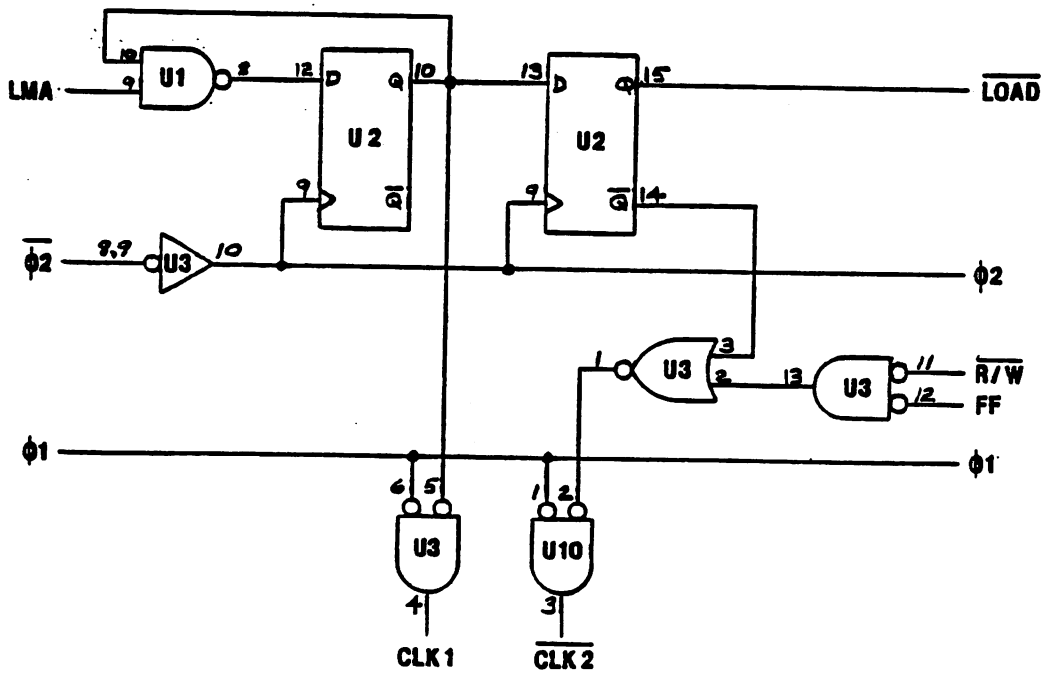


Figure 2-4. Control Logic circuit.

2-16. The Timing Logic generates the internal timing signals neccesary to synchronize the circuits within the PMS, and to synchronize the PMS and the HP-75. This circuit generate three signals; CTL, R/W, and READ. The CTL (control) line enables the RAM Select Logic. The R/W (read/write) line synchronizes the Control Logic and the Enable Clock Logic. It signifies either a read or write cycle, but not both. The READ line enables the Write Enable Logic when it goes high. It is also connected to the read line on the RAM IC's, thus controlling the duty cycle of the RAM chips.

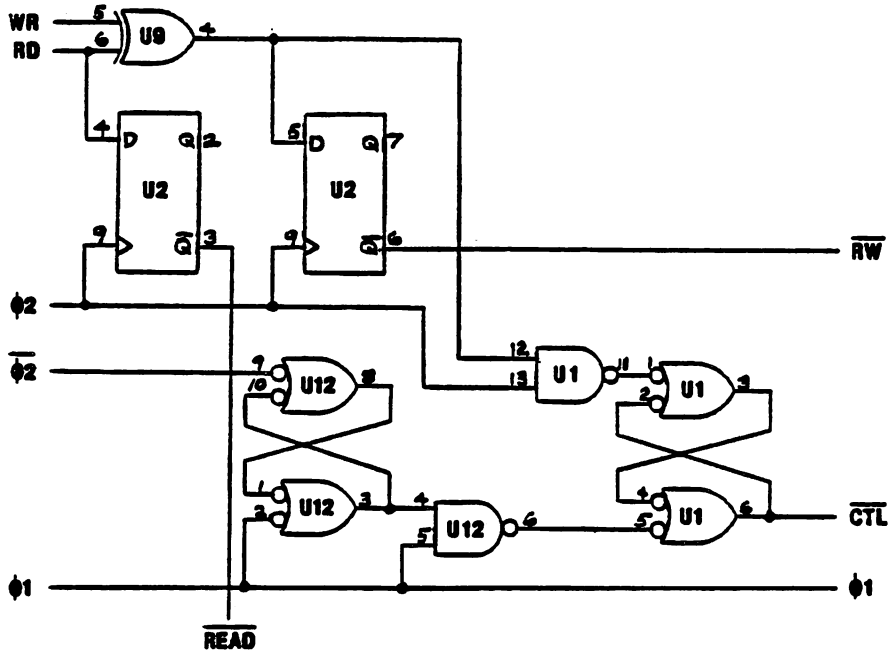


Figure 2-5. Timing Logic

2-17. The RAM Select Logic generates the select lines as well as the read and write signals for the RAM. U15 and U16 generates the 8 select lines from the 5 most significant bits of the Address/Latch Counter (A11-A15).

2-18. The SEND signal is also generated from the circuit. SEND is used to reverse the direction of the bidirectional buffer in the Connector/ Cable Assembly. SEND is asserted when the HP-75 has issued a read command to the PMS. The data lines are then reversed and data can be transfered from the PMS to the HP-75.

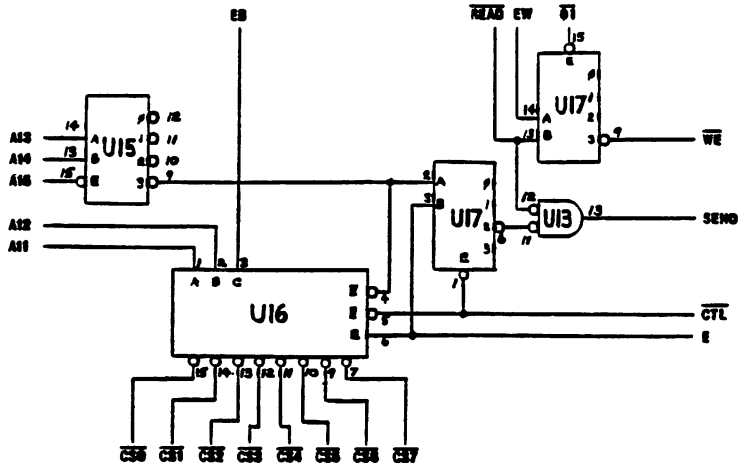


Figure 2-6. RAM Select Logic

2-19. I/O Decode Logic

2-20. The I/O Decode Logic consists of 3 circuits:

- o Enable Clock Logic
- o Bank Enable Logic
- o Write Enable Logic

2-21. The I/O Decode Logic monitors the address lines and several control control lines from the HP-75 bus. It decodes this information and enables or disables the appropriate bank of RAM. It also determines whether the bank is to be read or written to.

2-22. The Enable Clock Logic monitors the address lines looking for an address in the range FF40 to FF4F, and any even address in the range FF50 to FF5F. If either a read or write command is issued to any of these addresses, a clock pulse is generated to the Bank Enable Logic, and the Write Enable Logic.

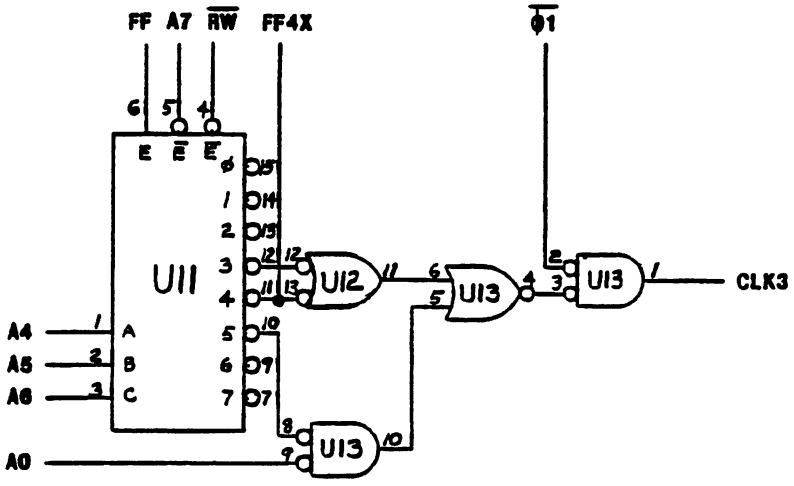


Figure 2-7. Enable Clock Logic

2-23. The Bank Enable Logic decodes the I/O address to determine which bank is being addressed. Only 2 addresses in the range FF40- FF4F will will enable a bank of RAM. (see table 2-1). Either bank can be enabled by a read or write to the appropriate I/O address. Any bank not being addressed when a clock pulse is recieved from the Enable Clock Logic will be disabled. When a bank is enabled by this circuit and the enable write (EW) line is not asserted, the bank can only be read from.

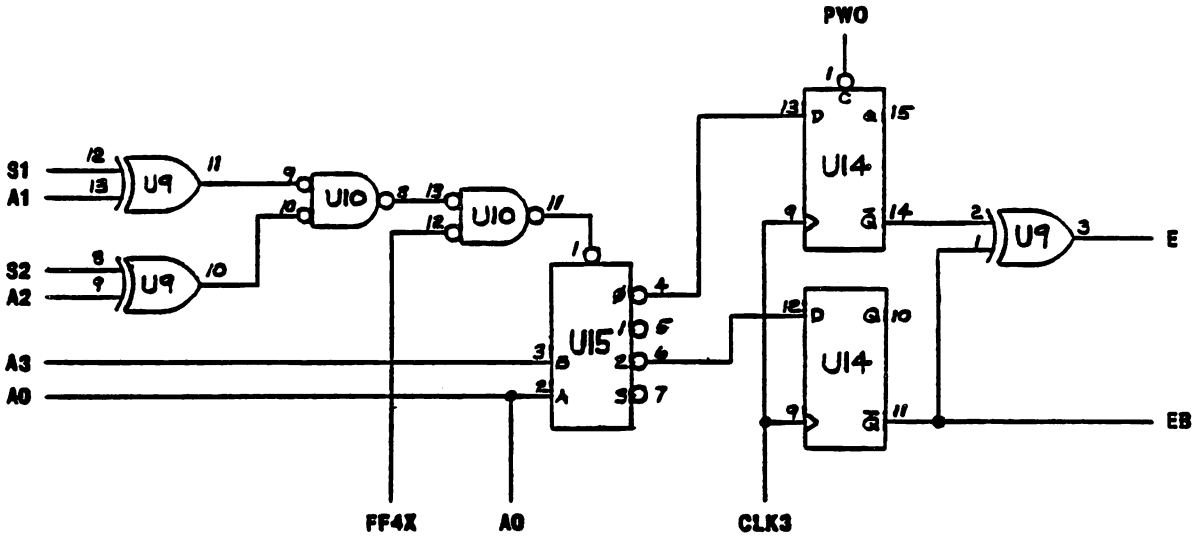


Figure 2-9. Bank Enable Logic

2-24. The Write Enable Logic allows the RAM to be written to. This circuit is set by accessing any even address the Enable Clock Logic recognizes (see table 2-1). The HP-75 can write to the PMS when the enable write (EW) line is asserted and a bank is selected (from the Bank Enable Logic).

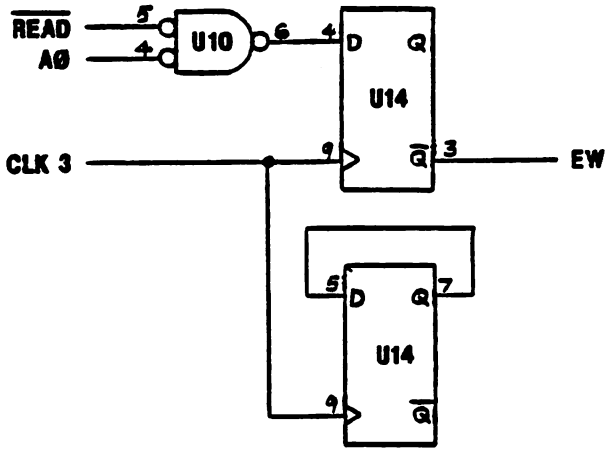


Figure 2-8. Write Enable Logic

2-25. Power Supply

2-26. The Power Supply provides power to the PMS when it is not powered by its primary source, the HP-75. When the PMS is not plugged into the HP-75, the Power Supply provides power to all of the circuits including the RAM. This maintains the contents of RAM making the PMS self-sustaining and portable.

2-27. The heart of the Power Supply is the battery (BT1). It is a single cell Lithium-Iodine type. It does not contain any liquid or gaseous chemicals. It exibits very long shelf life as well as being hardened against environmental extremes. It is enclosed in a laser sealed case. Its expected life is in excess of 5 years.

2-28. The Power Supply contains diode circuitry that automatically switches in. Whenever the PMS is plugged into the HP-75, the VI line is held high. This suppresses current flow through CR2 and essentially isolates the battery from the circuitry. Whenever VI is not powered (PMS removed from the HP-75), CR2 allows current from the battery to flow. The battery then energizes all of the IC's and maintains the RAM.

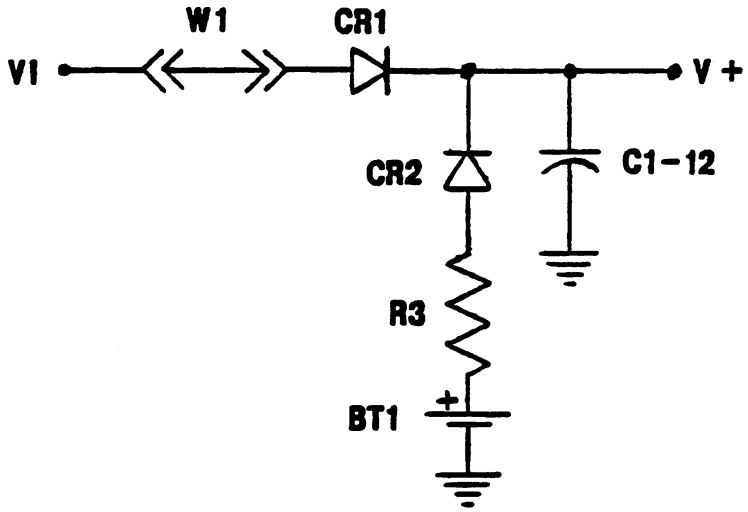


Figure 2-10. Power Supply

2-29. The Buffer Circuit Consists of the following circuits:

- o Unidirectional buffer
- o Bidirectional buffer
- o EMI circuitry

2-30. The Unidirectional buffer buffers the clock lines (phi 1, phi 2) and control lines (LMA, RD, WR) from the HP-75 bus before reaching the logic board. This insures that the load of the PMS is isolated from the HP-75 so that the 75 is not adversely affected in normal operation. The buffer used is an inverting type constructed in high speed CMOS. Typical time delay through the buffer is 10nsec.

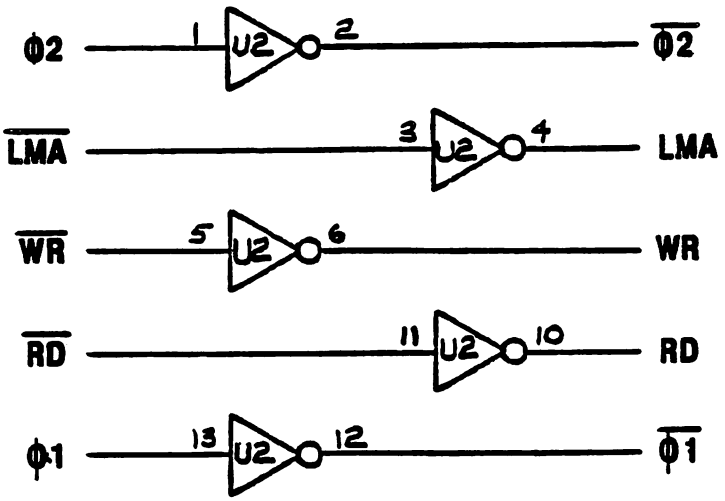


Figure 2-11. Unidirectional Buffer

2-31. The Bidirectional buffer allows data to be read and written to the PMS from the HP-75. U1 on the buffer board contains the neccesary circuitry to accomplish this (see figure 2-12). The direction of data flow is controlled by the SEND signal from the logic board. When the SEND signal is asserted, the buffer is enabled to allow data flow from the PMS to the HP-75. When SEND is not asserted, the buffer allows data to be sent from the HP-75 to the PMS.

2-32. The SEND signal is inverted on the buffer board and pulled to ground through a 1 Mohm resistor. This is done to insure that data may still flow to the PMS even when the SEND line is disconnected on the logic board. This allows the HP-75 to talk to the PMS for troubleshooting purposes.

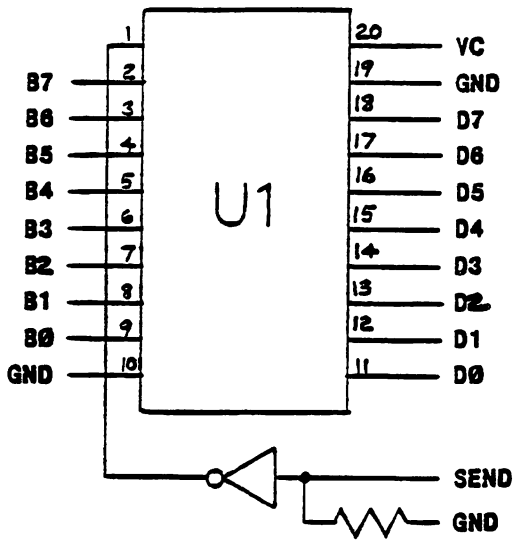


Figure 2-12. Bidirectional Buffer

2-33. The EMI Circuitry (see figure 2-13) is designed to isolate any noise generated from the PMS.

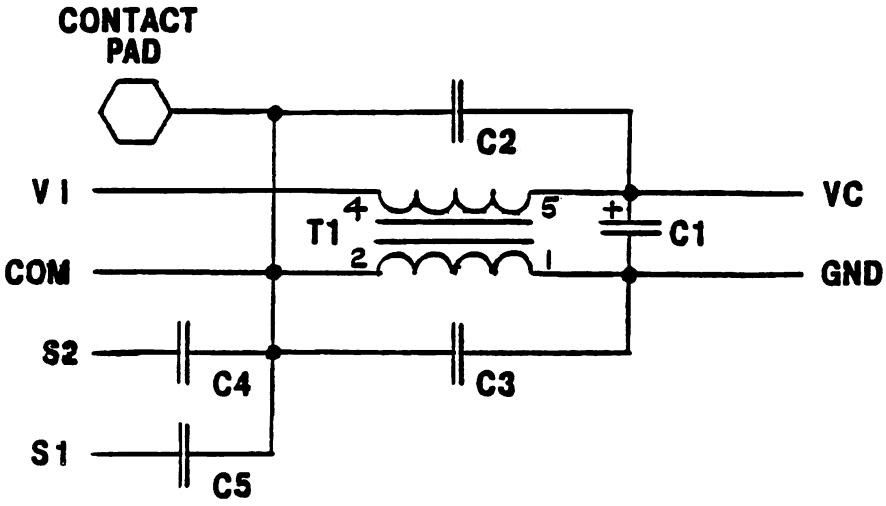


Figure 2-13 EMI Circuitry

2-34. The Cable connects the buffer board and the logic board. It contains 2[illegible] signal lines and is shielded from EMI and ESD (Electro-Static Discharge).

Table 2-1. 82713A I/O Enable Addresses

I/O Address Port 3 (left)	Port 2 (middle)	Port 1 (right)	Function
FF42	FF44	FF40	Enable Read/Write on Bank A
FF43	FF45	FF41	Disable Read/Write on Bank A
FF4A	FF4C	FF48	Enable Read/Write on Bank B
FF4B	FF4D	FF49	Disable Read/Write on Bank B

Table 2-2. Signal Names

A0-7	Address lines 0 thru 7.
CS0-7	Chip Select 0 thru 7.
CTL	Control line.
D0-7	Data lines 0 thru 7.
E	Enable
EB	Enable Bank line.
EW	Enable Write line.
LMA	Load Memory Address.
OE	Output Enable.
PWO	Power On.
RD	Read.
RW	Read/Write.
S1/S2	ROM Select lines.
WE	Write Enable.
WR	Write.
O1	Phase 1 clock.
O2	Phase 2 clock.

Disassembly and Reassembly

The following procedures describe the steps necessary to disassemble and reassemble the HP 82713A PMS in order to replace or repair components that are faulty:

- Opening the case (procedure 3-1).
- Removing the Logic board (procedure 3-2).
- Removing the Connector/Cable assembly (procedure 3-3).
- Removing the Battery (procedure 3-4).
- Assembling the Logic board and the Connector/Cable assembly (procedure 3-5).
- Assembling the case (procedure 3-6).

CAUTION

The ICs in the HP 82713A are easily damaged by ESD (Electro-Static Discharge) if adequate precautions are not taken. Observe these precautions:

- The surface of the repair bench must be grounded.
- Any tool used in the assembly, disassembly, or troubleshooting of the PMS must be grounded to the surface of the repair bench.
- All parts must be kept within their antistatic containers during storage and while being carried to the repair bench.
- While handling parts and assemblies, repair personnel must wear a wrist strap grounded to the surface of the repair bench.
- Use an air ionizer to drain static charge from the repair bench area.

3-1. OPENING THE CASE.

a. Ensure that the PMS is not plugged into any other device.

b. Place the unit on the bench so that the three screws and the bottom case are facing up and the Connector/ Cable Assembly is on your right.

c. Using a #2 Posidrive screwdriver, remove the three screws and lift off the bottomcase.

d. Remove the rear panel.

3-2. REMOVING THE LOGIC BOARD.

a. The board facing you is the Logic board.

b. Lift the Logic board out of the topcase with the Connector/Cable assembly attached.

Note: Do not lay the bare board on a conductive surface. This may cause shorting between pins and may damage the board. It is recommended that the Logic board be placed on a nonconductive surface, component side up for troubleshooting.

3-3. REMOVING THE CONNECTOR/CABLE ASSEMBLY.

a. Desolder the 20 leads of J1. Remove J1 from the Logic board.

b. Loosen the nuts on the cable clamp and remove the top of the cable clamp.

c. Lift the cable out of the clamp.

3-4. REMOVING THE BATTERY.

a. Desolder the three battery leads.

b. Remove the battery.

c. Solder a 50K ohm resistor across the battery terminals.

d. Dispose of in the normal manner.

Note: Do not incinerate or expose contents to water.

3-5. ASSEMBLING THE LOGIC BD. AND THE CONNECTOR/CABLE ASSEMBLY.

a. Lay the Logic board in the bottom case. Be sure the three screw holes in the Logic board are aligned with the three screw holes in the bottom case.

b. Align the Connector/Cable assembly so that the front panel slips into its slot in the bottom case, and the cable lays in the bottom half of the cable clamp.

c. Fasten the cable clamp around the cable.

d. Insert and solder J1 into the Logic board. Be careful not to stress J1 in any manner.

3-6. ASSEMBLING THE CASE.

a. Lay the Logic board, with the Connector/Cable assembly attached, in the top case component side down. Be sure the front panel is properly aligned in the top case.

b. Drop the rear panel into its slot in the top case, with the painted side facing out.

c. Align the bottom case over the topcase and press the two halves together.

d. Insert and tighten the three screws.

Diagnostic Software

4-1. INTRODUCTION

4-2. This section is a reference section that describes the diagnostic software, "713DIAG", and the way it tests the PMS. This software is used as part of the troubleshooting procedure in section 5.

4-3. USING THE DIAGNOSTIC SOFTWARE

4-4. "713DIAG" is contained on card. It first must be copied into the HP-75 that is being used to test the PMS in question.

4-5. "713DIAG" is a LEX file. It consists of a number of keywords which may be executed in a BASIC program or executed from the keyboard. For example, any of the keywords such as RAMTEST may be executed as follows:

1. Type:
   a)"10 RAMTEST"
   b) <rtn>
   c) <run>

2. Type:
   a)"RAMTEST"
   b) <rtn>

4-6. When using "713DIAG",only one PMS can be plugged into the test HP-75 and it must be plugged into the leftmost port on the 75. "713DIAG" does not talk to the other two ports.

4-7. DESCRIPTION OF THE DIAGNOSTIC SOFTWARE

"713DIAG" consists of the following keywords:

1. RAMTEST
2. VERIFY
3. POWER
4. ADRTEST
5. SELTEST
6. SIGNAL

4-8. RAMTEST

4-9. RAMTEST performs a comprehensive test of both banks of RAM in the PMS. It writes a test pattern to RAM, then reads it back and compares to see if the data it read back is correct. If an incorrect value is read back, the test is terminated and the address in RAM from which the error originated displayed. This write/read procedure is performed for both banks of RAM.

4-10. VERIFY

4-11. VERIFY allows you to determine if the contents of either RAM bank is maintained for an extended period of time. This test should only be run after RAMTEST. It compares the data stored in the PMS under test to the pattern written by RAMTEST.

4-12. POWER

4-13. POWER executes a worst case power drain loop in an PMS. It is used in conjunction with troubleshooting procedure in making worst case current measurments.

4-14. ADRTEST

4-15. ADRTEST is a continuous loop routine that writes a byte of data to every location in both banks of RAM. This routine aids in troubleshooting the RAM address circuitry by toggeling all of the address lines.

4-16. SELTEST

4-17. SELTEST is a continuous loop routine that writes and reads a byte of data to each RAM chip. This routine aids in troubleshooting by toggeling all of the RAM select lines.

4-18. SIGNAL

4-19. SIGNAL is a continuous loop routine that is used with the signature analysis routine in the troubleshooting procedure. It reads and writes a given data string to and from the PMS in a known repeating pattern. This then generates the signatures used in signature analysis.

Troubleshooting and Testing

5-1. INTRODUCTION

5-2. This section contains the procedures you should follow to isolate the cause of the problem in a PMS. It also gives the procedure to verify that a unit is good.

CAUTION

Ensure that adequate precautions are taken regarding electrostatic protection. Work at a bench setup that is electrostatically protected. Otherwise, components may be damaged.

Recommended Tools

HP PART/MODEL NUMBER	DESCRIPTION
82713-60902	Signature Analysis Tool
8710-0899	#1 Pozidrive Screwdriver
5004A	Signature Analyzer
1740 or equivalent	Oscilloscope with RF probe
HP-75C	Test Computer
82713-60903	Diagnostic Program "713DIAG"

5-3. This section contains seven tables. The first is table 5-1, Test Procedures. This table contains the neccesary information to thoroughly test an PMS. This table is the main backbone of the actual repair procedure. The six other tables contain troubleshooting procedures. Table 5-2 gives directions on how to remove the wire jumper W2, while Table 5-3 descibes how to reinsert W2. Table 5-4 describes the initial troubleshooting routine for a no turn on problem. Table 5-5 contains the signature analysis troubleshooting routine. Table 5-6 contains the RAM replacement procedure. Table 5-7 contains the procedure to use with a major no turn on problem.

5-4. When troubleshooting the PMS, start with table 5-1, Test Procedures. Sequentially follow the actions in this table. If an error occurs while troubleshooting the PMS, you will branch to the recommended table. After you have succesfully completed the recommended action, return to the step in table 5-1 from which you branched and repeat that step. For example, if a no turn on problem is encountered, branch to table 5-4. After performing the neccesary troubleshooting steps and replacing the bad part, return to step A in table 5-1 and repeat the entire step.

5-5. Signature Analysis is the primary method of troubleshooting the PMS. It is a unique procedure that allows the operator to easily track down a bad IC by monitoring the surrounding signal lines. SIGNAL, a software routine in "713DIAG", performs a known and repeatable set of operations within the PMS under test. These repeating operations set up unique signals known as "signatures" on each of the signal lines. It is these signatures that will tell whether an IC is bad or not. For example, if the signatures at the inputs of U10 pins 9 and 10 (a gate in the Bank Enable Logic) were correct (798P and 3957 respectively), and the output at pin 8 had a bad signature, then the gate between these lines is bad. U10 would then be replaced.

5-6. In table 5-5, you will be given a starting point from which you should start looking at signatures. If a bad signature is encountered, you should follow that signal line back to the next IC. Then monitor all of the inputs to that IC. If any of the inputs have bad signatures, then follow these lines back to the next IC and monitor all of the inputs to this IC. Repeat this procedure until an IC is found that has good inputs and one or more bad outputs. This manual will refer to this IC as the 'source' IC.

5-7. It is very important that the procedure in table 5-5 be followed every time signature analysis is performed on any PMS. This type of troubleshooting is highly dependant on the state that the HP-75 is in. The procedure contained in table 5-5 puts the 75 into a known state. The correct signatures will only be generated when the 75 is in this state. For example, signature analysis has just been performed on a unit and an error was found and corrected. The operator correctly branched back to step B in table 5-1 and reperformed RAMTEST. At this point, if the signatures were checked again, some signatures would have changed. This is because RAMTEST placed the 75 into a different state.

5-7. INITIAL PREPARATION

5-8. Perform the following steps before attempting to troubleshoot the PMS:

a. Visually inspect the unit for physical damage. Replace any assemblies that are physically damaged.

b. Determine the customers concern, if possible. Frequently the customer will include a message with the unit describing the problem.

Table 5-1. Test Procedure

STEP	ACTION
A. TURN ON TEST 1. Be sure the HP-75 is turned off. 2. Plug the PMS into the leftmost port of the HP-75. 3. Press <ATTN>.	If the HP-75 does not turn on, branch to table 5-4.
B. FUNCTIONAL TEST 1. Load "713DIAG" into the HP-75. 2. Type: RAMTEST <RTN>.	If "Bank A..OK", and "Bank B..OK" is displayed, then procede to step C (Battery Test). If "Bank A..Failed Address 6000" is displayed, procede to table 5-5. If a failure is reported at any other address, procede to table 5-6.

C. BATTERY TEST 1. Press <SHIFT-ATTN>. 2. Unplug the PMS. 3. Remove the topcase if not already removed. 4. Measure the battery voltage on the battery case. 5. Lift one end of R3. 6. Connect an ammeter in series with the lifted end of R3 and the pad it came from. 7. Measure the current flow. 8. Measure the current flow again. 9. Reinsert the lifted end of R3.	If the battery voltage is greater than 2.4 volts, procede to step D (POWER USAGE TEST). If the current is less than 35 microamps, then replace the battery (BT1). If the current is less than 35 microamps, then replace the logic board.
D. POWER USAGE TEST 1. Lift one end of W1. 2. Connect an ammeter in series with the lifted end of W1 and the pad it came from. 3. Be sure the HP-75 is turned off. 4. Plug the PMS into the leftmost port of the HP-75.	

5. Press <ATTN>. 6. Type: POWER <RTN>. 7. Measure the current flow. 8. Press <SHIFT-ATTN>. 9. Remove the PMS from the HP-75. 10.Reinsert the lifted end of W1. 11.Reassemble the PMS.	If the current is greater than 26 milliamps. then replace the logic board.

Table 5-2. Wire Jumper (W2) Removal

STEP	ACTION
A. Press <SHIFT-ATTN>. B. Unplug the PMS. C. Remove the top case of the PMS. D. Lift wire jumper W2. E. Return to the previous table.	

STEP	ACTION
A. Press <SHIFT-ATTN>. B. Unplug the PMS. C. Reinsert W2. D. Plug the PMS into the leftmost port of the HP-75. E. Return to the current test in table 5-1 and repeat.	

Table 5-4. No Turn On (Secondary Test)

STEP	ACTION
A. Proceed to table 5-2 and remove W2.	
B. Plug the PMS into the leftmost port of the HP-75.	
C. Press <ATTN>.	If the HP-75 turns on, then go to table 5-5.
D. Press <ATTN> and hold for 3 seconds.	If the HP-75 does not turn on, then procede to table 5-7. If the HP-75 does turn on, then procede to table 5-5.

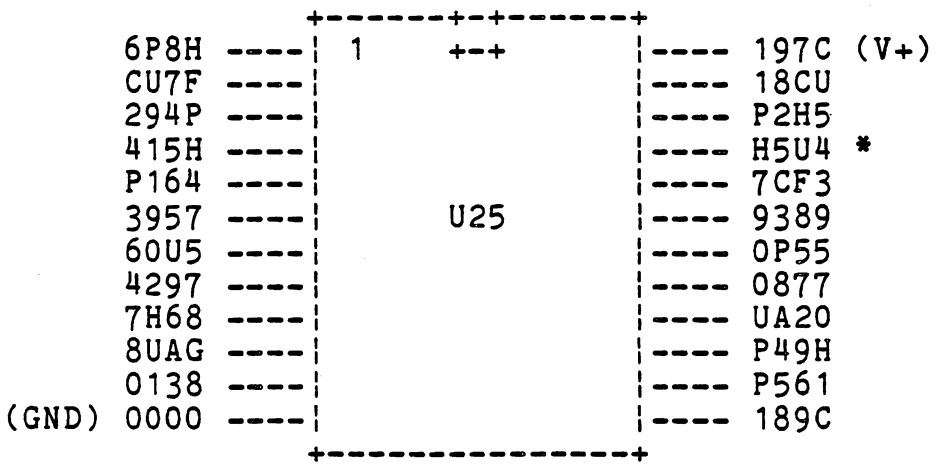
Table 5-5. Signature Analysis Procedure

STEP	ACTION
A. INITIALIZE THE HP-75 NOTE: a. This initialization routine must be performed before signature analysis is attempted. If any other programs or actions are performed on the HP-75 after this initialization routine is performed, none of the signatures can be guaranteed. b. Set the signature analizer so that the START, STOP, and CLOCK lines trigger on a rising pulse.	
1. Procede to table 5-2 and remove W2 of not already removed. 2. Press <SHIFT-CTL-CLEAR>. 3. Plug the PMS into the leftmost port of the HP-75 if not already plugged in. 3. Press <ATTN>, <EDIT>, <EDIT>. 4. Copy "713DIAG" into the HP-75 by typing: COPY CARD TO 'U' <RTN>. 5. Type: 10 SIGNAL & GOTO 10 <RTN>. 6. Type: CLEARVARS <RTN>. 7. Type: <RUN>.	

8. Press the reset button on the signature analizer probe.	The signature 197C should be shown. If not, go back to step 1 and reperform the initialization routine.
9. Probe J1 pin 10.	The signature 7H68 should be shown. If not, go back to step 1 and reperform the initialization routine.
B. TROUBLESHOOTING	
1. Probe all 20 leads of J1, U25, and U13 pin 12 (7CF3) comparing the signatures found to those in figures 5-1, and 5-2.	If any of the signatures are not correct, be sure the 75 has been initialized correctly. If the initialization was performed correctly, then using figure 7-2, locate the bad IC using the method described in paragraph 5-6.

PINS			TYPE	SIGNATURE	CLOCK
		1	VI (+5v)	197C	phase 1
	2		GND	0000	phase 1
3			D7	0877	phase 1
4			D6	UA20	phase 1
		5	D5	P49H	phase 1
	6		D4	P561	phase 1
7			D3	189C	phase 1
8			D2	0138	phase 1
		9	D1	8UA6	phase 1
	10		D0	7H68	phase 1
11			PH. 2 CLK	197C	phase 1
12			PH. 1 CLK	197C	phase 2
		13	PWO (+5v)	197C	phase 2
	14		LMA	26AU	phase 2
15			RD	62C8	phase 2
16			WR	HFUC	phase 2
		17	SEND	----	
	18		GND	0000	phase 1
19			S2 (GND)	0000	phase 1
20			S1 (+5v)	197C	phase 1

Figure 5-1. Connector (J1) Signal Table



* You must clock on the rising edge of the phase 1 clock to see this signal.

Figure 5-2. U25 Signature Diagram

2. Set up an oscilliscope as follows: 2 volts/division 50 microsec/div. + trigger level	
3. Using the oscilloscope, probe the lines with the bad signatures.	If the signal is making the full transition from a logic "0" to a logic "1", then replace the 'source' IC. If the signal is not making the full logic transition, then replace the IC that is being driven by the 'source' IC

NOTE: A bad signature on an address line presents a difficult problem to resolve. Up to 10 ICs can be connected to an address line (including all of the RAM). When dealing with a bad address line, replace the appropriate IC in the RAM address and select circuitry (U5-8, U11, U15, U15). Always replace RAM last.

4. Procede to table 5-3 and reinsert W2.	

Table 5-6. RAM Replacement

STEP	ACTION
A. Press <SHIFT-ATTN>.	
B. Unplug the PMS from the HP-75.	
C. Remove the topcase of the PMS.	
D. RAM failure in bank A.	If 6000 <= "XXXX" < 6800, then replace U18. If 6800 <= "XXXX" < 7000, then replace U19. If 7000 <= "XXXX" < 7800, then replace U20. If 7800 <= "XXXX" < 8000, then replace U21.
E. RAM failure in bank B.	If 6000 <= "XXXX" < 6800, then replace U22. If 6800 <= "XXXX" < 7000, then replace U23. If 7000 <= "XXXX" < 7800, then replace U24. If 7800 <= "XXXX" < 8000, then replace U25.
. Return to table 5-1, step B and repeat.	

Table 5-7. No Turn On Troubleshooting

STEP	ACTION
A. Press <SHIFT-ATTN>.	
B. Unplug the PMS from the HP-75.	
C. Replace the Connector/ Cable assembly.	
D. Plug the PMS into the HP-75.	
E. Press <ATTN>.	If the HP-75 turns on, procede to table 5-3.
F. Unplug the PMS from the HP-75.	
G. Replce the logic board.	
H. Plug the PMS into the HP-75.	
I. Press <ATTN>.	If the HP-75 turns on, procede to step L.
J. Go back to step A.	
K. Press <SHIFT-ATTN>.	
L. Unplug the PMS from the HP-75.	
M. Replace the Connector/ Cable assembly with the original assembly.	
N. Plug the PMS into the HP-75.	
O. Press <ATTN>.	If the HP-75 turns on, then procede to table 5-3.
P. Go back to step A.	

Replaceable Parts

6-1. INTRODUCTION

6-2. This section lists the replaceable parts and assemblies of the PMS. The reorder part number of the complete PMS unit is 82713-69901.

6-3. Parts descriptions, HP part numbers, quantities, and reference designations (where applicable) for the PMS are listed in table 6-1. (The PMS is illustrated in figure 6-1.)

6-4. ORDERING INFORMATION

6-5. To order replacement parts or assemblies, address your order to the Corporate Parts Center or Parts Center Europe. Specify the following information for each part ordered:

a. Product model and serial number.

b. HP part number.

c. Part description.

d. Complete reference designation (if applicable).

Table 6-1. 82713A PMS Replaceable Parts

REFERENCE DESIGNATOR	HP PART NUMBER	DESCRIPTION	QUANTITY
	82713-60901	ASSEMBLY, CABLE/CONNECTOR, SVC	1
	82713-	ASSEMBLY, LOGIC BD. SVC	1
BT1	1420-0275	BATTERY, LITHIUM-IODINE	1
	82713-00011	CABLE CLAMP, BOTTOM	1
	82713-00008	CABLE CLAMP, TOP	1
C5-12	0160-3334	CAPACITOR, .01uf 10%	8
C1-4	0180-2602	CAPACITOR, 47uf 20% 8V	4
	82163-40010	CASE, BOTTOM	1
	82163-40011	CASE, TOP	1
CR1-2	1901-0868	DIODE, SCHOTTKY BARRIER	2
	0403-0432	FOOT	2
	5040-9207	FOOT	4
U18-25	1818-1738	IC, MEMORY	8
U5-8	1820-1391	IC, MM74C161N	4
U2,14	1820-1562	IC, MM74C175N	2
U3,13	1820-1627	IC, MM74C02N	2
U1,12	1820-2210	IC, MM74C00N	2
U10	1820-2213	IC, MM74C32N	1
U4	1820-2215	IC, MM74C373N	1
U9	1820-2276	IC, 74C86	1
U11,16	1820-2907	IC, TC40H138P	2
U15,17	1820-3014	IC, 74HC139	2
	82713-90008	LABEL, BOTTOM	1
	7121-4056	LABEL, IDENTIFICATION	1
	0590-0199	NUT, HEX, WITH LOCKWASHER	2
	82713-00004	PANEL, REAR, PAINTED	1
R3	0698-3445	RESISTER, 348 OHM 1% .125W	1
R1,2	1810-0454	RESISTER, NETWORK, SIP	2
	0624-0400	SCREW, TAPPING 6-19	3
	2200-0147	SCREW, MACHINE 4-40	2
W1,2	8159-0005	WIRE, JUMPER 0 OHMS	2

Reference Diagrams

7-1. This section includes reference diagrams for the HP 82713A Plug-In Module Simulator.

7-2. The component location diagram for the logic board, the logic board schematic, and the buffer board schematic are shown in figures 7-1, 7-2, and 7-3 respectively.

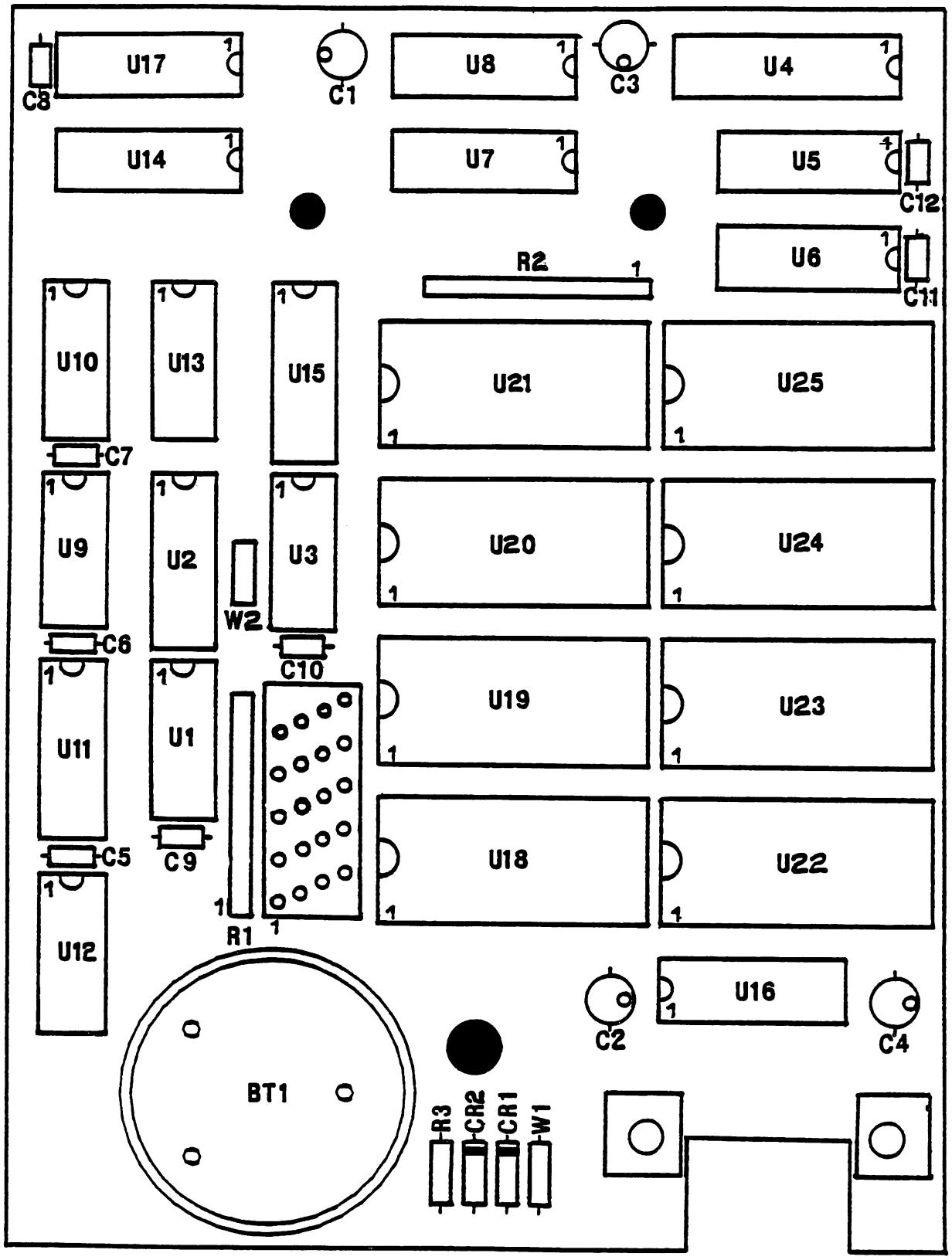
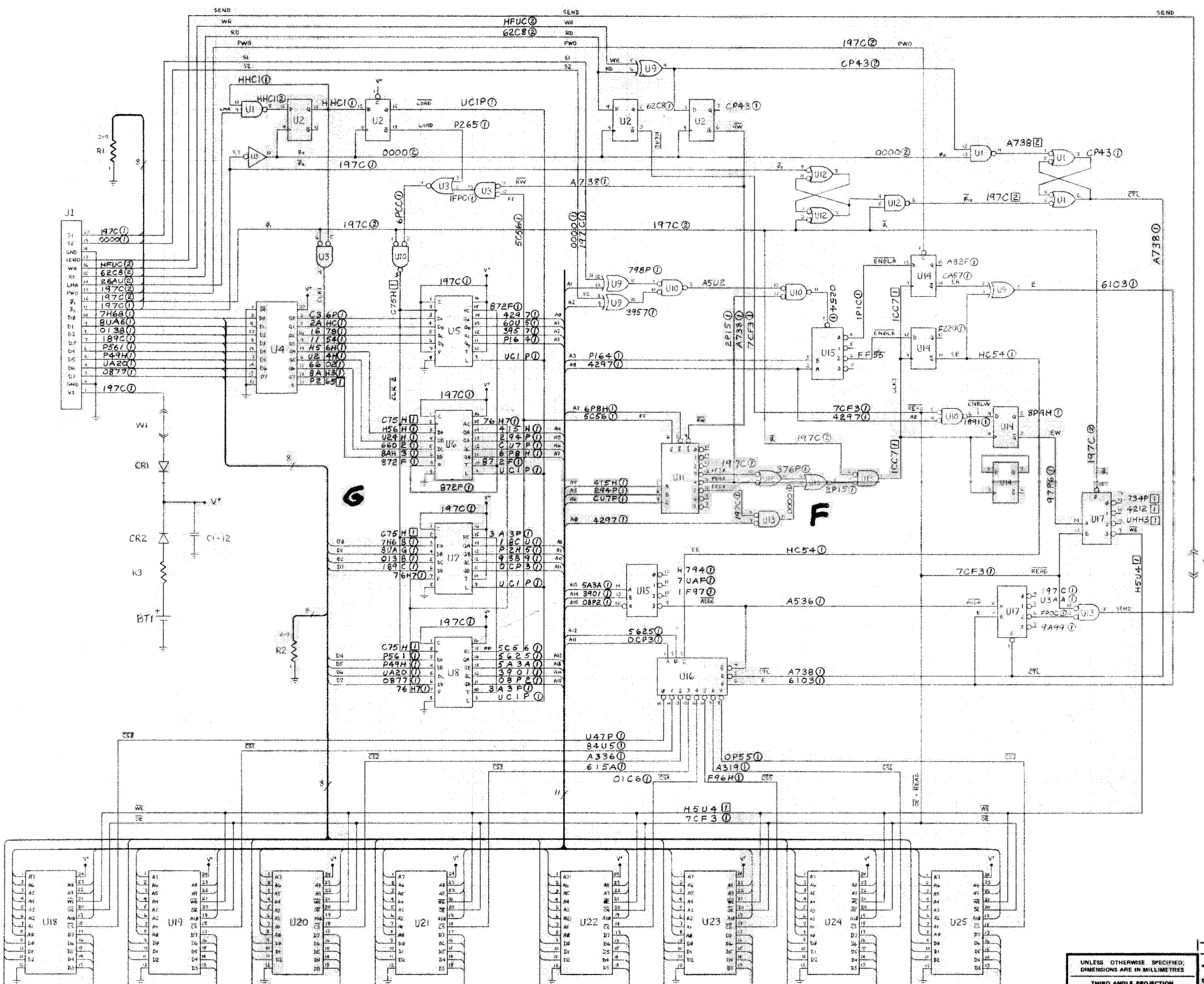


Figure 7-1. Component Location Diagram

1000 N.E. Circle Blvd., Corvallis, OR 97330, U.S.A.

82713-90010

Printed in U.S.A.



SIGNATURE CLOCK SYMBOLS

SYMBOL	CLOCK
①	PHASE 1
1 (boxed)	PHASE 1
②	PHASE 2
2 (boxed)	PHASE 2

REVISIONS: A — AS ISSUED

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN MILLIMETRES
THIRD ANGLE PROJECTION
TOLERANCES: XX ± 0.5 mm or ± 0.4 mm; XX.X ± 0.2 mm or ± 0.1 mm
STRIKE OUT ONE XX AND ONE XX.X
SEE CORP. STD. 808
DO NOT SCALE THIS DRAWING

DRAWN BY: MIKE CARLIN — 7-20-82
ENGINEER: MIKE CARLIN — 7-20-82
RELEASE TO PROD.: 1-11-83
SUPERSEDES DWG.: D-82713-60001-50 REV 2 — 4-12-82

TITLE: LOGIC BOARD SCHEMATIC
NEXT ASSEMBLY: 82713-69901
HEWLETT PACKARD
PART NUMBER: 82713-60001
D-82713-60001-50